

2.5V 20-Bit Universal Bus Driver with 3-State Outputs

Product Features

- PI74AVC+16836 is designed for low voltage operation, $V_{CC} = 1.65V$ to $3.6V$
- True $\pm 24mA$ Balanced Drive @ $3.3V$
- I_{OFF} supports partial power-down operation
- $3.6V$ I/O Tolerant inputs and outputs
- Meets PC133 SDRAM Registered DIMM Specifications
- All outputs contain a patented DDC (Dynamic Drive Control) circuit that reduces noise without degrading propagation delay
- Industrial operation at $-40^{\circ}C$ to $+85^{\circ}C$
- Available Packages:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 173 mil wide plastic TVSOP (K)

Product Description

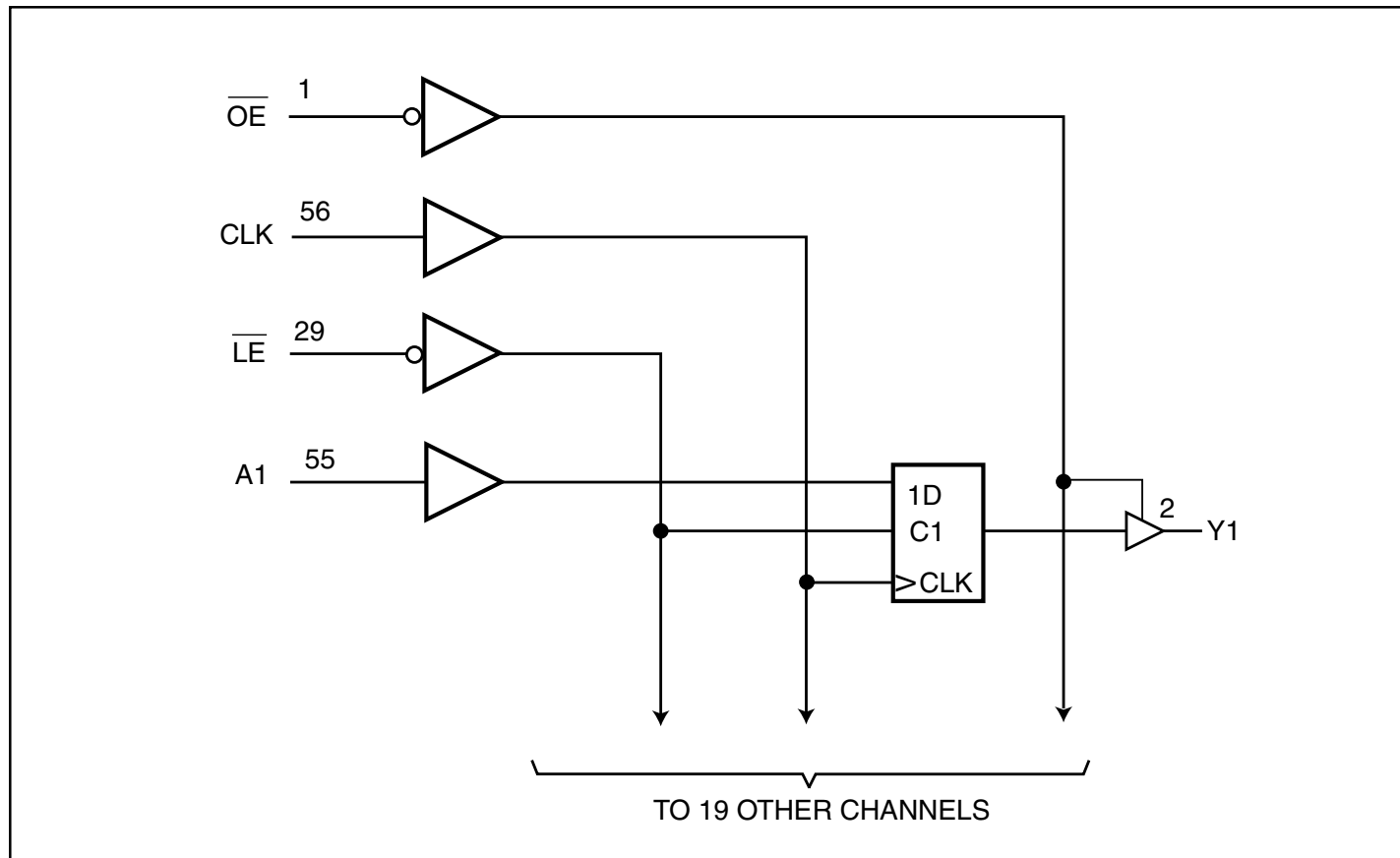
Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

The 20-bit PI74AVC+16836 universal bus driver is designed for $1.65V$ to $3.6V$ V_{CC} operation.

Data flow from A to Y is controlled by the Output Enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable ($\overline{LE}$) input is LOW. When $\overline{LE}$ is HIGH, the A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is HIGH, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state, but all the inputs are enabled and data is capable of being stored in the register.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{LE}$	Latch Enable (Active LOW)
CLK	Clock Input
A	Data Input
Y	Data Output
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs				Outputs Y
$\overline{OE}$	$\overline{LE}$	CLK	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y ₀ ⁽²⁾

Pin Configuration

$\overline{OE}$	1	56	CLK
Y1	2	55	A1
Y2	3	54	A2
GND	4	53	GND
Y3	5	52	A3
Y4	6	51	A4
Vcc	7	50	Vcc
Y5	8	49	A5
Y6	9	48	A6
Y7	10	47	A7
GND	11	46	GND
Y8	12	45	A8
Y9	13	44	A9
Y10	14	43	A10
Y11	15	42	A11
Y12	16	41	A12
Y13	17	40	A13
GND	18	39	GND
Y14	19	38	A14
Y15	20	37	A15
Y16	21	36	A16
Vcc	22	35	Vcc
Y17	23	34	A17
Y18	24	33	A18
GND	25	32	GND
Y19	26	31	A19
Y20	27	30	A20
NC	28	29	$\overline{LE}$

Note:

- 1 H = High Signal Level
L = Low Signal Level
Z = High Impedance
↑ = Transition LOW-to-HIGH
X = Irrelevant
2. Output level before the indicated steady-state input conditions were established.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V_{CC}	–0.5V to +4.6V
Input voltage range, V_I	–0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, $V_O^{(1)}$	–0.5V to +4.6V
Voltage range applied to any output in the high or low state, $V_O^{(1,2)}$	–0.5V to $V_{CC}+0.5V$
Input clamp current, I_{IK} ($V_I < 0$)	–50mA
Output clamp current, I_{OK} ($V_O < 0$)	–50mA
Continuous output current, I_O	±50mA
Continuous current through each V_{CC} or GND	±100mA
Package thermal impedance, $\theta_{JA}^{(3)}$: package A	64°C/W
package K	48°C/W
Storage Temperature range, T_{stg}	–65°C to 150°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:

1. Input & output negative-voltage ratings may be exceeded if the input and output current rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions⁽¹⁾

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	$V_{CC} = 1.2V$	V_{CC}		
	$V_{CC} = 1.65V$ to 1.95V	$0.65 \times V_{CC}$		
	$V_{CC} = 2.3V$ to 2.7V	1.7		
	$V_{CC} = 3V$ to 3.6V	2		
V_{IL} Low-level Input Voltage	$V_{CC} = 1.2V$		Gnd	
	$V_{CC} = 1.65V$ to 1.95V		$0.35 \times V_{CC}$	
	$V_{CC} = 2.3V$ to 2.7V		0.7	
	$V_{CC} = 3V$ to 3.6V		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OH} High-level output current	$V_{CC} = 1.65V$ to 1.95V		– 6	mA
	$V_{CC} = 2.3V$ to 2.7V		– 12	
	$V_{CC} = 3V$ to 3.6V		– 24	
I_{OL} Low-level output current	$V_{CC} = 1.65V$ to 1.95V		6	
	$V_{CC} = 2.3V$ to 2.7V		12	
	$V_{CC} = 3V$ to 3.6V		24	
$\Delta t \Delta v$ Input transition rise or fall rate	$V_{CC} = 1.65V$ to 3.6V		5	ns/V
T_A Operating free-air temperature		–40	85	°C

Notes:

1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$)

Parameters		Test Conditions ⁽¹⁾	V_{CC}	Min.	Max.	Units
V_{OH}		$I_{OH} = -100\mu\text{A}$	1.65V to 3.6V	$V_{CC} - 0.2\text{V}$		V
		$I_{OH} = -6\text{mA}$ $V_{IH} = 1.07\text{V}$	1.65V	1.2		
		$I_{OH} = -12\text{mA}$ $V_{IH} = 1.7\text{V}$	2.3V	1.75		
		$I_{OH} = -24\text{mA}$ $V_{IH} = 2\text{V}$	3V	2.0		
V_{OL}		$I_{OL} = 100\mu\text{A}$	1.65V to 3.6V		0.2	
		$I_{OL} = 6\text{mA}$ $V_{IH} = 0.57\text{V}$	1.65V		0.45	
		$I_{OL} = 12\text{mA}$ $V_{IH} = 0.7\text{V}$	2.3V		0.55	
		$I_{OL} = 24\text{mA}$ $V_{IH} = 0.8\text{V}$	3V		0.8	
I_I	Control Inputs	$V_I = V_{CC}$ or GND	3.6V		± 2.5	μA
I_{OFF}		V_I or $V_O = 3.6\text{V}$	0		± 10	
I_{OZ}		$V_I = V_{CC}$ or GND	3.6V		± 10	
I_{CC}		$V_O = V_{CC}$ or GND $I_O = 0$	3.6V		40	
C_I	Control Inputs	$V_I = V_{CC}$ or GND	2.5V		4	pF
			3.3V		4	
	Data Inputs		2.5V		6	
			3.3V		6	
C_O	Outputs	$V_O = V_{CC}$ or GND	2.5V		8	
			3.3V		8	

Note: Typical values are measured at $T_A = 25^{\circ}\text{C}$.

Timing Requirements (Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

			V _{CC} = 1.2V		V _{CC} = 1.5V ±0.1V		V _{CC} = 1.8V ±0.15V		V _{CC} = 2.5V ±0.2V		V _{CC} = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f _{clock}	Clock Frequency							180		180		180	MHz
t _w Pulse Duration	LE Low						2.0		1.2		1.0		ns
	CLK High or Low						2.0		1.2		1.0		
t _{su} Setup Time	Data before CLK↑						1.4		1.2		1.0		
	Data before LE↑	CLK High					1.4		1.2		1.0		
		CLK Low					1.4		1.2		1.0		
t _h Hold Time	Data after CLK↑						1.0		0.8		0.6		
	Data after LE↑	CLK High or Low					1.0		0.8		0.6		

Switching Characteristics over recommended operating free-air temperature range

(unless otherwise noted, see Figures 1 thru 4)

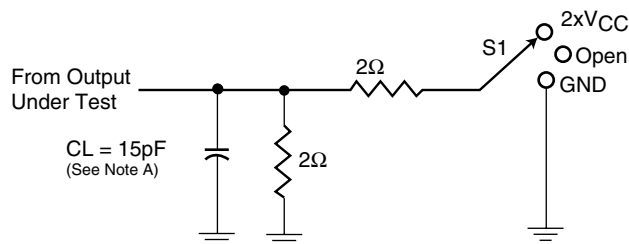
Parameters	From (Input)	To (Output)	V _{CC} = 1.2V		V _{CC} = 1.5V ±0.1V		V _{CC} = 1.8V ±0.15V		V _{CC} = 2.5V ±0.2V		V _{CC} = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f _{max}							180		180		180		MHz
t _{pd}	A	Y					1.0	4.5	0.8	3.0	0.7	2.4	ns
	LE						1.0	5.0	0.8	3.3	0.7	2.5	
	CLK						1.0	4.5	0.8	3.0	0.7	2.5	
t _{en}	OE						1.5	5.5	1.0	4.5	1.0	4.0	
t _{dis}	OE						1.5	5.0	1.0	4.5	1.0	4.0	

Operating Characteristics, T_A = 25°C

Parameters		Test Conditions	V _{CC} = 1.8V ±0.1V	V _{CC} = 2.5V ±0.2V	V _{CC} = 3.3V ±0.3V	Units
			Typical	Typical	Typical	
C _{pd} Power Dissipation Capacitance	Outputs Enabled	C _L = 0pF, f = 10 MHz	48	50	55	pF
	Outputs Disabled		25	28	32	

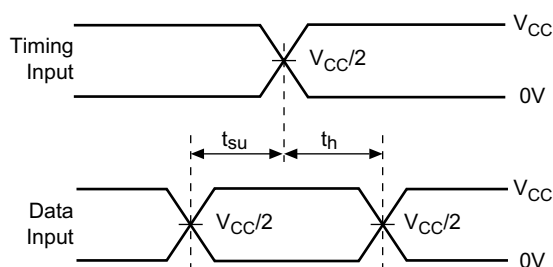
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2V \text{ AND } 1.5V \pm 0.1V$

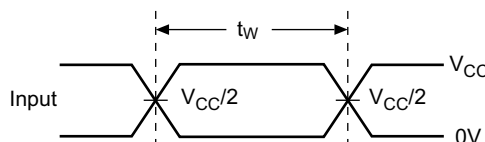


Load Circuit

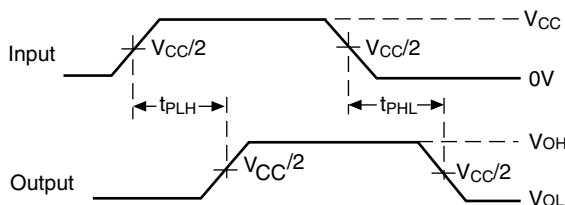
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



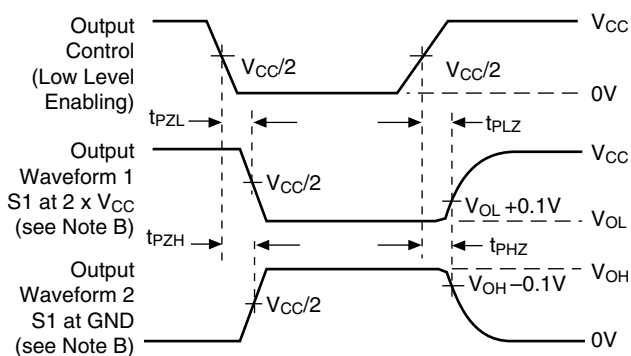
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

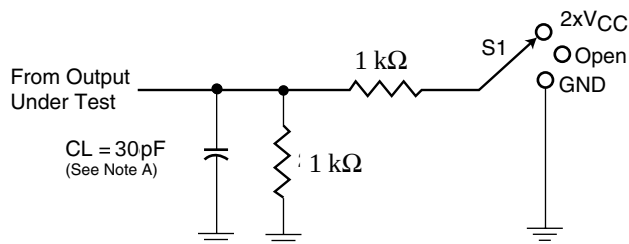
Figure 1. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0ns$, $t_F \leq 2.0ns$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

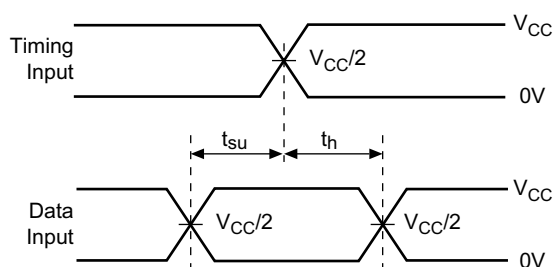
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8V \pm 0.15V$$

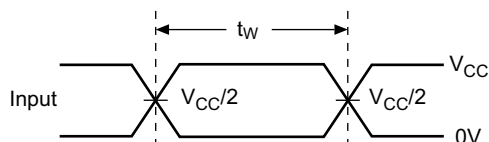


Load Circuit

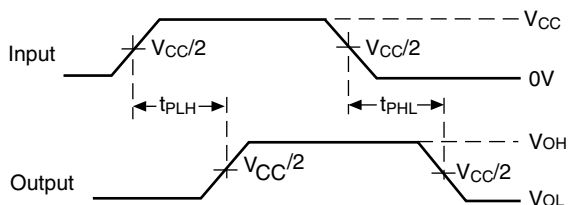
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x VCC GND



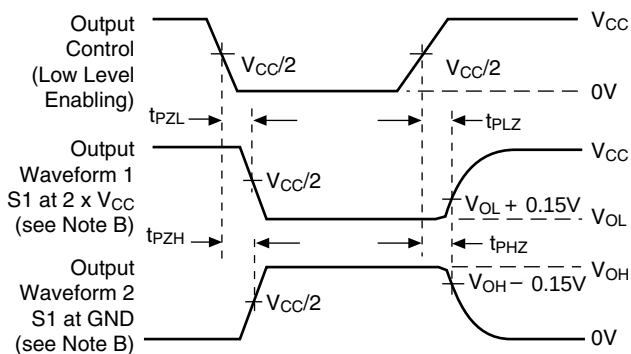
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

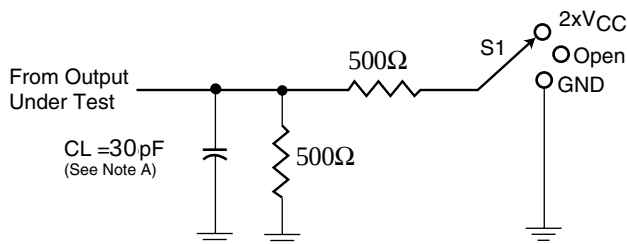
Figure 2. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having these characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 0.1ns$, $t_F \leq 0.1ns$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

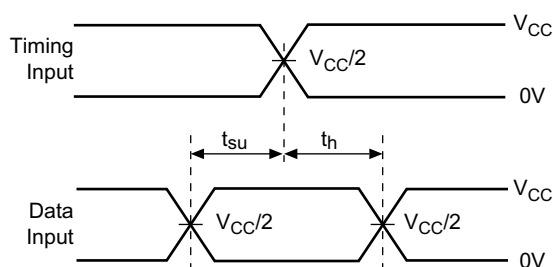
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5V \pm 0.2V$$

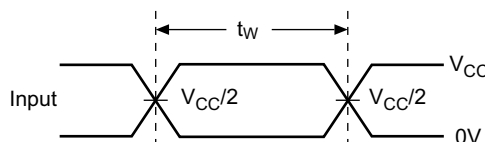


Load Circuit

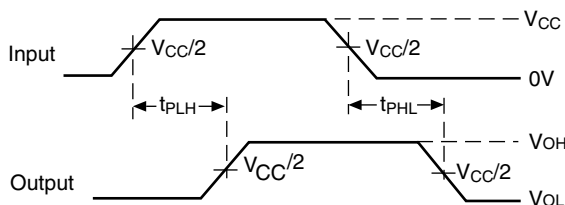
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x V_{CC} GND



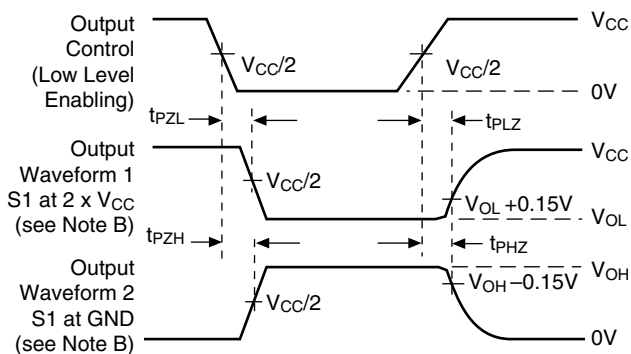
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

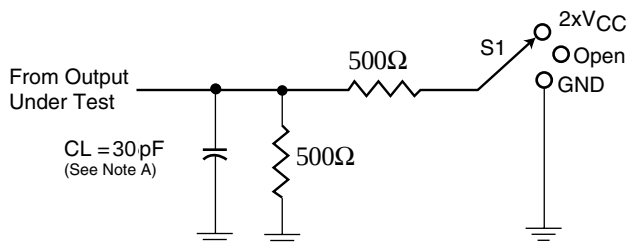
Figure 3. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having these characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 0.5\text{ns}$, $t_F \leq 0.5\text{ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

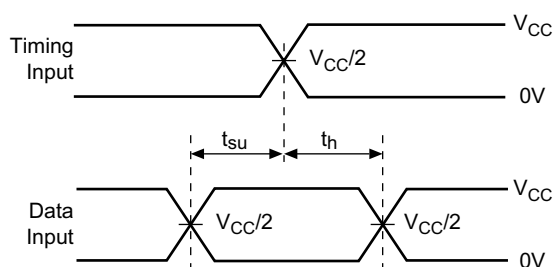
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3V \pm 0.3V$$

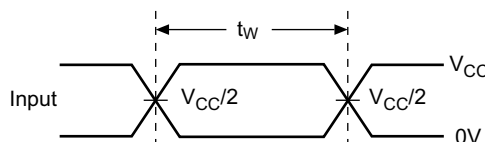


Load Circuit

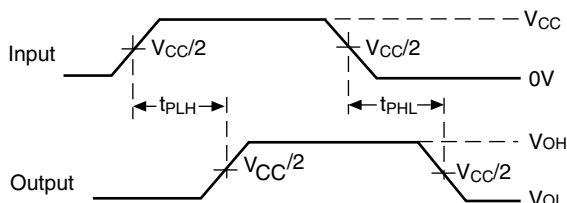
Test	S1
t _{pd} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 x V _{CC} GND



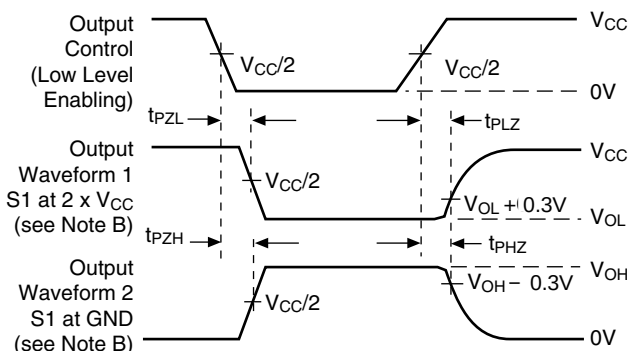
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

Figure 4. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having these characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 0.5ns, t_F ≤ 0.5ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}