


**SANYO Semiconductors**

# DATA SHEET

An ON Semiconductor Company

## LC72725KM, — CMOS IC LC72725KV RDS(RBDS) Demodulation IC

### Overview

The LC72725KM and LC72725KV are ICs that implement the signal processing required by the European Broadcasting Union RDS (Radio Data System) standard and by the US NRSC (National Radio System Committee) RBDS (Radio Broadcast Data System) standard. These ICs include band-pass filter, demodulator, and data buffer on chip. RDS data can be read out from this on-chip memory by external clock input in slave operation mode.

### Functions

- Bandpass filter: Switched capacitor filter (SCF)
- RDS Demodulation: 57KHz carrier and RDS data clock regeneration, biphasic decode, differential decode.
- Buffer: 128 bit (about 100ms) can be restored in the on-chip data buffer RAM.
- Data output: Master or slave output mode can be selected.
- RDS-ID: Detect RDS signal which can be reset by RST signal input.
- Standby control: Crystal oscillator can be stopped.
- Fully adjustment free
- Low Voltage

### Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$ ,  $V_{SSd} = V_{SSa} = 0\text{V}$

Parameter	Symbol	Pin Name	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	$V_{DDd}$ , $V_{DDa}$ *	$V_{DDa} \leq V_{DDd} + 0.3\text{V}$	-0.3 to +6.5	V
Maximum input voltage	$V_{IN1\text{ max}}$	TEST, MODE, XIN, RDCL, RST		-0.3 to $V_{DDd} + 0.3$	V
	$V_{IN2\text{ max}}$	MPXIN, CIN		-0.3 to $V_{DDa} + 0.3$	V
Maximum output voltage	$V_{O1\text{ max}}$	RDS-ID(READY)		-0.3 to +6.5	V
	$V_{O2\text{ max}}$	XOUT, RDDA, RDCL		-0.3 to $V_{DDd} + 0.3$	V
	$V_{O3\text{ max}}$	FLOUT		-0.3 to $V_{DDa} + 0.3$	V
Maximum output current	$I_{O1\text{ max}}$	XOUT, FLOUT, RDDA, RDCL		+2.0	mA
	$I_{O2\text{ max}}$	RDS-ID(READY)		+8.0	mA

\*  $V_{DDa} \leq V_{DDd} + 0.3\text{V}$

Continued on next page.

■ Any and all SANYO Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO Semiconductor representative nearest you before using any SANYO Semiconductor products described or contained herein in such applications.

■ SANYO Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor products described or contained herein.

**SANYO Semiconductor Co., Ltd.**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## LC72725KM, 72725KV

Continued from preceding page.

Parameter	Symbol	Pin Name	Conditions	Ratings	Unit
Allowable power dissipation	Pd max		(Ta≤85°C)MFP16	140	mW
			(Ta≤85°C)SSOP16	100	mW
Operating temperature	Topr1		V <sub>DD</sub> = 2.7V to 5.5V	-20 to +70	°C
	Topr2		V <sub>DD</sub> = 3.0V to 5.5V	-40 to +85	°C
Storage temperature	Tstg			-40 to +125	°C

**Allowable Operating Ranges** at Ta = -20 to +70°C, V<sub>SSd</sub> = V<sub>SSa</sub> = 0V, V<sub>DDd</sub> = V<sub>DDa</sub> = 2.7V to 5.5V

Ta = -40 to +85°C, V<sub>SSd</sub> = V<sub>SSa</sub> = 0V, V<sub>DDd</sub> = V<sub>DDa</sub> = 3.0V to 5.5V

Parameter	Symbol	Pin Name	Conditions	Ratings			unit
				min	typ	max	
Supply voltage	V <sub>DD1</sub>	V <sub>DDd</sub> , V <sub>DDa</sub>	Ta = -20 to +70°C	2.7		5.5	V
	V <sub>DD2</sub>	V <sub>DDd</sub> , V <sub>DDa</sub>	Ta = -40 to +85°C	3.0		5.5	
Input high-level voltage	V <sub>IH1</sub>	TEST, MODE, RST		0.7V <sub>DDd</sub>		6.5	V
	V <sub>IH2</sub>	RDCL		0.7V <sub>DDd</sub>		V <sub>DDd</sub>	V
Input low-level voltage	V <sub>IL</sub>	TEST, MODE, RST, RDCL		0		0.3V <sub>DDd</sub>	V
Output voltage	V <sub>O1</sub>	RDDA, RDCL				V <sub>DDd</sub>	V
	V <sub>O2</sub>	RDS-ID(READY)				6.5	V
Input amplitude	V <sub>IN</sub>	MPXIN	f = 57±2kHz	1.6		50	mVrms
	VXIN	XIN		400		1500	mVrms
Guaranteed crystal oscillator frequencies	Xtal	XIN, XOUT	Cl≤120Ω		4.332		MHz
Crystal oscillator operating range	TXtal	XIN, XOUT	Fo = 4.332MHz			±100	ppm
RDCL setup time	t <sub>CS</sub>	RDCL, RDDA		0			μs
RDCL high-level time	t <sub>CH</sub>	RDCL		0.75			μs
RDCL low-level time	t <sub>CL</sub>	RDCL		0.75			μs
Data output time	t <sub>DC</sub>	RDCL, RDDA				0.75	μs
READY output time	t <sub>RC</sub>	RDCL, READY				0.75	μs
READY low-level time	t <sub>RL</sub>	READY				107	ms

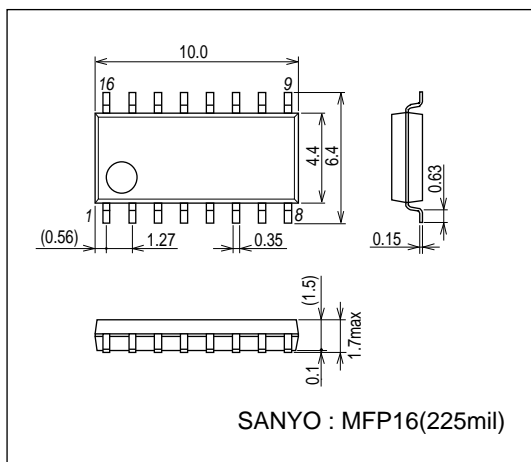
# LC72725KM, 72725KV

## Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin Name	Conditions	Ratings			unit
				min	typ	max	
Input resistance	Rmpxin	MPXIN-V <sub>SSa</sub>	f = 57kHz		100		kΩ
	Rcin	CIN-V <sub>SSa</sub>	f = 57kHz		100		kΩ
Internal feedback resistance	Rf	XIN			1.0		MΩ
Center frequency	fc	FLOUT		56.5	57.0	57.5	kHz
-3dB band width	BW-3dB	FLOUT		2.5	3.0	3.5	kHz
Gain	Gain	MPXIN-FLOUT	f = 57kHz	28	31	34	dB
Stop band attenuation	Att1	FLOUT	Δf = ±7kHz	30			dB
	Att2	FLOUT	F < 45kHz, f > 70kHz	40			dB
	Att3	FLOUT	F < 20kHz	50			dB
Reference voltage output	Vref	Vref	V <sub>DDa</sub> = 3V		1.5		V
Hysteresis	VHIS	TEST, MODE, RST, RDCL			0.1V <sub>DDd</sub>		V
Output low-level voltage	V <sub>OL1</sub>	RDDA, RDCL	I = 2mA			0.4	V
	V <sub>OL2</sub>	RDS-ID(READY)	I = 8mA			0.4	V
Output high-level voltage	V <sub>OH</sub>	RDDA, RDCL	I = 2mA	V <sub>DDd</sub> -0.4			V
Input high-level current	I <sub>IH1</sub>	TEST, MODE, RST, RDCL	V <sub>I</sub> = 6.5V			5.0	μA
	I <sub>IH2</sub>	XIN	V <sub>I</sub> = V <sub>DDd</sub>	2.0		11	μA
Input low-level current	I <sub>IL1</sub>	TEST, MODE, RST, RDCL	V <sub>I</sub> = 0V			5.0	μA
	I <sub>IL2</sub>	XIN	V <sub>I</sub> = 0V	2.0		11	μA
Output off leakage current	IOFF	RDS-ID(READY)	V <sub>O</sub> = 6.5V			5.0	μA
Current drain	I <sub>DD</sub>	V <sub>DDd</sub> +V <sub>DDa</sub>	V <sub>DDd</sub> +V <sub>DDa</sub> (V <sub>DDd</sub> = V <sub>DDa</sub> = 3V)		5		mA

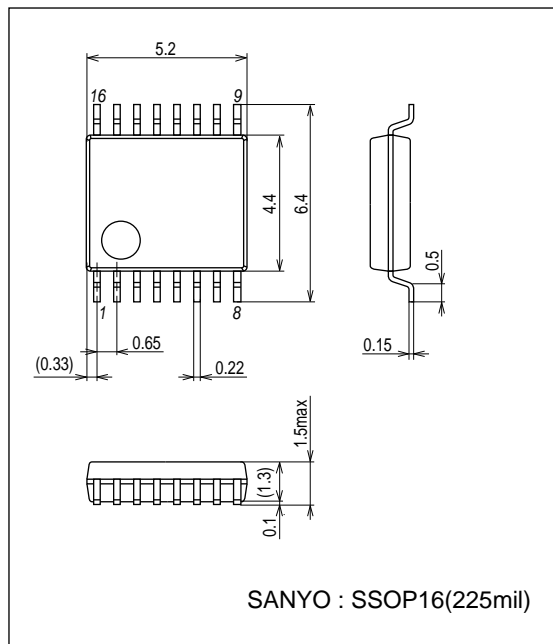
### Package Dimensions

unit : mm (typ)  
3035B [LC72725KM]



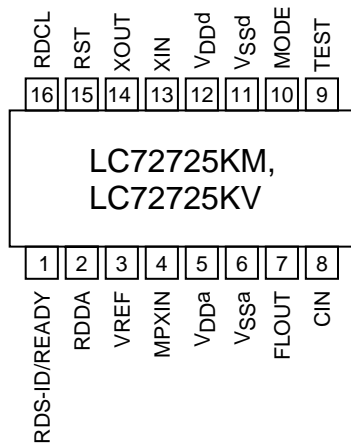
### Package Dimensions

unit : mm (typ)  
3178B [LC72725KV]



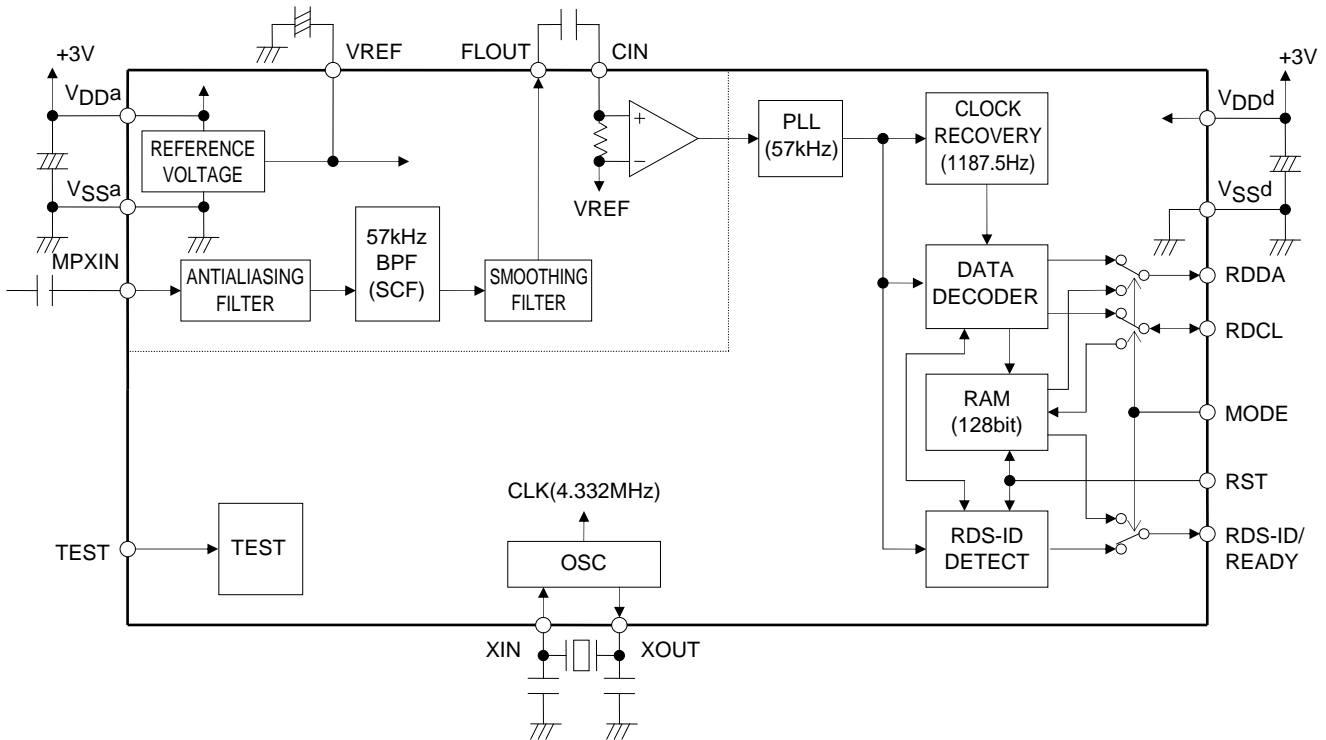
# LC72725KM, 72725KV

## Pin Assignment



Top view

## Block Diagram



# LC72725KM, 72725KV

## Pin Descriptions

Pin No.	Pin Name	I/O	Function	Pin Circuit
3	VREF	Output	Reference voltage output ( $V_{DDa}/2$ )	
4	MPXIN	Input	Baseband (multiplexed) signal input	
7	FLOUT	Output	Subcarrier output (filter output)	
8	CIN	Input	Subcarrier input (comparator input)	
5	$V_{DDa}$	-	Analog system power supply (+3V)	
6	$V_{SSa}$	-	Analog system ground	
14	XOUT	Output	Crystal oscillator output (4.332MHz)	
13	XIN	Input	Crystal oscillator input (external reference signal input)	
9	TEST		Test input	
10	MODE		Read out mode (0:master, 1:slave)	
15	RST		RDS-ID/RAM reset (active high)	
2	RDDA	Output	RDS data output	
16	RDCL	I/O	RDS clock output (master mode) / RDS read out clock input (slave mode)	
1	RDS-ID/ READY	Output	RDS reliability data output (High: data with high RDS reliability Low: data with low RDS reliability) READY output (active high)	
12	$V_{DDd}$	-	Digital system power supply (+3V)	
11	$V_{SSd}$	-	Digital system ground	

# LC72725KM, 72725KV

## Input/Output Data Format

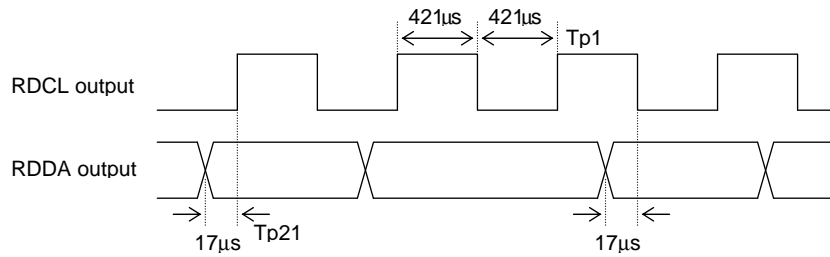
TEST	MODE	Circuit Operation Mode	RDCL Pin	RDS-ID/READY Pin
0	0	Master read out mode	Clock output	RDS-ID output
0	1	Slave read out mode	Clock input	READY output
1	0	Standby mode (crystal oscillator stopped)	-	-
1	1	IC test mode which is not available to user applications.	-	-

RST Pin	
RST = 0	Normal operation
RST = 1	RDS-ID • demodulation circuit clear + READY • memory clear (when slave mode)

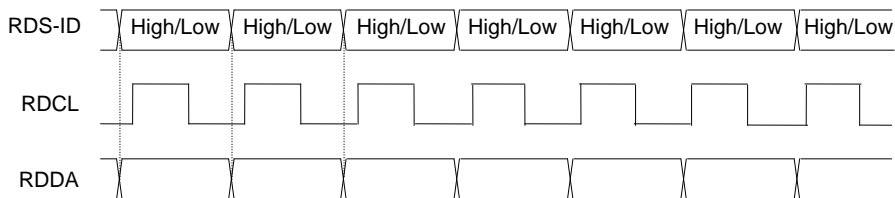
RDS-ID/READY Pin	
Master mode	RDS-ID output (Active-high)
Slave mode	READY output (Active-high)

Note: RDS-ID(READY) pin is an n-channel open-drain output, and requires an external pull-up resistor to output data.

## RDCL/RDDA Output Timing in Master Mode

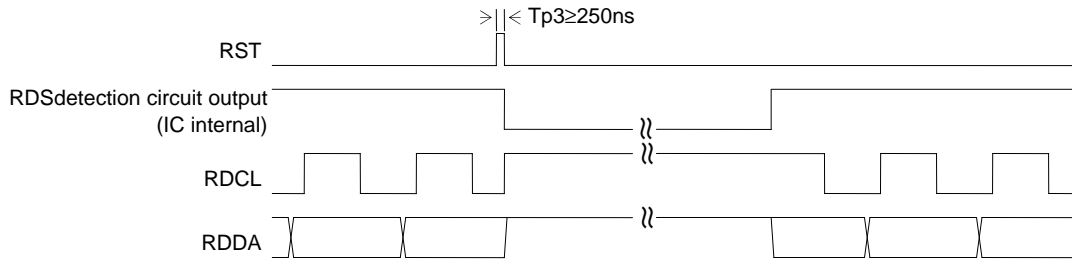


## RDS-ID Output Timing



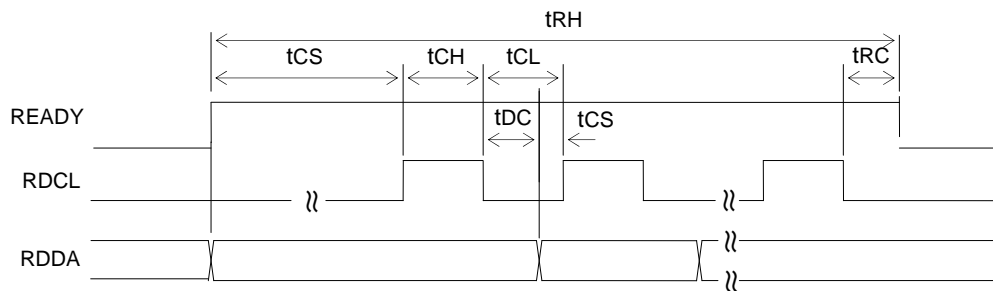
Note: RDS-ID is High: data with high RDS reliability, Low: data with low RDS reliability

### RST Operation in Master Mode



Note: RDCL and RDDA outputs keep high level after input of RST until RDS detection circuit output is detected.

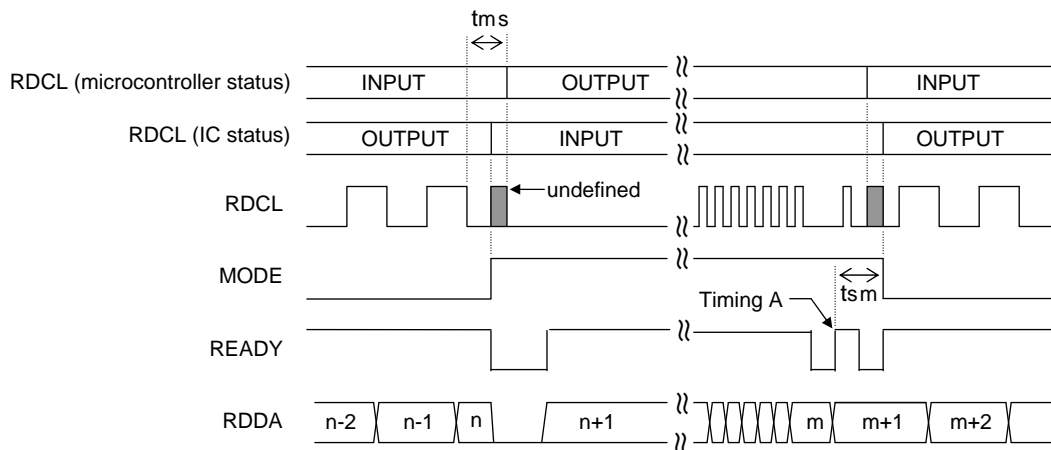
### RDCL Operation in Slave Mode



Parameter	Symbol	Pin Name	Conditions	Ratings			unit
				min	typ	max	
RDCL setup time	tCS	RDCL,RDDA		0			μs
RDCL high-level time	tCH	RDCL		0.75			μs
RDCL low-level time	tCL	RDCL		0.75			μs
Data output time	tDC	RDCL,RDDA				0.75	μs
READY output time	tRC	RDCL,READY				0.75	μs
READY high-level time	tRH	READY				107	ms

## LC72725KM, 72725KV

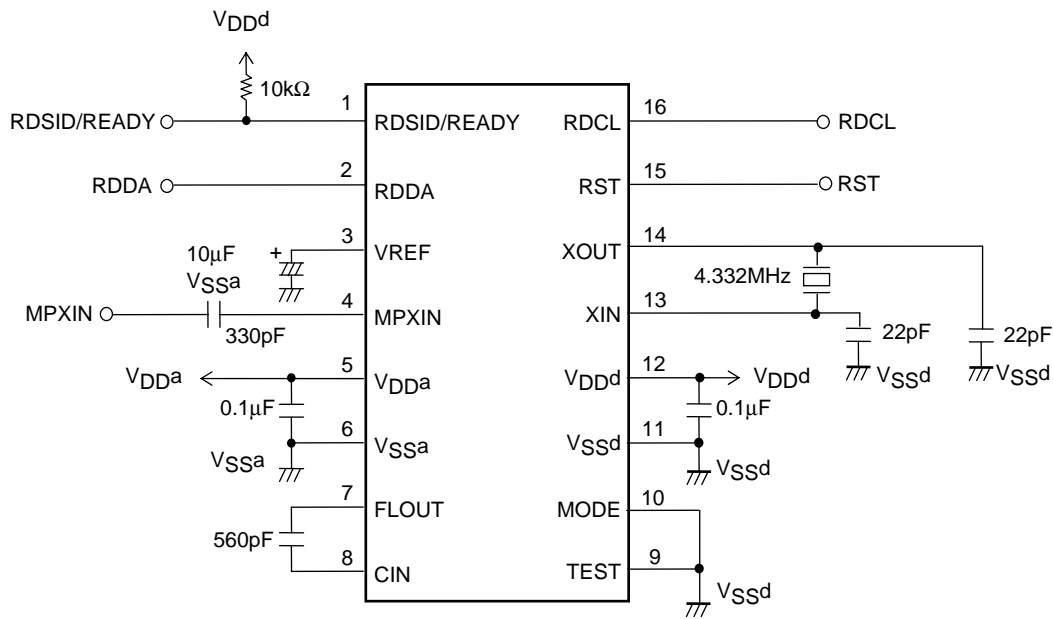
- Notes:
1. RDCL input must be started after READY signal goes high. When READY signal is low, RDCL must be low level.
  2. READY status must be checked after  $t_{RC}$  time from RDCL is set low. If the READY status is high, then next read cycle can be continued. If the READY status is low, next RDCL clock input must be stopped.
  3. If the above condition is satisfied, RDS data (RDDA) can be read out at both rising and falling edge of RDCL.
  4. READY signal goes low after the last data is read out from on-chip memory. If one RDS data is stored in the memory, READY signal goes high again.
  5. When the reception channel is changed, a memory and READY reset must be applied using RST input. If a reset is not applied, reception data from the previous channel may remain in memory. If RST input is applied, reception data is not stored in memory until the first RDS-ID is detected, and READY output goes high after the first RDS-ID is detected. After the first RDS-ID is detected, reception data is stored even if RDS-ID is not detected.
  6. The readout mode may be switched between master and slave modes during readout. Applications must observe the following points to assure data continuity during this operation.
    - 1) Data acquisition timing in master mode  
Data must be read on the falling edge of RDCL
    - 2) Timing of the switch from master mode to slave mode  
After the RDCL output goes low and the RDDA data has been acquired, the application must set MODE high immediately.  
Then, the microcontroller starts output by setting the RDCL signal low.  
The microcontroller RDCL output must start within  $840\mu\text{s}$  ( $t_{ms}$ ) after RDCL went low.  
In this case, if the last data read in master mode was data item  $n$ , then data starting with item  $n+1$  will be written to memory.
    - 3) Timing of the switch from slave mode to master mode  
After all data has been read from memory and READY has gone high, the application must then wait until READY goes low once again the next time (timing A in the figure), immediately read out one bit of data and input the RDCL clock.  
Then, at the point READY goes high, the microcontroller must terminate RDCL output and then set MODE low.  
The application must switch MODE to low within  $840\mu\text{s}$  ( $t_{ms}$ ) after READY goes low (timing A in the figure).





## LC72725KM, 72725KV

### Sample Application Connection Circuit (for master mode operation)



Note: If the RST pin is unused, it must be connected to ground.

- Specifications of any and all SANYO Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Semiconductor Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Semiconductor Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of September, 2006. Specifications and information herein are subject to change without notice.