# ACT–S512K32 High Speed 16 Megabit SRAM Multichip Module

## Features

- 4 Low Power CMOS 512K x 8 SRAMs in one MCM
- Factory configured as 512K x 32; User configurable as 1M x 16 or 2M x 8
- Input and Output TTL & CMOS Compatible Design
- Fast 17,20,25,35,45,55nS Access Times
- Full Commercial and Industrial (-55°C to +125°C) Temperature Range
- +5 V Power Supply
- Available in two Surface Mount Packages, and one PGA Type Package
  - 68–Lead, Low Profile CQFP(F1), 1.56"SQ x .140"max
  - 68–Lead, Dual-Cavity CQFP(F2), 0.88"SQ x .20"max (.18 max thickness available, contact factory for details) *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
  - 66–Lead, PGA-Type(P1), 1.38"SQ x .245"max
- Internal Decoupling Capacitors
- DESC SMD# 5962–94611 Released(P1,F2)
  5962–95624 Released(F1)

AEROFLEX CIRCUIT TECHNOLOGY

## General Description

The ACT–S512K32 is a High Speed, 16 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range industrial, military, or space, mass memory and fast cache applications.

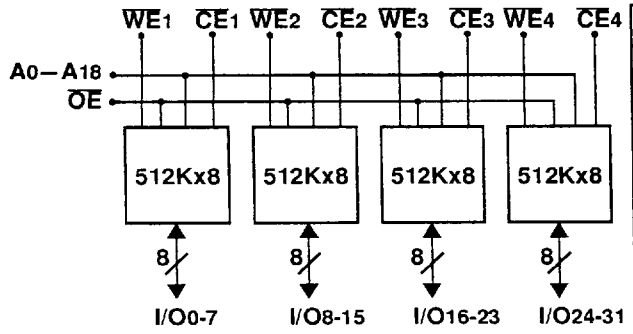
The MCM can be organized as a 512K x 32 bit, 1M x 16 bit or 2M x 8 bit device and is input and output TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and output enable ($\overline{OE}$) are both low. Access time grades of 17nS (-40°C to +85°C), 20nS, 25nS, 35nS, 45nS and 55nS maximum are standard high speed versions.

The +5 Volt power supply version is standard and +3.3 Volt lower power model is a future optional product.

The products are designed for operation over the temperature range of -55°C to +125°C and under the full military environment. DESC Standard Military Drawing (SMD) numbers are released.

The ACT-S512K32 is manufactured in Aeroflex's 80,000 square foot MIL-PRF-38534 certified facility in Plainview, N.Y.

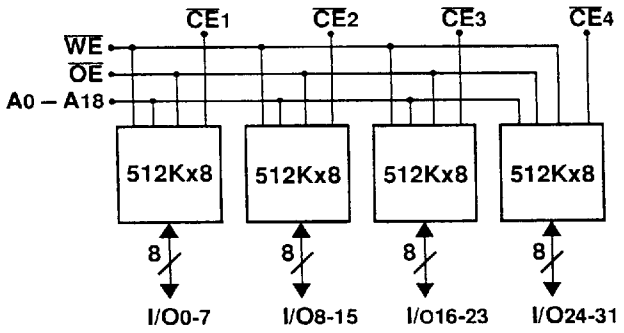
### Block Diagram – PGA Type Package(P1) & CQFP(F2)




Pin Description

| | |
|---|---|
| I/O0-31 | Data I/O |
| A0–18 | Address Inputs |
| $\overline{WE}$1–4 | Write Enables |
| $\overline{CE}$1–4 | Chip Enables |
| $\overline{OE}$ | Output Enable |
| Vcc | Power Supply |
| GND | Ground |
| NC | Not Connected |

### Block Diagram – CQFP(F1)




Pin Description

| | |
|---|---|
| I/O0-31 | Data I/O |
| A0–18 | Address Inputs |
| WE | Write Enable |
| $\overline{CE}$1–4 | Chip Enables |
| $\overline{OE}$ | Output Enable |
| Vcc | Power Supply |
| GND | Ground |
| NC | Not Connected |

## Absolute Maximum Ratings

| Symbol | Rating | | Range | Units |
|---|---|---|---|---|
| $T_A$ | Operating Temperature | Dash # -017 | -40 to +85 | °C |
| | | Dash # -020 to -055 | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | | -65 to +150 | °C |
| $P_D$ | Maximum Package Power Dissipation | | 3.0 | W |
| $Ø_{J-C}$ | Hottest Die, Max Thermal Resistance - Junction to Case | | 5 | °C/W |
| $V_G$ | Maximum Signal Voltage to Ground | | -0.5 to +7 | V |
| $T_L$ | Maximum Lead Temperature (10 seconds) | | 300 | °C |

## Normal Operating Conditions

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | +4.5 | +5.5 | V |
| $V_{IH}$ | Input High Voltage | +2.2 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.5 | +0.8 | V |

## Capacitance

($V_{IN}/V_{OUT}$ = 0V, f = 1MHz, $T_A$ = 25°C)

| Symbol | Parameter | Maximum | Units |
|---|---|---|---|
| $C_{AD}$ | $A_0 - A_{18}$ Capacitance | 50 | pF |
| $C_{OE}$ | $\overline{OE}$ Capacitance | 50 | pF |
| $C_{WE}$ | Write Enable Capacitance | | |
| | CQFP(F1) Package | 50 | pF |
| | PGA(P1) and CQFP(F2) Packages | 20 | pF |
| $C_{CE}$ | Chip Enable Capacitance | 20 | pF |
| $C_{I/O}$ | $I/O_0 - I/O_{31}$ Capacitance | 20 | pF |

This parameter is guaranteed by design but not tested

## DC Characteristics

($V_{CC}$ = 5.0V, $V_{SS}$= 0V, $T_A$= -55°C to +125°C; -017 version $T_A$= -40°C to +85°C)

| Parameter | Sym | Conditions | ALL Speeds Min | ALL Speeds Max | Units |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{CC}$ = +5.5V, $V_{IN}$ = 0 or $V_{CC}$ | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = 0 to $V_{CC}$ | | 10 | µA |
| Operating Supply Current 32 Bit Mode | $I_{CC1}$x32 | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, $V_{CC}$ = +5.5V<br>f = 5 MHz CMOS Compatible | | 400 | mA |
| Standby Current | $I_{SB1}$ | $\overline{CE}$ = $V_{CC}$, $\overline{OE}$ = $V_{IH}$, $V_{CC}$ = +5.5V<br>f = 5 MHz CMOS Compatible | | 80 | mA |
| Operating Supply Current 32 Bit Mode | $I_{CC2}$x32 | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, $V_{CC}$ = +5.5V<br>f = 50 MHz TTL Compatible | | 750 | mA |
| Standby Current | $I_{SB2}$ | $\overline{CE}$ = $V_{CC}$, $\overline{OE}$ = $V_{IH}$, $V_{CC}$ = +5.5V<br>f = 50 MHz TTL Compatible | | 240 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8 mA, $V_{CC}$ = +4.5V | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0 mA, $V_{CC}$ = +4.5V | 2.4 | | V |

## AC Characteristics
(VCC = 5.0V, VSS= 0V, TA= -55°C to +125°C)

### Read Cycle

| Parameter | Sym | -017 | | -020 | | -025 | | -035 | | -045 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 17 | | 20 | | 25 | | 35 | | 45 | | nS |
| Address Access Time | $t_{AA}$ | | 17 | | 20 | | 25 | | 35 | | 45 | nS |
| Chip Enable Access Time | $t_{ACS}$ | | 17 | | 20 | | 25 | | 35 | | 45 | nS |
| Output Hold from Address Change | $t_{OH}$ | 4 | | 4 | | 5 | | 5 | | 5 | | nS |
| Output Enable to Output Valid | $t_{OE}$ | | 9 | | 10 | | 12 | | 25 | | 35 | nS |
| Chip Enable to Output in Low Z * | $t_{CLZ}$ | 3 | | 3 | | 3 | | 3 | | 3 | | nS |
| Output Enable to Output in Low Z * | $t_{OLZ}$ | 0 | | 0 | | 0 | | 0 | | 0 | | nS |
| Chip Deselect to Output in High Z * | $t_{CHZ}$ | | 8 | | 8 | | 10 | | 15 | | 15 | nS |
| Output Disable to Output in High Z * | $t_{OHZ}$ | | 8 | | 8 | | 10 | | 15 | | 15 | nS |

* Parameters guaranteed by design but not tested

### Write Cycle

| Parameter | Sym | -017 | | -020 | | -025 | | -035 | | -045 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 17 | | 20 | | 25 | | 35 | | 45 | | nS |
| Chip Enable to End of Write | $t_{CW}$ | 15 | | 15 | | 20 | | 30 | | 35 | | nS |
| Address Valid to End of Write | $t_{AW}$ | 15 | | 15 | | 20 | | 30 | | 35 | | nS |
| Data Valid to End of Write | $t_{DW}$ | 12 | | 12 | | 15 | | 20 | | 30 | | nS |
| Write Pulse Width | $t_{WP}$ | 13 | | 13 | | 15 | | 25 | | 35 | | nS |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | 0 | | nS |
| Output Active from End of Write * | $t_{OW}$ | 0 | | 0 | | 0 | | 0 | | 0 | | nS |
| Write to Output in High Z * | $t_{WHZ}$ | | 8 | | 11 | | 13 | | 15 | | 15 | nS |
| Data Hold from Write Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | nS |
| Address Hold Time | $t_{AH}$ | 0 | | 1 | | 2 | | 2 | | 2 | | nS |

* Parameters guaranteed by design but not tested

## Data Retention Electrical Characteristics (Special Order Only)
(TA = -55°C to +125°C)

| Parameter | Sym | Test Conditions | All Speeds | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{CC}$ for Data Retention | $V_{DR}$ | $\overline{CE} \geq V_{CC} - 0.2V$ | 2 | 5.5 | V |
| Data Retention Current | $I_{CCDR1}$ | $V_{CC}$ = 3V | | 8.5 | mA |

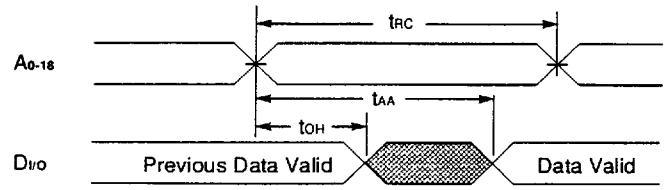
## Truth Table

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | Data I/O | Power |
|---|---|---|---|---|---|
| Standby | H | X | X | High Z | Standby (deselect/power down) |
| Read | L | L | H | Data Out | Active |
| Read | L | H | H | High Z | Active (deselected) |
| Write | L | X | L | Data In | Active |

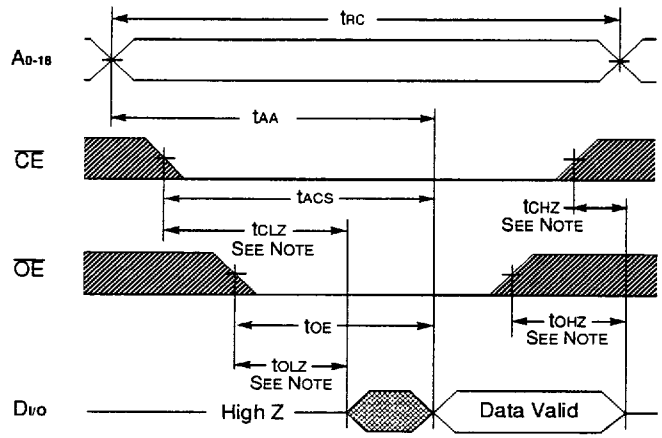
# Timing Diagrams

## Read Cycle Timing Diagrams

### Read Cycle 1 ($\overline{CE}$ = $\overline{OE}$ = VIL, $\overline{WE}$ = VIH)




### Read Cycle 2 ($\overline{WE}$ = VIH)

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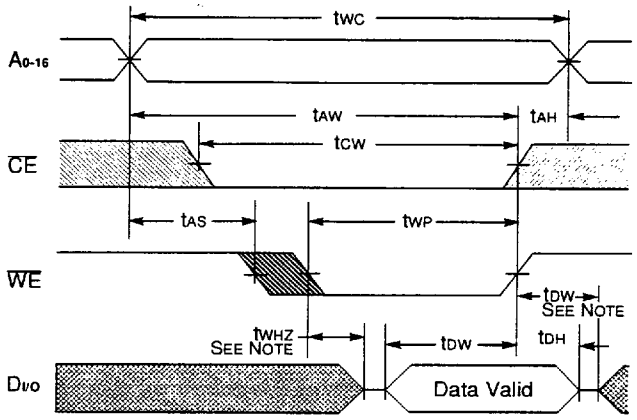
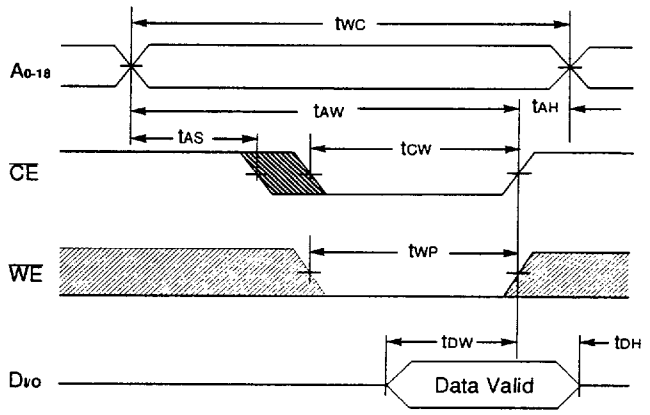
## Write Cycle Timing Diagrams

### Write Cycle 1 ($\overline{WE}$ Controlled, $\overline{OE}$ = VIL)

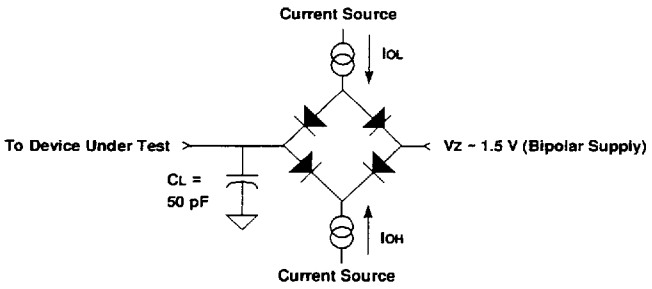



### Write Cycle 2 ($\overline{CE}$ Controlled, $\overline{OE}$ = VIH )




Note: Guaranteed by design, but not tested.

### AC Test Circuit



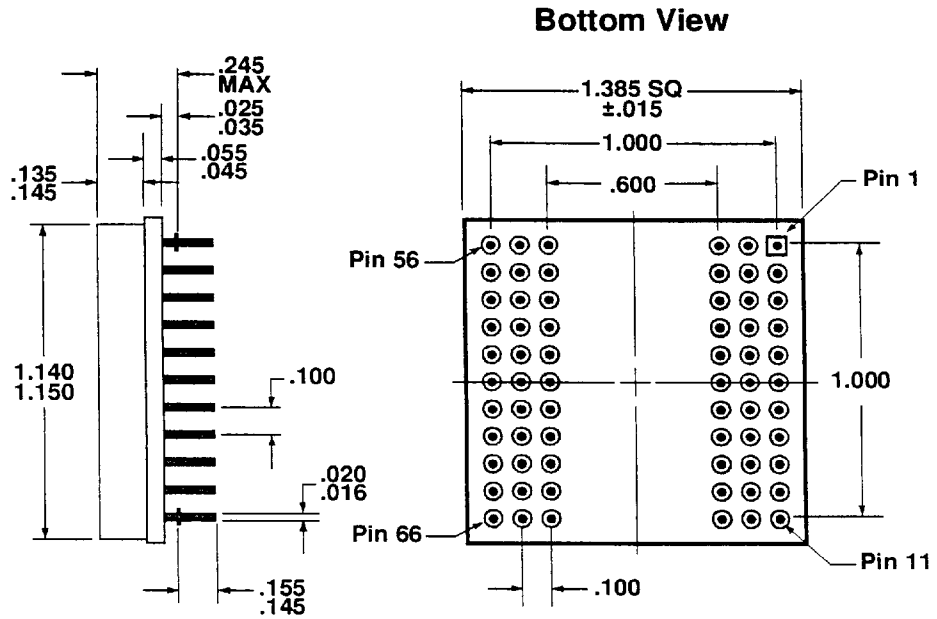

| Parameter | Typical | Units |
|---|---|---|
| Input Pulse Level | 0 – 3.0 | V |
| Input Rise and Fall | 5 | nS |
| Input and Output Timing Reference Level | 1.5 | V |
| Output Lead Capacitance | 50 | pF |
| Vcc | 4.5 – 5.5 | V |
| GND | | Ground |
| NC | | Not Connected |

Notes:
1) VZ is programmable from -2V to +7V. 2) IOL and IOH programmable from 0 to 16 mA. 3) Tester Impedance ZO = 75Ω. 4) VZ is typically the midpoint of VOH and VOL. 5) IOL and IOH are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

## Pin Numbers & Functions

| 66 Pins — PGA-Type | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin # | Function | Pin # | Function | Pin # | Function | Pin # | Function |
| 1 | I/O8 | 18 | A12 | 35 | I/O25 | 52 | $\overline{WE3}$ |
| 2 | I/O9 | 19 | Vcc | 36 | I/O26 | 53 | $\overline{CS3}$ |
| 3 | I/O10 | 20 | $\overline{CS1}$ | 37 | A6 | 54 | GND |
| 4 | A13 | 21 | NC | 38 | A7 | 55 | I/O19 |
| 5 | A14 | 22 | I/O3 | 39 | NC | 56 | I/O31 |
| 6 | A15 | 23 | I/O15 | 40 | A8 | 57 | I/O30 |
| 7 | A16 | 24 | I/O14 | 41 | A9 | 58 | I/O29 |
| 8 | A17 | 25 | I/O13 | 42 | I/O16 | 59 | I/O28 |
| 9 | I/O0 | 26 | I/O12 | 43 | I/O17 | 60 | A0 |
| 10 | I/O1 | 27 | $\overline{OE}$ | 44 | I/O18 | 61 | A1 |
| 11 | I/O2 | 28 | A18 | 45 | Vcc | 62 | A2 |
| 12 | $\overline{WE2}$ | 29 | $\overline{WE1}$ | 46 | $\overline{CS4}$ | 63 | I/O23 |
| 13 | $\overline{CS2}$ | 30 | I/O7 | 47 | $\overline{WE4}$ | 64 | I/O22 |
| 14 | GND | 31 | I/O6 | 48 | I/O27 | 65 | I/O21 |
| 15 | I/O11 | 32 | I/O5 | 49 | A3 | 66 | I/O20 |
| 16 | A10 | 33 | I/O4 | 50 | A4 | | |
| 17 | A11 | 34 | I/O24 | 51 | A5 | | |

## Package Outline — PGA-Type "P1"

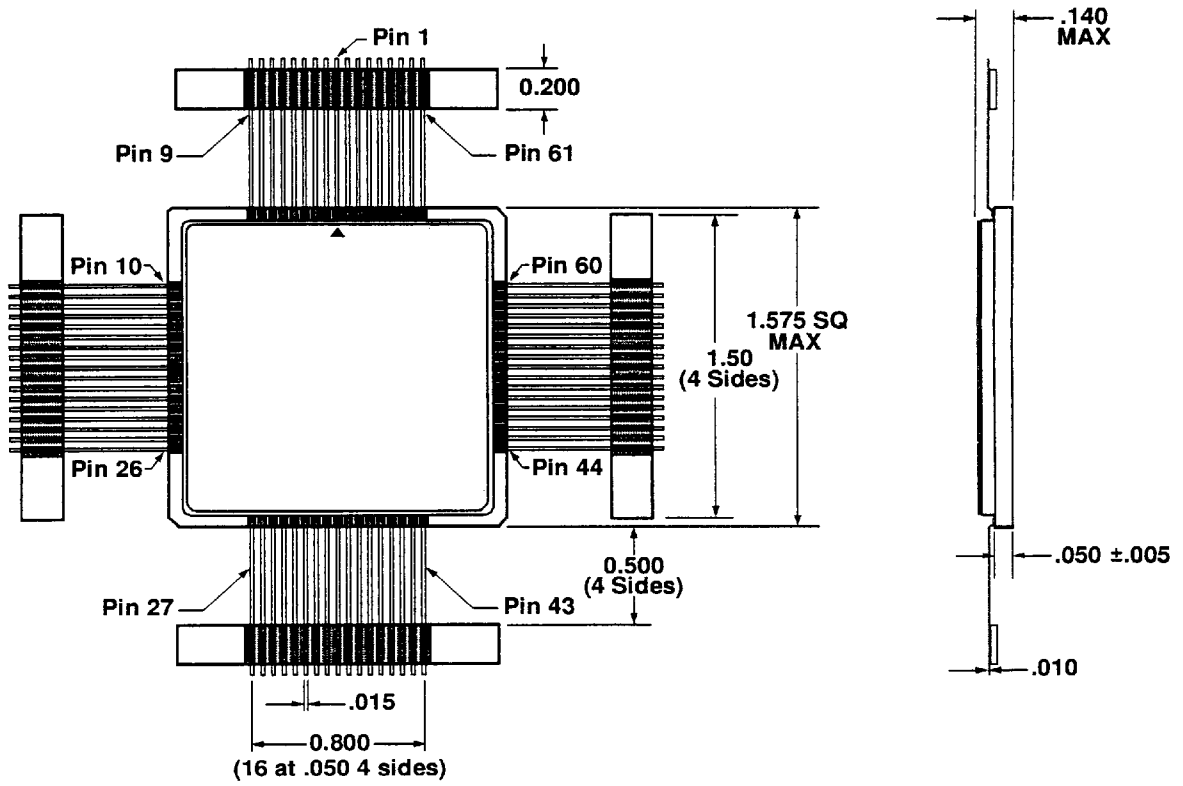



All dimensions in inches

## Pin Numbers & Functions

| 68 Pins — CQFP | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin # | Function | Pin # | Function | Pin # | Function | Pin # | Function |
| 1 | GND | 18 | GND | 35 | $\overline{OE}$ | 52 | GND |
| 2 | $\overline{CS_1}$ | 19 | I/O8 | 36 | $\overline{CS_4}$ | 53 | I/O23 |
| 3 | A5 | 20 | I/O9 | 37 | A17 | 54 | I/O22 |
| 4 | A4 | 21 | I/O10 | 38 | A18 | 55 | I/O21 |
| 5 | A3 | 22 | I/O11 | 39 | NC | 56 | I/O20 |
| 6 | A2 | 23 | I/O12 | 40 | NC | 57 | I/O19 |
| 7 | A1 | 24 | I/O13 | 41 | NC | 58 | I/O18 |
| 8 | A0 | 25 | I/O14 | 42 | NC | 59 | I/O17 |
| 9 | NC | 26 | I/O15 | 43 | NC | 60 | I/O16 |
| 10 | I/O0 | 27 | Vcc | 44 | I/O31 | 61 | Vcc |
| 11 | I/O1 | 28 | A11 | 45 | I/O30 | 62 | A10 |
| 12 | I/O2 | 29 | A12 | 46 | I/O29 | 63 | A9 |
| 13 | I/O3 | 30 | A13 | 47 | I/O28 | 64 | A8 |
| 14 | I/O4 | 31 | A14 | 48 | I/O27 | 65 | A7 |
| 15 | I/O5 | 32 | A15 | 49 | I/O26 | 66 | A6 |
| 16 | I/O6 | 33 | A16 | 50 | I/O25 | 67 | $\overline{WE}$ |
| 17 | I/O7 | 34 | $\overline{CS_2}$ | 51 | I/O24 | 68 | $\overline{CS_3}$ |

## Package Outline — CQFP "F1"



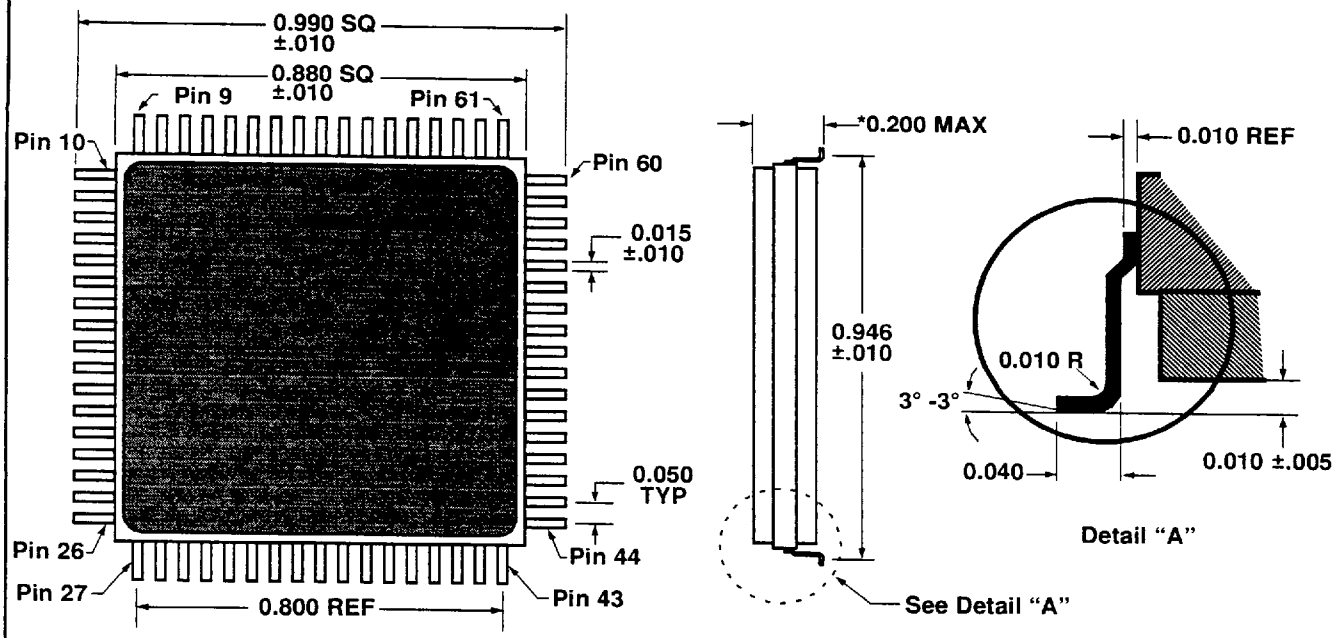

All dimensions in inches

## Pin Numbers & Functions

| 68 Pins — Dual-Cavity CQFP | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin # | Function | Pin # | Function | Pin # | Function | Pin # | Function |
| 1 | GND | 18 | GND | 35 | $\overline{OE}$ | 52 | GND |
| 2 | $\overline{CE_3}$ | 19 | $I/O_8$ | 36 | $\overline{CE_2}$ | 53 | $I/O_{23}$ |
| 3 | $A_5$ | 20 | $I/O_9$ | 37 | $A_{17}$ | 54 | $I/O_{22}$ |
| 4 | $A_4$ | 21 | $I/O_{10}$ | 38 | $\overline{WE_2}$ | 55 | $I/O_{21}$ |
| 5 | $A_3$ | 22 | $I/O_{11}$ | 39 | $\overline{WE_3}$ | 56 | $I/O_{20}$ |
| 6 | $A_2$ | 23 | $I/O_{12}$ | 40 | $\overline{WE_4}$ | 57 | $I/O_{19}$ |
| 7 | $A_1$ | 24 | $I/O_{13}$ | 41 | $A_{18}$ | 58 | $I/O_{18}$ |
| 8 | $A_0$ | 25 | $I/O_{14}$ | 42 | NC | 59 | $I/O_{17}$ |
| 9 | NC | 26 | $I/O_{15}$ | 43 | NC | 60 | $I/O_{16}$ |
| 10 | $I/O_0$ | 27 | $V_{CC}$ | 44 | $I/O_{31}$ | 61 | $V_{CC}$ |
| 11 | $I/O_1$ | 28 | $A_{11}$ | 45 | $I/O_{30}$ | 62 | $A_{10}$ |
| 12 | $I/O_2$ | 29 | $A_{12}$ | 46 | $I/O_{29}$ | 63 | $A_9$ |
| 13 | $I/O_3$ | 30 | $A_{13}$ | 47 | $I/O_{28}$ | 64 | $A_8$ |
| 14 | $I/O_4$ | 31 | $A_{14}$ | 48 | $I/O_{27}$ | 65 | $A_7$ |
| 15 | $I/O_5$ | 32 | $A_{15}$ | 49 | $I/O_{26}$ | 66 | $A_6$ |
| 16 | $I/O_6$ | 33 | $A_{16}$ | 50 | $I/O_{25}$ | 67 | $\overline{WE_1}$ |
| 17 | $I/O_7$ | 34 | $\overline{CE_1}$ | 51 | $I/O_{24}$ | 68 | $\overline{CE_4}$ |

## Package Outline — Dual-Cavity CQFP "F2"

### Top View




*0.180 MAX available, call factory for details

All dimensions in inches

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## Ordering Information

| Model Number | DESC Part Number | Speed | Package |
|---|---|---|---|
| ACT–S512K32N–017F1Q | 5962–9562410HXX(Pending) | 17nS | 1.56"sq CQFP |
| ACT–S512K32N–020F1Q | 5962–9562409HYC | 20nS | 1.56"sq CQFP |
| ACT–S512K32N–025F1Q | 5962–9562408HYC | 25nS | 1.56"sq CQFP |
| ACT–S512K32N–034F1Q | 5962–9562407HYC | 35nS | 1.56"sq CQFP |
| ACT–S512K32N–045F1Q | 5962–9562406HYC | 45nS | 1.56"sq CQFP |
| ACT–S512K32N–055F1Q | 5962–9562405HYC | 55nS | 1.56"sq CQFP |
| ACT–S512K32N–017F2Q | 5962–9461110HMC(Pending) | 17nS | .88"sq CQFP |
| ACT–S512K32N–020F2Q | 5962–9461109HMC | 20nS | .88"sq CQFP |
| ACT–S512K32N–025F2Q | 5962–9461108HMC | 25nS | .88"sq CQFP |
| ACT–S512K32N–035F2Q | 5962–9461107HMC | 35nS | .88"sq CQFP |
| ACT–S512K32N–045F2Q | 5962–9461106HMC | 45nS | .88"sq CQFP |
| ACT–S512K32N–055F2Q | 5962–9461105HMC | 55nS | .88"sq CQFP |
| ACT–S512K32N–017P1Q | 5962–9461110HXC(Pending) | 17nS | 1.38"sq PGA-Type |
| ACT–S512K32N–020P1Q | 5962–9461109HXC | 20nS | 1.38"sq PGA-Type |
| ACT–S512K32N–025P1Q | 5962–9461108HXC | 25nS | 1.38"sq PGA-Type |
| ACT–S512K32N–035P1Q | 5962–9461107HXC | 35nS | 1.38"sq PGA-Type |
| ACT–S512K32N–045P1Q | 5962–9461106HXC | 45nS | 1.38"sq PGA-Type |
| ACT–S512K32N–055P1Q | 5962–9461105HXC | 55nS | 1.38"sq PGA-Type |

## Model Number Breakdown

**ACT– S 512K 32 N– 020 F1 M**

**Aeroflex Circuit Technology**

***Memory Type***
- S = SRAM
- F = FLASH EEPROM
- E = EEPROM
- D = Dynamic RAM

***Memory Depth, Bits***

***Memory Width, Bits***

***Pinout Options***
- N = X

***Memory Speed, ns***

***Screening***
- C = Commercial Temp, 0°C to +70°C, No 883 Screening
- I = Industrial Temp, -40°C to +85°C, No 883 Screening
- T = Military Temp, -55°C to +125°C, No 883 Screening
- M = Military Temp, -55°C to +125°C, 883 Screening
- Q = MIL-STD-883 Compliant

***Package Type & Size***

***Surface Mount Packages***
- F1 = 1.56"SQ 68 Pin CQFP
- F2 = .88"SQ 68 Pin Dual-Cavity CQFP

***Thru-Hole Packages***
- P1 = 1.385"SQ PGA 66 Pins

Specification subject to change without notice

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