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SILICON SYSTEMS INC

SSI 73Q8360
Ethernet Controller/
ENDEC Combo

Preliminary Data

January 1993

DESCRIPTION

The SSI 78Q8360 is a combination Media Access Controller (MAC) and 10 Mbit/s Manchester encoder/decoder (ENDEC) with Attachment Unit Interface (AUI) for IEEE 802.3 applications. It is connected to the transmission medium through the AUI with a transceiver circuit such as the SSI 78Q8330 Ethernet Coax Transceiver or the 78Q902 10BaseT Transceiver. Connection to the host is accomplished via external bus decoding logic.

An intelligent Buffer Manager is controlled by the host read, host write, receive and transmit pointers, and the 8360 manages the pointers internally without any host intervention. The 8360 interleaves access to the buffer memory so that accesses from the host and from the network media seem to operate concurrently.

The 8360 has a sophisticated power management capability with three different operating modes allowing the user to maximize power savings. Interface with the host can be accomplished in several different ways: memory mapping, I/O mapping, programmable DMA or a combination of these. Big and little endian byte orderings make for simple bus interface to all standard microprocessors. The 78Q8360 is packaged in a 100-pin QFP or TQFP and uses a single 5V supply.

FEATURES

- **IEEE 802.3 and Ethernet 2.0 compliant**
- **Power management options include:**
  - **Intelligent power mode automatically shuts off unused circuitry**
  - **Standby mode reduces power while not in operation**
  - **Full power-down mode offers maximum power savings**
- **Advanced Buffer Manager architecture:**
  - **Automatic management of all pointers**
  - **Allows "simultaneous" access to data in buffer memory by both the network and host**
  - **High-speed received packet skip**
- **Configurable Buffer Memory for design flexibility:**
  - **Two-bank transmit buffer in 2, 4, 8, or 16 Kbyte sizes**
  - **Ring-structure receive buffer from 4 to 62 Kbytes**

(continued)

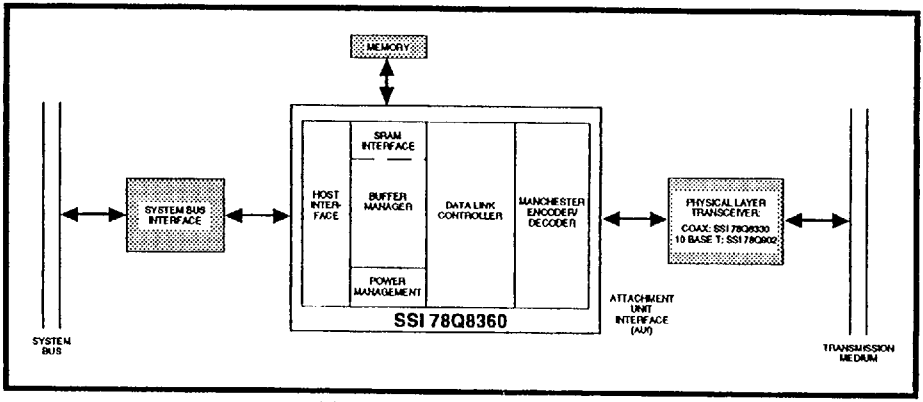

FIGURE 1: System Diagram

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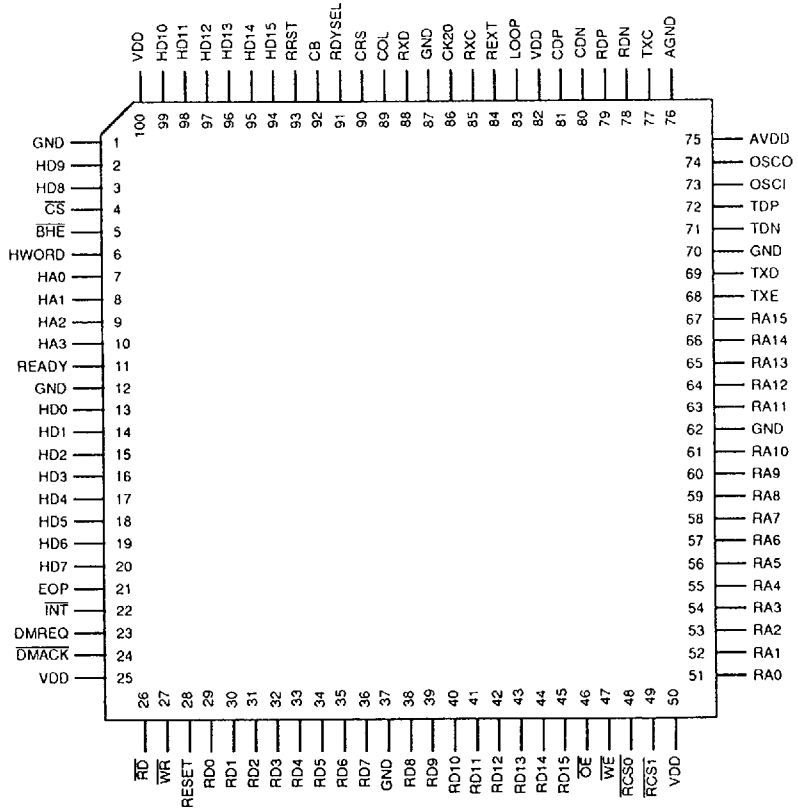
Note:
This is an abbreviated version of the actual data sheet. Please contact your local Silicon Systems' sales office or Silicon Systems' headquarters in Tustin for a complete, current data sheet.

FEATURES (continued)

- Software-configurable system bus structure:
  - Compatible with major microprocessors
  - 8- or 16-bit wide data path
  - Supports single and programmable burst DMA, I/O and interrupt operations
- Three different loopback modes
- Multicast address filtering via 64-element hash table



100-Lead TQFP

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