



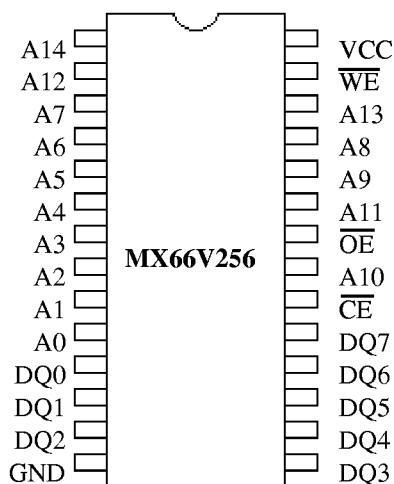
MX66V256

Super Low Power 32k x 8 CMOS SRAM

FEATURES

- ❑ Wide supply voltage range
 - CMOS Input level (0.8V_{cc}/0.2V_{cc})
5.5V to 2V
 - TTL Input level (3V/0V)
4.5V to 2V
- ❑ Super low power consumption
 - 5V operation
 - 60mA (Max.) write current
 - 20mA (Max.) read current
 - 2uA (Typ.) CMOS standby current
 - 3V operation
 - 30mA (Max.) write current
 - 10mA (Max.) read current
 - 0.3uA (Typ.) CMOS standby current
- ❑ High speed access time
 - 5V/3.3V operation
70ns /100ns (Max.)
 - 2.2V operation
200ns (Max.)
- ❑ Automatic power down when chip is deselected
- ❑ All inputs and outputs are TTL-compatible
- ❑ Complies to JEDEC low-voltage TTL standard
- ❑ Three state outputs
- ❑ Fully static operation
- ❑ Data retention supply voltage as low as 1.5V
- ❑ Easy expansion with $\overline{CE}$ and $\overline{OE}$ options
- ❑ All I/O pins are 5V tolerant in 3V/2V operation

PIN CONFIGURATIONS (SOP/DIP)



DESCRIPTION

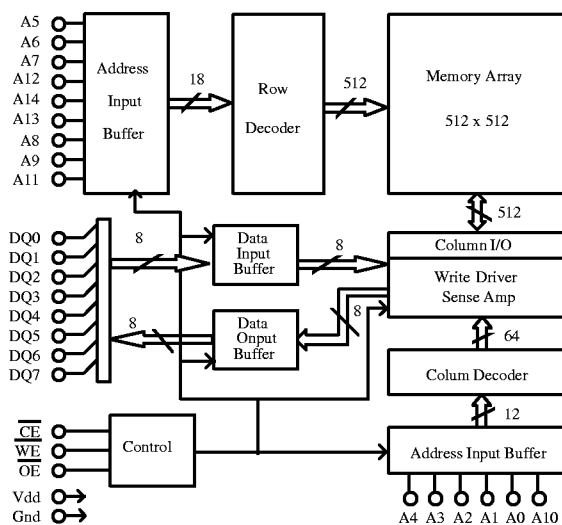
The MX66V256 is a high performance, low power CMOS Static Random Access Memory organized as 32,768 words by 8 bits and operates from a wide range of supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.3uA and maximum access time of 70ns/100ns in 3V operation. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state output drivers.

The MX66V256 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The MX66V256 is available in the JEDEC standard 28 pin 600mil/300mil Plastic DIP, 330mil Plastic SOP, and 8mmx13.4mm TSOP (normal type).

BLOCK DIAGRAM





PIN DESCRIPTIONS

A₀-A₁₄ Address Input

These 15 address input select one of the 32768 x 8-bit words in the RAM

$\overline{\text{CE}}$ Chip Enable Input

$\overline{\text{CE}}$ is active LOW . Chip enable must be active to read from or write to the device. if chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.

$\overline{\text{WE}}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{\text{WE}}$ is HIGH and $\overline{\text{OE}}$ is LOW, output data will be present on the DQ pins; when $\overline{\text{WE}}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

$\overline{\text{OE}}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{\text{OE}}$ is inactive.

DQ₀ - DQ₇ Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{cc}

Power Supply

GND

Ground

TRUTH TABLE

MODE	$\overline{\text{WE}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	I/O Operation	V _{cc} Current
Not Selected	X	H	X	High Z	I _{CCSB} , I _{CCSB1}
Output Disabled	H	L	H	High Z	I _{cc}
Read	H	L	L	D _{OUT}	I _{cc}
Write	L	L	X	D _{IN}	I _{cc}

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	PARAMETER	RATING	UNITS
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-10 to +125	°C
T _{STG}	Storage Temperature	-60 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V _{cc}
INDUSTRIAL	-10° C to + 70° C	2V to 5.5V

CAPACITANCE⁽¹⁾ (T_A = 25° C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{DQ}	Input/Output Capacitance	V _{IO} = 0V	8	pF

1. This parameter is guaranteed and not tested.



DC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNITS
V _{IL}	Guaranteed Input Low Voltage ⁽²⁾		-0.5	—	+0.8	V
V _{IH}	Guaranteed Input High Voltage ⁽²⁾		2.0	3.3	5.5	V
I _{IL}	Input Leakage Current	V _{CC} = Max, V _{IN} = 0V to V _{CC}	—	—	1	uA
I _{OL}	Output Leakage Current	V _{CC} = Max, $\overline{CE}$ = V _{IH} , or $\overline{OE}$ = V _{IH} , V _{IO} = 0V to V _{CC}	—	—	1	uA
V _{OL}	Output Low Voltage	V _{CC} = Max, I _{OL} = 4mA	—	—	0.4	V
V _{OH}	Output High Voltage	V _{CC} = Min, I _{OH} = -1mA	2.4	—	—	V
I _{CC}	Operating Power Supply Current	V _{CC} = Max, $\overline{CE}$ = V _{IL} , I _{DQ} = 0mA, F = F _{max} ⁽³⁾	—	20	30	mA
I _{CCSB}	Standby Power Supply Current	V _{CC} = Max, $\overline{CE}$ = V _{IH} , I _{DQ} = 0mA,	—	—	1	mA
I _{CCSDI}	Power Down Supply Current	V _{CC} = Max, $\overline{CE}$ ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≥ 0.2V	—	0.3	3	uA

1. Typical characteristics are at V_{CC} = 3.3V, T_A = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3. F_{MAX} = 1/t_{RC}.

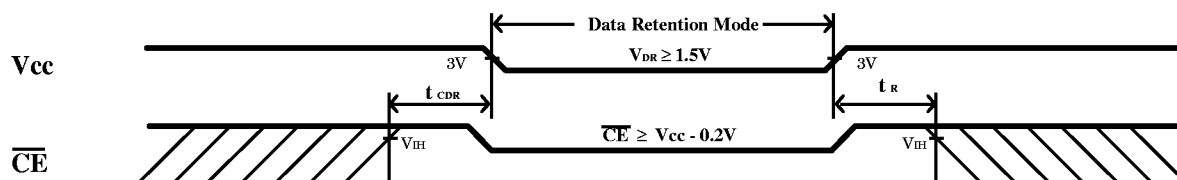
DATA RETENTION CHARACTERISTICS (T_A = -10°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNITS
V _{DR}	V _{CC} for Data Retention	$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	1.5	—	—	V
I _{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	0.1	1	uA
t _{CDR}	Chip Deselect to Data Retention Time	See Retention Wavform	0	—	—	ns
t _R	Operation Recovery Time		T _{RC} ⁽²⁾	—	—	ns

1. V_{CC} = 1.5V, T_A = +25°C

2. t_{RC} = Read Cycle Time

LOW VCC DATA RETENTION WAVEFORM⁽¹⁾ ($\overline{CE}$ Controlled)



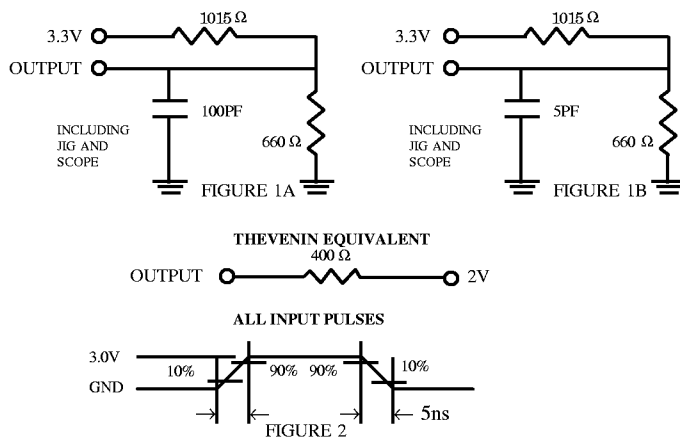


MX66V256

AC TEST CONDITIONS

Input Pulse Levels	0.8V _{cc} /0.2V _{cc} or 3V/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V

AC TEST LOADS AND WAVEFORMS



KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE i ^{OFF} i ^{STATE}

AC ELECTRICAL CHARACTERISTICS (over the operating range)

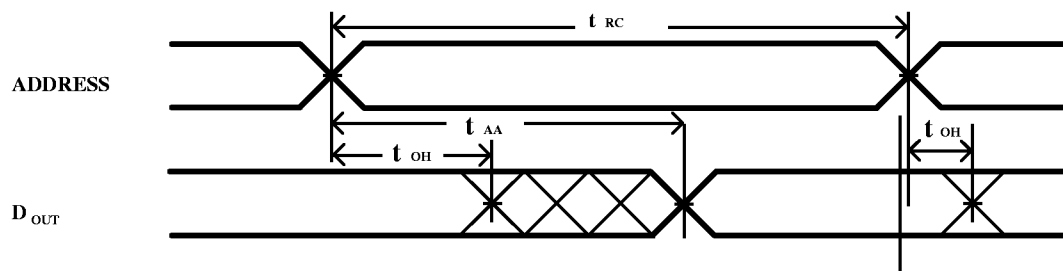
READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	70	—	—	ns
t_{AVQV}	t_{AA}	Address Access Time	—	—	70	ns
t_{ELQV}	t_{ACS}	Chip Select Access Time	—	—	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	—	—	50	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z	10	—	—	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	10	—	—	ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	0	—	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	—	30	ns
t_{AXQX}	t_{OH}	Output Disable to Output Address Change	10	—	—	ns

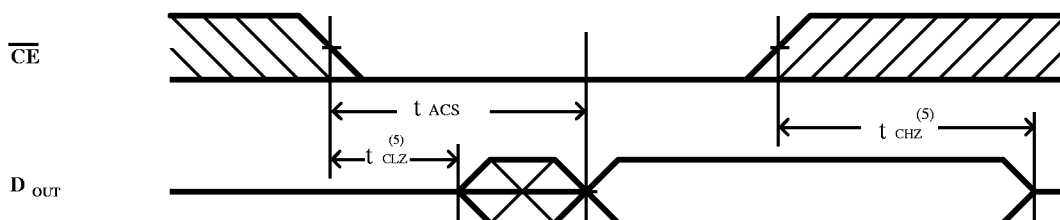
1. Typical characteristics are at V_{cc} = 3.3V, T_A = 25°C.

SWITCHING WAVEFORMS (READ CYCLE)

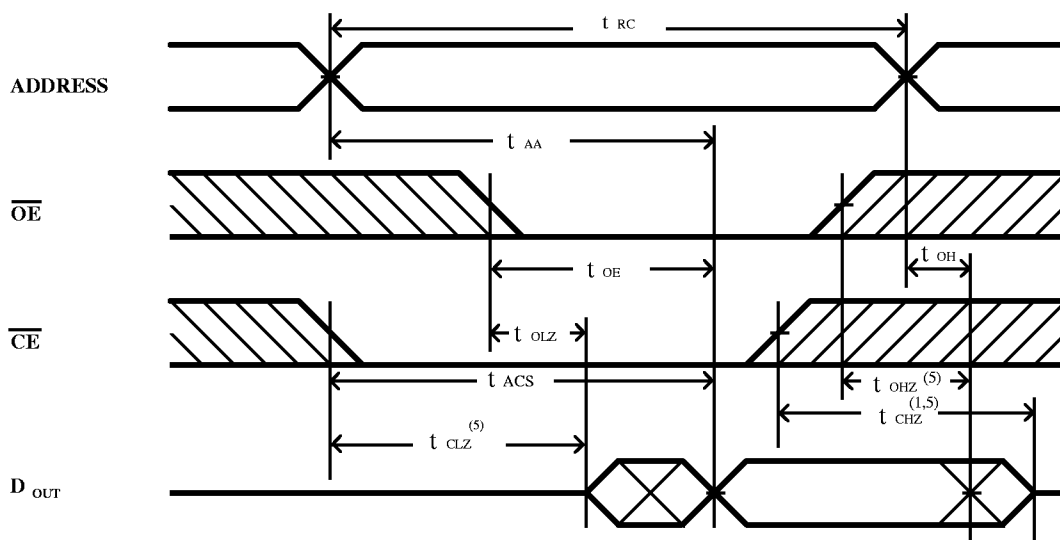
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:

1. $\overline{WE}$ is high for read Cycle.
2. Device is continuously selected when $\overline{CE} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.



AC ELECTRICAL CHARACTERISTICS (over the operating range)

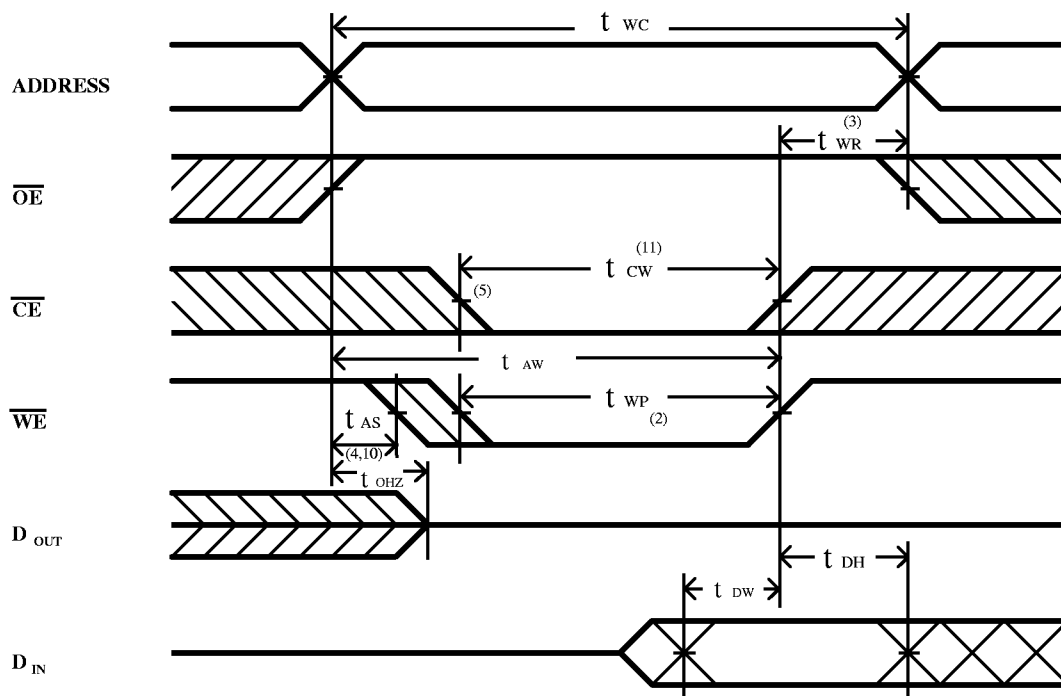
WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	MX66V256-70 MIN. TYP. MAX.			UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	70	—	—	ns
t_{EILWH}	t_{CW}	Chip Select to End of Write	70	—	—	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	—	—	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	70	—	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	—	—	ns
t_{WHAX}	t_{WR}	Write Recovery Time ($\overline{CE}$, $\overline{WE}$)	0	—	—	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	—	—	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	40	—	—	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	—	—	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	—	30	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	—	—	ns

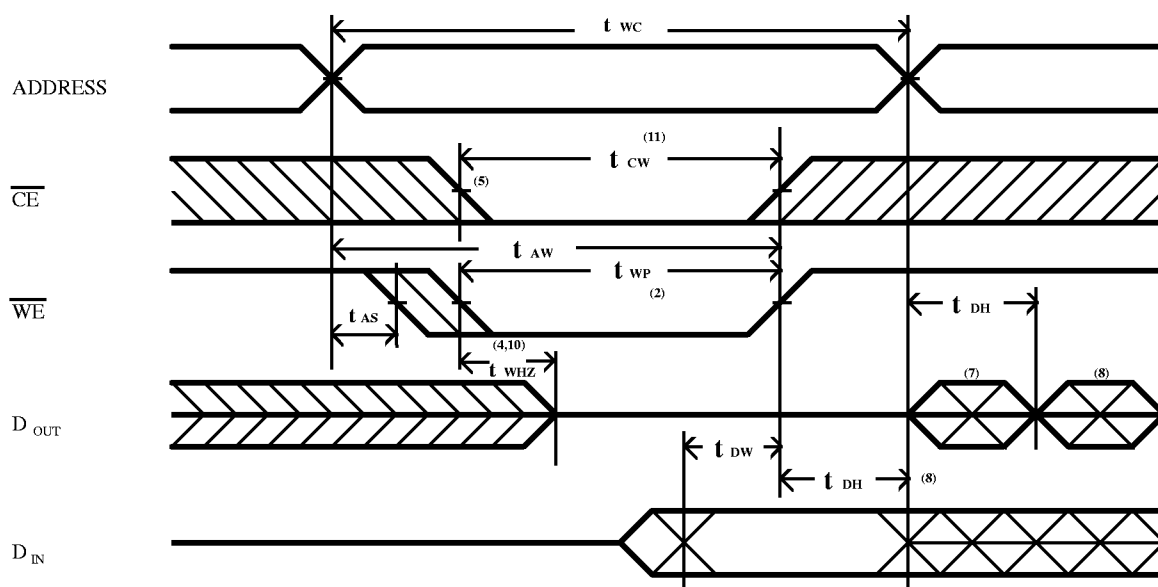
1. Typical characteristics are at $V_{CC} = 3.3V$, $T_A = 25^\circ C$.

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1⁽¹⁾



WRITE CYCLE^(1,6)



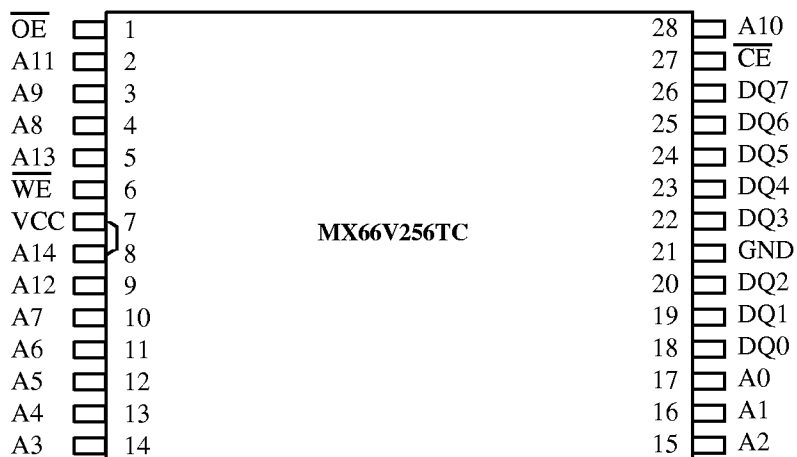
NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm 500mV$ from steady state with $C_L = 5pF$ as shown in Figure 1b. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.



PIN CONFIGURATIONS (cont.)

28-Pin Plastic TSOP (Normal Pinouts)



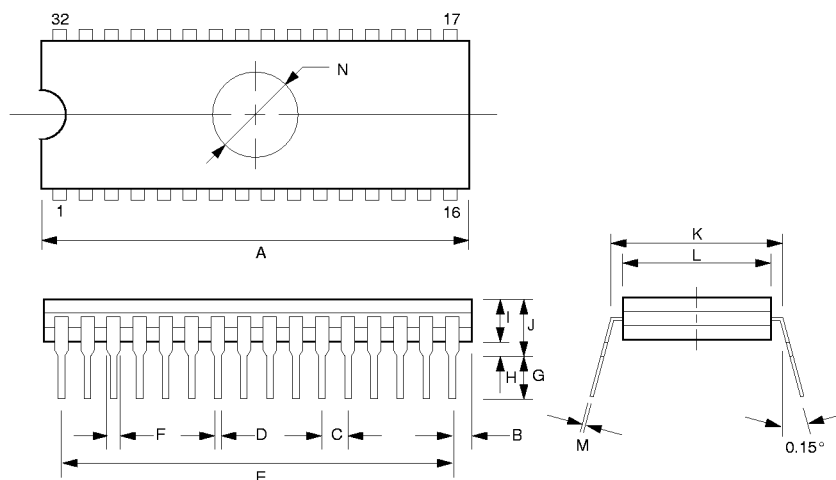
Suffix-TC in the package identifier

PACKAGE INFORMATION

32-PIN CERDIP(MSI) WITH WINDOW (600mil)

ITEM	MILLIMETERS	INCHES
A	42.26 max	1.665 max
B	1.90 ± .38	.075 ± .015
C	2.54 [TP]	.100 [TP]
D	.46 [REF]	.018 [REF]
E	38.07	1.500
F	1.42 [REF]	.056 [REF]
G	3.43 ± .38	.135 ± .015
H	.96 ± .43	.038 ± .017
I	4.06	.160
J	5.00	.203
K	15.58 ± .13	.614 ± .005
L	13.20 ± .38	.520 ± .015
M	.25 [REF]	.010 [REF]
N	ø8.12	ø.320

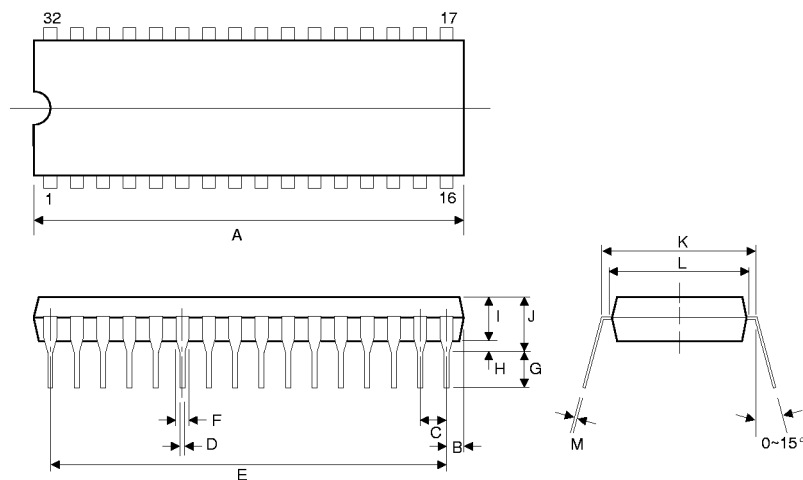
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



32-PIN PLASTIC DIP(600 mil)

ITEM	MILLIMETERS	INCHES
A	42.13 max.	1.660 max.
B	1.90 [REF]	.075 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	38.07	1.500
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97 ± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.

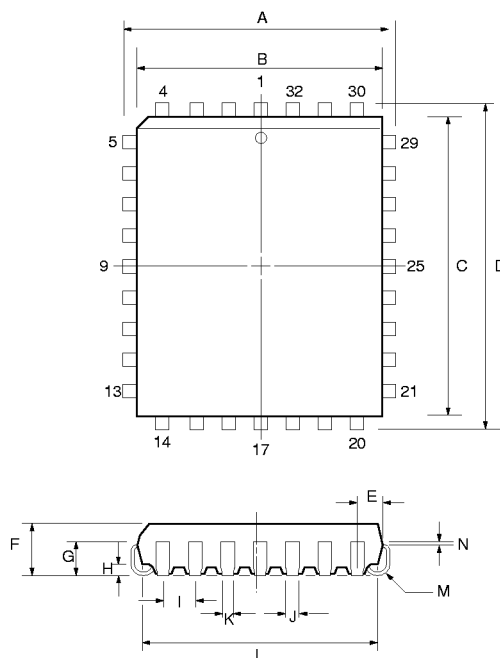


PACKAGE INFORMATION

32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	12.44 ± .13	.490 ± .005
B	11.50 ± .13	.453 ± .005
C	14.04 ± .13	.553 ± .005
D	14.98 ± .13	.590 ± .005
E	1.93	.076
F	3.30 ± .25	.130 ± .010
G	2.03 ± .13	.080 ± .005
H	.51 ± .13	.020 ± .005
I	1.27 [Typ.]	.050 [Typ.]
J	.71 [REF]	.028 [REF]
K	.46 [REF]	.018 [REF]
L	10.40/12.94 (W) (L)	.410/.510 (W) (L)
M	.89 R	.035 R
N	.25 (TYP.)	.010 (TYP.)

NOTE: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



28-PIN PLASTIC SOP(330 mil)

ITEM	MILLIMETERS	INCHES
A	18.11 max.	.713 max.
B	1.194 max	.047 max
C	1.27 [TP]	.050 [TP]
D	.41 [Typ.]	.016 [Typ.]
E	.10 min.	.004 min.
F	2.84 max.	.112 max.
G	2.49 ± .13	.098 ± .005
H	11.81 ± .31	.465 ± .012
I	8.41 ± .13	.331 ± .005
J	1.70 ± .20	.067 ± .008
K	.25 [Typ.]	.010 [Typ.]
L	.762	.03

NOTE: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.

