# SR002AN/D

# Linear Regulators with Microprocessor Control Functions

ON Semiconductor™

http://onsemi.com

APPLICATION NOTE

**Kieran O'Malley**
**ON Semiconductor**
**2000 South County Trail**
**East Greenwich, RI 02818**

Although microprocessors are often considered the "brains" of a control system, they need a well regulated power supply and constant supervision for consistent operation. The system designer must choose between building these supervisory functions using discrete circuitry, a microprocessor supervisory IC, or a regulator which has the supervisory functions included. This article examines each of the common supervisory functions required in a microprocessor control system and shows how they are integrated into a SMART REGULATOR® to provide a complete system solution.

## Introduction

ON Semiconductor SMART REGULATORs are linear regulators that provide a power supply and supervisory functions for microprocessor control systems. Along with the basic 5.0 V or 3.3 V supply, a microprocessor also requires circuitry to provide functions such as:

- Power on Reset
- Low Voltage Reset
- Watchdog Timer
- Wake–up Timer
- On–Off control or Enable

Several of the newer microprocessors have some of these functions already incorporated but most designers prefer that supervisory tasks are handled by an external device to provide an additional safety measure. (A microprocessor will not be able to detect its own errors, especially in low supply voltage situations.)

Microprocessor control functions can be implemented with individual discrete circuits, microprocessor supervisor IC's, or by using a SMART REGULATOR like those manufactured by ON Semiconductor . The advantage that a SMART REGULATOR offers is complete integration where all the functions are fully compatible with each other in a single space saving design.

## Power On Reset

When power is initially applied to a microprocessor, its internal registers contain random data. Applying a Reset to the microprocessor overcomes the potential for errors by resetting all internal circuitry to a predictable starting point. To ensure proper startup, the reset input of the microprocessor must be held low for a fixed amount of time. During this time the supply voltage reaches its nominal value and the oscillator frequency stabilizes. This power on reset period is usually specified by the microprocessor manufacturer as a number of clock cycles or a time period. The time period ranges from 20 to several hundred milliseconds depending on the microprocessor.

Reset circuitry is powered either directly from the regulator's input voltage, $V_{IN}$ or from its output voltage, $V_{OUT}$. If the reset circuitry is powered from $V_{IN}$, the Reset will not function when the input voltage disappears suddenly or drops out of regulation. However, the microprocessor may continue to work, powered by the output capacitor voltage. Without a valid Reset, the microprocessor may operate erroneously.

Because of this possibility, all ON Semiconductor SMART REGULATOR reset circuitry is powered from the regulator's output voltage, $V_{OUT}$, rather than its input voltage, $V_{IN}$. Reset will function for values of $V_{OUT}$ as low as 1.0 Volt.

## Delayed Reset

ON Semiconductor SMART REGULATORs have either a delayed Reset or a real time Reset. In a delayed reset circuit like the one in the CS8126, the user programs the time for which the reset output remains low with an external capacitor, $C_{DELAY}$. The CS8126 uses an internal current source to charge $C_{DELAY}$ when the output voltage is above a predetermined level ($V_{RT(ON)}$) as shown in Figure 1. The reset output is an open collector NPN transistor that requires a pull up resistor (Figure 2, $R_{RST}$) connected to $V_{OUT}$.

The reset delay time is calculated from the formula:

$$\text{DelayTime} = \frac{C_{DELAY} \times V_{CHARGE}(\text{Delay Threshold})}{I_{CHARGE}}$$

Using an ideal 0.1 μF capacitor, the delay time ranges from 22 ms to 65 ms due to regulator variation alone.

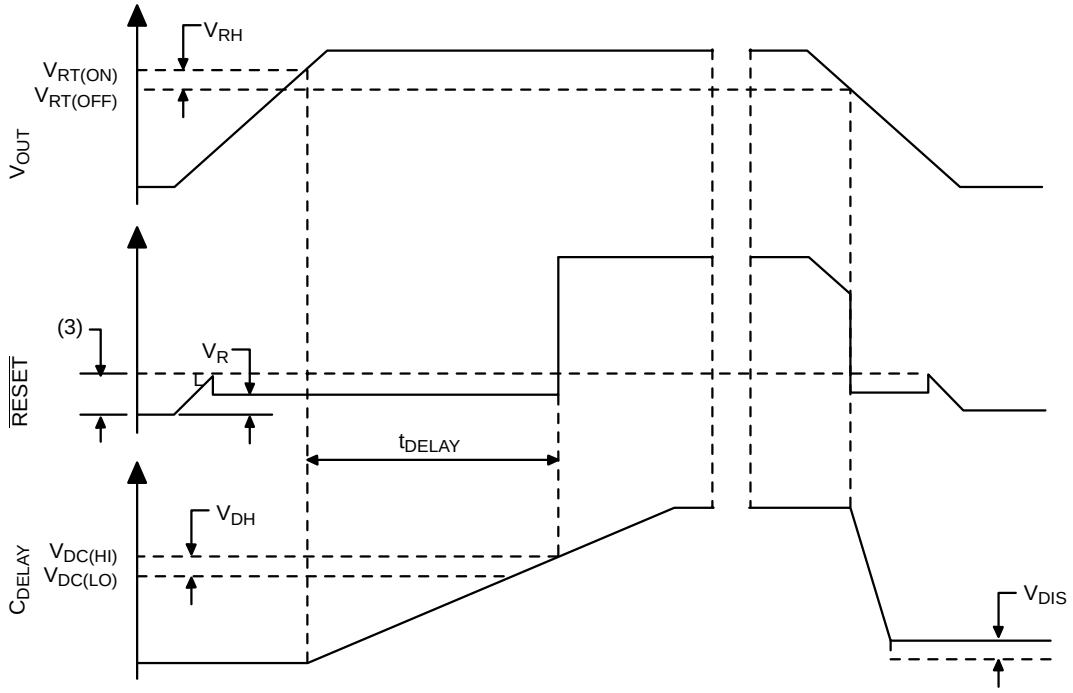



**Figure 1. Reset Waveforms: Output Voltage, $\overline{\text{RESET}}$ Voltage and Delay Capacitor Voltage. $T_{DELAY}$ is the Time Between the Capacitor's Initial Charging and the Issuance of the $\overline{\text{RESET}}$ Signal**

A point often overlooked by designers is that the capacitor tolerance must be taken into account in the equation to guarantee the required *minimum delay time* for the microprocessor. If the capacitor has a ±10%, the delay could range from 19.5 ms to 71.5 ms.

## Real Time Reset

A real time reset circuit like the one in the CS8120 also consists of an open collector NPN transistor. To provide a reset delay, the user can connect an RC network as shown in Figure 2.

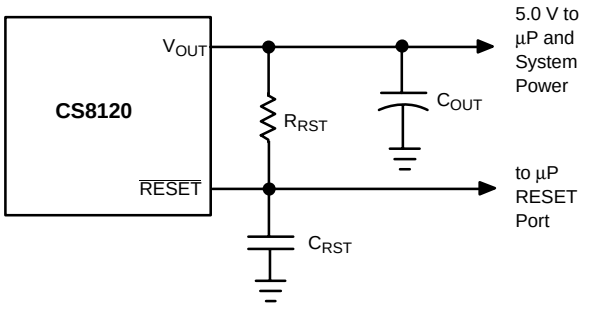



**Figure 2. RC Network for $\overline{\text{RESET}}$ Delay in the CS8120**

The capacitor $C_{RST}$ is charged to $V_{OUT}$ through the parallel combination of $R_{RST}$ and the input impedance of microprocessor reset line. Unlike the delayed reset, the real time reset output rises gradually from 0 V when a delay capacitor is used. If no capacitor is used, Reset goes high as soon as the output voltage is within specification. Of the two types of reset circuitry, more precise control is offered by the delayed reset option.

The reset delay time for the CS8120 is calculated using the standard capacitor charge formula:

$$V = e^{\frac{-t}{RC}}$$

Solving for the RC time constant, the equation becomes:

$$R_{TOT} \times C_{RST} = \left( \frac{-t_{DELAY}}{\ln\left(\frac{V_T - V_{OUT}}{V_{RST} - V_{OUT}}\right)} \right)$$

where:

$R_{TOT} = R_{RST}$ in parallel with $R_{IN}$,
$R_{IN}$ = input impedance of the microprocessor,
$C_{RST}$ = Reset delay capacitor,
$t_{DELAY}$ = desired delay time,
$V_T$ = microprocessor logic threshold voltage, and
$V_{RST}$ = Vsat of the reset pin (~0.4 V)

## Low Voltage Reset

The power supply for a microprocessor must be constantly monitored to ensure that it is within specification. Undervoltage conditions such as brief glitches or gradual decay due to an aging battery, can cause microprocessor errors. Power on Reset and low voltage Reset usually use the same circuitry and issue a Reset when the voltage they are monitoring falls out of regulation (Figure 3). As $V_{CC}$ rises above its minimum operating value, the reset output remains low for a fixed period ($t_{DELAY}$).

All ON Semiconductor reset circuitry includes hysteresis ($V_{RH}$) to provide noise immunity and avoid errors as the battery ages and the supply falls slowly out of regulation.

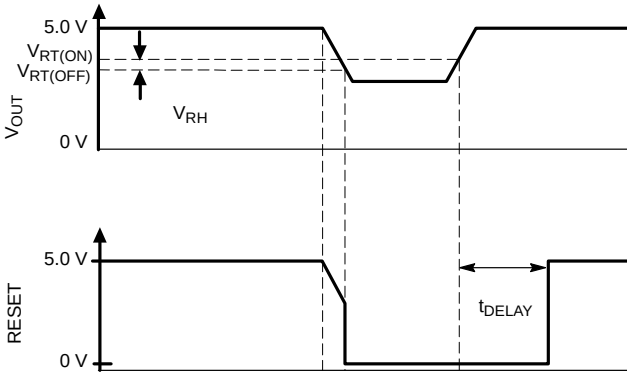



**Figure 3. Reset Waveforms During a Low Voltage Condition. When $V_{OUT}$ Falls Below $V_{RTON}$, the RESET Goes Low and Remains Low for a Fixed Period, $t_{DELAY}$ After $V_{OUT}$ Rises Above $V_{RT(OFF)}$**

## Watchdog

In a typical microprocessor system, the software routines are usually written as a number of modules within a larger, continuous loop. An error can cause the program to stall within a module.

A watchdog timer circuit is usually connected to the output port of a microprocessor and a short software routine is written to send an interrupt to this port within a predetermined time period. This short routine is incorporated in each module in the program loop. If the expected data is not received within this time period, the watchdog timer assumes there is an error and issues a system reset.

Several of the newer microprocessors have internal watchdog timers which are used to perform the self check described above. System designers who are reluctant to use the internal watchdog, implement it using either discrete circuitry, a specialized microprocessor supervisory IC or a SMART REGULATOR with a built–in watchdog timer such as the CS8140, CS8141 or CS8151 from ON Semiconductor.

The CS8140 has an externally programmable watchdog window while the CS8141 has a programmable lower watchdog frequency. The CS8140 offers tighter control since it has an upper and lower frequency threshold but the software requirements are more stringent.

Figure 4 shows a typical timing diagram for the CS8140 where, after a period of normal operation, the watchdog signal frequency increases beyond the upper limit. A programmable reset pulse train is issued until a watchdog signal is received within the required time period.

## Wake Up

Microprocessors used in battery operated equipment usually have an operating mode where some or all of the internal circuitry is shut down to conserve energy. This low power operating mode is known by many different names including, halt, suspend, idle, sleep, etc., depending on the manufacturer.

The microprocessor can be restarted from this sleep mode using a real time interrupt triggered by some external event or by periodically interrupting the microprocessor and having it perform a checking routine to see if it needs to remain active or return to the sleep mode.

The CS8151 combines a linear regulator with watchdog, wakeup and reset control functions. The wake–up output signal interrupts the microprocessor periodically at a frequency determined by an external capacitor. In the CS8151, a single capacitor ($C_{DELAY}$ in Figure 5) determines the wake up signal frequency, wake up delay time and reset pulse width. The SMART REGULATOR control functions are integrated in such a way that the regulator issues a wake–up signal and waits for a watchdog signal back from the microprocessor (Figure 6). If the microprocessor fails to send a WDI within one wake up period, the regulator issues a RESET (Figure 7).

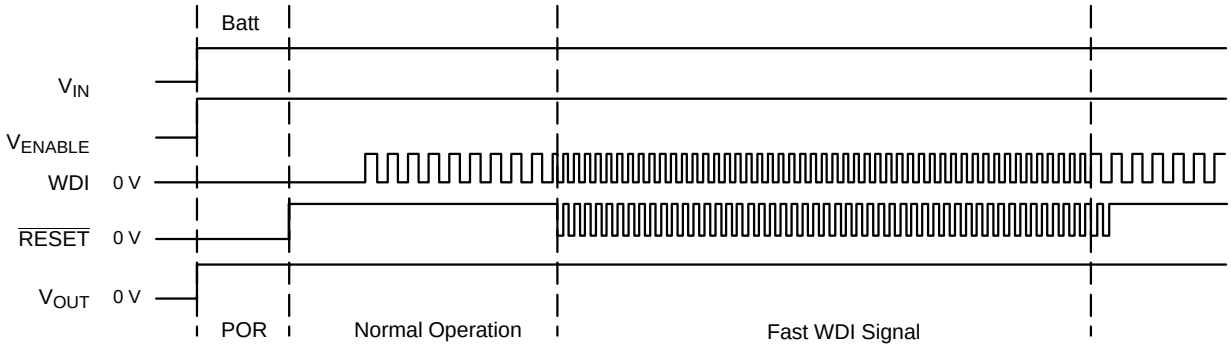



**Figure 4. WDI Frequency Rises Above the Upper Frequency Threshold After a Normal Period of Operation. The CS8140 Issues a RESET Pulse Train Until the WDI Frequency Falls Back Within its Preset Limits**

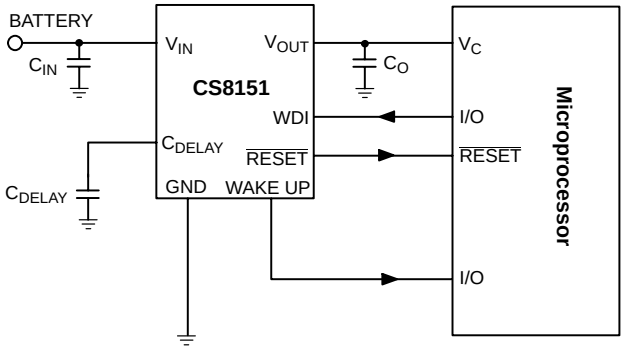



**Figure 5. In the CS8151, $C_{IN}$ is a Filtering Capacitor and $C_O$ is a Compensation Capacitor. $C_{DELAY}$ Sets the Timing for the RESET and Wake Up Functions**

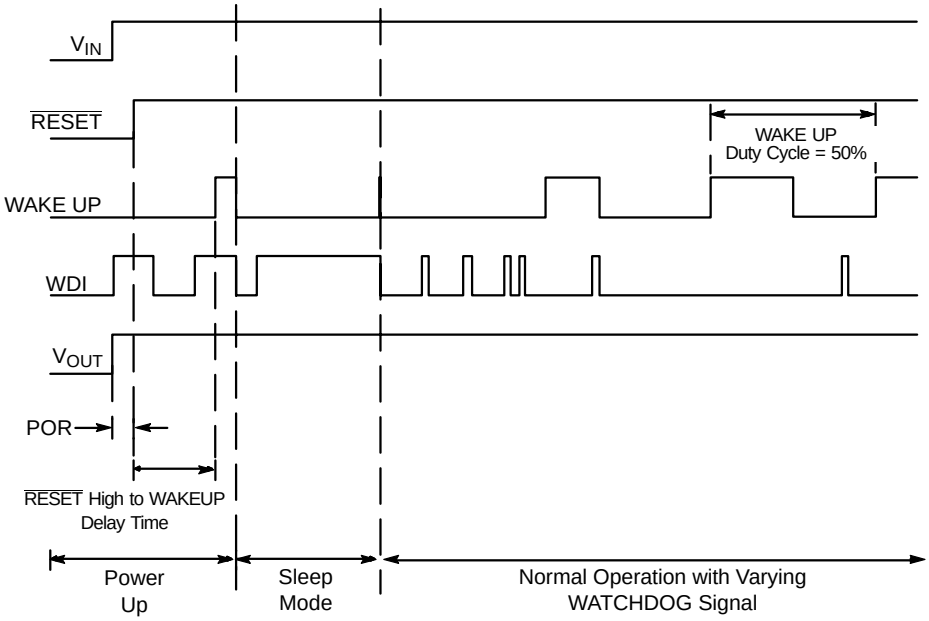



**Figure 6. Power Up, Sleep Mode and Normal Operation for CS8151. After Power Up, the Microprocessor Remains in Sleep Mode and Sends Back at Least One WDI within Each Wake Up Period**

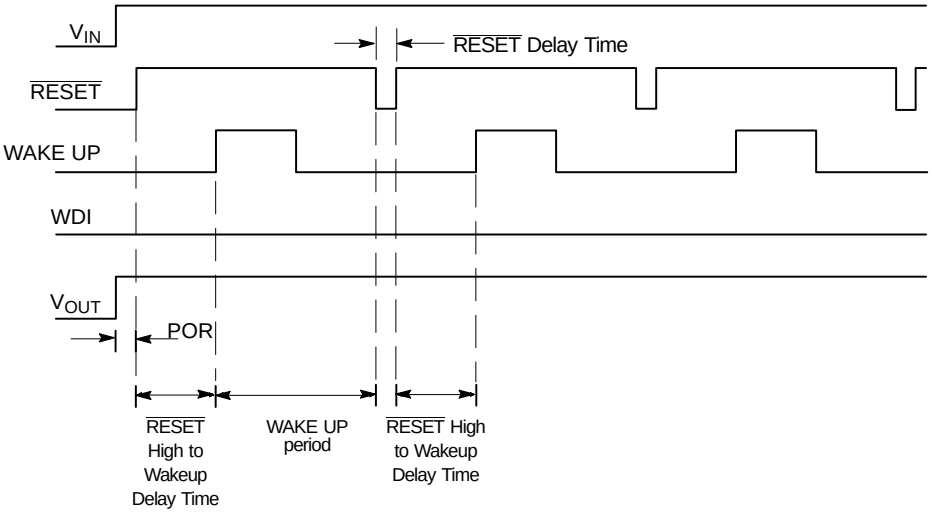



**Figure 7. When the Microprocessor Fails to Send a WDI Signal to the Regulator, the CS8151 Issues a RESET Back to the Microprocessor Until a WDI Appears**

### On–Off Control or Enable

The Enable or on/off pin provides a means of controlling the regulator's output voltage (one or both outputs in a dual regulator). This feature is also called Shutdown or Inhibit depending on the manufacturer and the device.

Switching off outputs when they are not needed reduces power consumption and prolongs battery life.

Enable circuitry is usually TTL or CMOS compatible so that it can be controlled directly from logic circuitry.

If Enable is not required in a design, it should be tied high or low depending on its signal polarity, to keep the output permanently on. With the CS8120 in Figure 8, the output voltage is on when the voltage on the Enable pin is less than 1.1 V. Conversely, the CS8140's enable is active high. Its enable pin must be tied high, to keep the output voltage on.

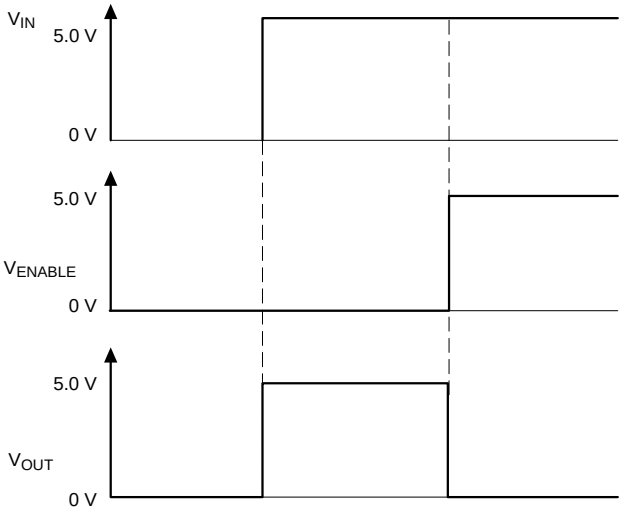



**Figure 8. The CS8120 Regulator Output Remains On when the Enable Voltage is Low and is Switched Off when Enable is Pulled High**

### Working with Integrated Smart Features A Design Example

When a number of microprocessor control features occur in a single SMART REGULATOR, it's not always clear which one(s) should be considered first. However, for most microprocessor based systems, the overriding requirement is the reset delay (also known as power on reset). For SMART REGULATORs like the CS8140 where Reset, Enable and Watchdog are set by one external capacitor, the capacitor is chosen to meet the reset delay requirement. Reset duration and watchdog timing follow.

For the CS8140, reset delay is given by:

$$T_{POR}(\text{typical}) = (4.75 \times 10^5) \times C_{DELAY}$$

From the CS8140 data sheet, the reset delay has a tolerance of ±37%. In addition, the external capacitor has a ±10% tolerance. The equation for the minimum $T_{POR}$ is

$$T_{POR}(\text{min}) = (4.75 \times 10^5 \times 0.63) \times C_{DELAY} \times 0.9$$

Solving for the minimum value of $C_{DELAY}$,

$$C_{DELAY}(\text{min}) = \frac{T_{POR}(\text{min})}{2.69 \times 10^5}$$

If, for this design example, the reset delay period must be a minimum of 200 ms, then

$$C_{DELAY}(\text{min}) = 0.743\ \mu F$$

Since the closest standard value is 0.82 μF, the minimum and maximum delays using 0.82 μF will be 220 ms and 586 ms respectively.

The duration of the reset pulse in the CS8140 is given by:

$$T_{WDI(reset)} = (1.0 \times 10^4) \times C_{DELAY}$$

With the capacitor value fixed at 0.82 mF, and a tolerance of ±50% due to the IC, and ±10% due to the capacitor, the duration of the reset pulse ranges from 3.69 ms to 13.5 ms.

The watchdog signal can be expressed as a frequency or time period. From a programmers point of view, time is more useful since they must ensure that a watchdog signal is issued consistently several times per second.

The maximum and minimum watchdog times are given by:

$$T_{WDI(LOWER)} = (1.3 \times 10^5)C_{DELAY}$$

$$T_{WDI(UPPER)} = (3.82 \times 10^4)C_{DELAY}$$

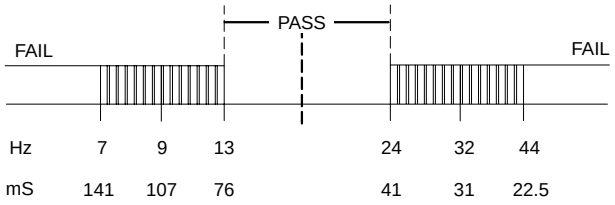
As with the above calculations, the tolerance of the IC and the external capacitor must be considered. With a tolerance of ±20% from the IC and ±10% from the capacitor, the above two equations become

$$T_{WDI(LOWER)} = (1.30 \times 1.2 \times 10^5)(1.1 \times 0.82 \times 10^{-6}) = 141\ \text{ms}$$

$$T_{WDI(UPPER)} = (3.82 \times 0.8 \times 10^4)(0.9 \times 0.82 \times 10^{-6}) = 22.5\ \text{ms}$$

$$T_{WDI(LOWER)} = (1.30 \times 0.8 \times 10^5)(0.9 \times 0.82 \times 10^{-6}) = 76\ \text{ms}$$

$$T_{WDI(UPPER)} = (3.82 \times 1.2 \times 10^4)(1.1 \times 0.82 \times 10^{-6}) = 41\ \text{ms}$$




C = 0.1 μF ±10%

**Figure 9. WDI Signal for $C_{DELAY}$ = 0.82 μF Using CS8140**

Based on these calculations, the software must be written so that a watchdog signal arrives at least every 76 ms but not faster than every 41 ms.

### Energy Conservation and Smart Features

Energy conservation is another benefit of using a regulator with integrated microprocessor control features. Using the CS8140 or CS8141 as indicated in Figure 10, the microprocessor can control its own power down sequence.

The momentary contact switch quickly charges C1 through R1. When the voltage across C1 reaches 3.95 V ( the enable threshold), the output switches on and $V_{OUT}$ rises to 5.0 V. After a delay period determined by $C_{DELAY}$, a frequency programmable reset pulse train is generated at the reset output. The pulse train continues until the correct watchdog signal appears at the WDI pin. C1 is now left to discharge through the input impedance of the enable pin (approximately 150 kΩ) and the enable signal disappears. The output voltage remains at 5.0 V as long as the CS8140 continues to receive the correct watchdog signal.

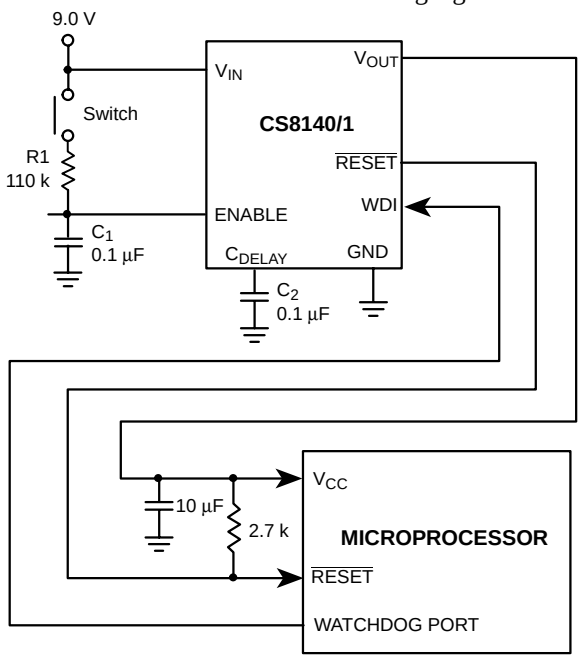



**Figure 10. Applications Diagram for CS8140 Provides a 5.0 V Tightly Regulated Supply and Control Function to the Microprocessor. In this Application, the Microprocessor Controls its Own Power Down Sequence (*see text*)**

The microprocessor can power itself down by terminating its watchdog signal. When the microprocessor finishes its housekeeping or power down software routine, it stops sending a watchdog signal. In response, the regulator generates a reset signal and goes into a sleep mode where $V_{OUT}$ drops to 0 V, shutting down the microprocessor.

## Conclusion

As the CS8140 design example illustrates, SMART REGULATORs with their integrated microprocessor control feature offer a level of control and flexibility unavailable with discrete implementations.

# Notes

SMART REGULATOR is a registered trademark of Semiconductor Components Industries, LLC (SCILLC).



## PUBLICATION ORDERING INFORMATION

**Literature Fulfillment**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
**Fax**: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
**Email**: ONlit@hibbertco.com

**N. American Technical Support**: 800–282–9855 Toll Free USA/Canada

**JAPAN**: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
**Phone**: 81–3–5740–2700
**Email**: r14525@onsemi.com

**ON Semiconductor Website**: http://onsemi.com

For additional information, please contact your local
Sales Representative.