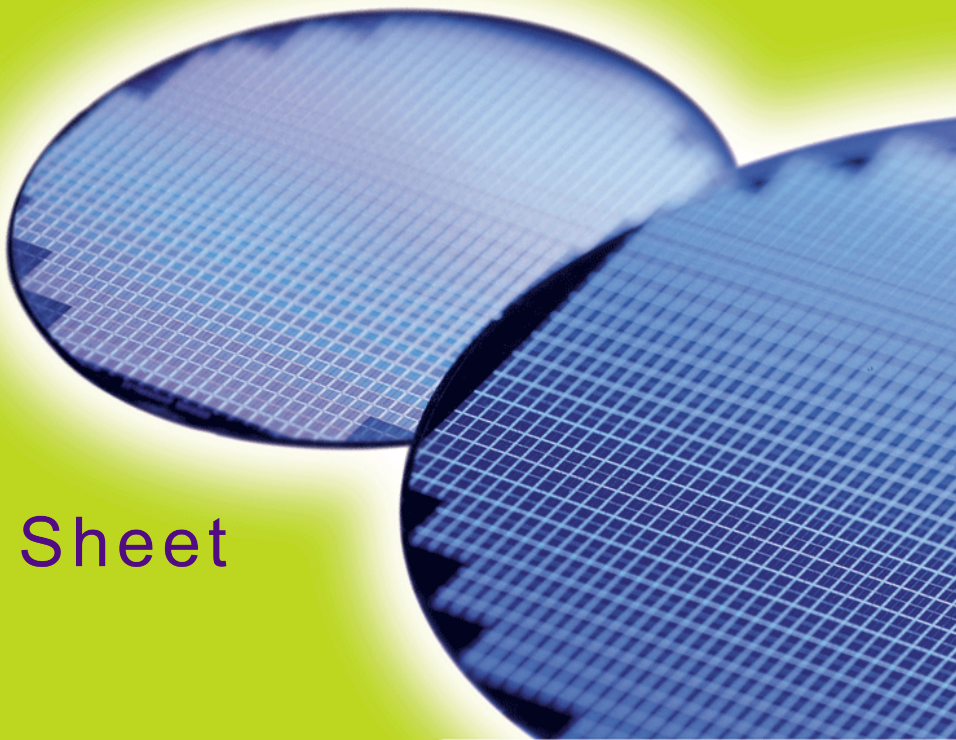
August 2007

HYS72D64301HBR–[5/6]–C
HYS72D128300HBR–[5/6]–C
HYS72D128321HBR–[5/6]–C
HYS72D256x20HBR–[5/6]–C

184-Pin Registered Double-Data-Rate SDRAM Module
RDIMM
DDR SDRAM
RoHS Compliant



Internet Data Sheet

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HYS72D64301HBR–[5/6]–C, HYS72D128300HBR–[5/6]–C, HYS72D128321HBR–[5/6]–C, HYS72D256x20HBR–[5/6]–C

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Page	Subjects (major changes since last revision)
All	Adapted internet edition
All	Tables updated
Previous Revision: 2006-03, Rev. 1.21	
All	Qimonda update
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Page	**Subjects (major changes since last revision)**
8	Added product types to PC2700R
Previous Revision: 2005-12, Rev. 1.1	

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1 Overview

1.1 Features

- 184-Pin Registered 8-Byte Dual-In-Line DDR SDRAM Module for PC, Workstation and Server main memory applications
- One rank 64M ×72, 128M ×72 organization , and two ranks 256M ×72 organization
- Standard Double Data Rate Synchronous DRAMs (DDR SDRAM) with a single + 2.5 V (± 0.2 V) power supply and +2.6 (± 0.1 V) power supply for DDR400
- Built with DDR SDRAMs in FBGA 60 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- RAS-lockout supported $t_{RAP}= t_{RCD}$
- All inputs and outputs SSTL_2 compatible
- Re-drive for all input signals using register and PLL devices.
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor: 133.35 mm × 28.58 mm (1.1”) × 4.00 mm and 133.35 mm × 30.48 mm (1.2”)
- Standard reference card layout Raw Card A, B, C and F
- Gold plated contacts
- RoHS Compliant Product[1)]

TABLE 1
Performance

Part Number Speed Code			–5	–6	Unit
Speed Grade	Component		DDR400B	DDR333B	—
	Module		PC3200–3033	PC2700–2533	—
max. Clock Frequency	@CL3	f_{CK3}	200	166	MHz
	@CL2.5	$f_{CK2.5}$	166	166	MHz
	@CL2	f_{CK2}	133	133	MHz

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The HYS72D[64/128/256]xxxHBR–[5/6]–C are low-profile versions of the standard Registered DIMM modules with 1.1-inch (28.58 mm) and 1.2-inch (30.40 mm) height for Server Applications. The low-profile DIMM versions are available as 64M ×72 (512MB), 128M ×72 (1 GB), and 256M ×72 (2 GB). The memory array is designed with Double-Data-Rate Synchronous DRAMs for ECC applications. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes contain factory programmed configuration data and the second 128 bytes are made available to the customer.

green Product

TABLE 2
Ordering Information

Product Type[1]	Compliance Code[2]	Description	SDRAM Technology
PC3200 (CL=3)			
HYS72D64301HBR–5–C	PC3200R–30331–A0	one rank 512 MByte Reg. ECC DIMM	512 MBit (×8)
HYS72D128300HBR–5–C	PC3200R–30331–C0	one rank 1 GByte Reg. ECC DIMM	512 MBit (×4)
HYS72D128321HBR–5–C	PC3200R–30331–B0	two ranks 1 GByte Reg. ECC DIMM	512 MBit (×8)
HYS72D256320HBR–5–C	PC3200R–30331–F0	two ranks 2 GByte Reg. ECC DIMM	512 MBit (×4)
PC2700 (CL=2.5)			
HYS72D64301HBR–6–C	PC2700R–25331–A0	one rank 512 MByte Reg. ECC DIMM	512 MBit (×8)
HYS72D128300HBR–6–C	PC2700R–25331–C0	one rank 1 GByte Reg. ECC DIMM	512 MBit (×4)
HYS72D128900HBR–6–C	PC2700R–25331–C0	one rank 1 GByte Reg. ECC DIMM	512 MBit (×4)
HYS72D128321HBR–6–C	PC2700R–25331–B0	two ranks 1 GByte Reg. ECC DIMM	512 MBit (×8)
HYS72D256320HBR–6–C	PC2700R–25331–F0	two ranks 2 GByte Reg. ECC DIMM	512 MBit (×4)
HYS72D256920HBR–6–C	PC2700R–25331–F0	two ranks 2 GByte Reg. ECC DIMM	512 MBit (×4)

1) All product types end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS72D256320HBR–5–C, indicating Rev.C die are used for SDRAM components.
2) The Compliance Code is printed on the module labels and describes the speed sort (for example "PC2700R"), the latencies (for example "25331" means CAS latency of 2.5 clocks, Row-Column-Delay (RCD) latency of 3 clocks and Row Precharge latency of 3 clocks), SPD code definition version 1, and the Raw Card used for this module.

TABLE 3
Address Format

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/bank/ column bits	Refresh	Period	Interval
512 MB	64M ×72	1	64M ×8	9	13/2/11	8K	64 ms	7.8 ms
1 GB	128M ×72	1	128M ×4	18	13/2/12	8K	64 ms	7.8 ms
1 GB	128M ×72	2	64M ×8	18	13/2/11	8K	64 ms	7.8 ms
2 GB	256M ×72	2	128M ×4	36	13/2/12	8K	64 ms	7.8 ms

2 Pin Configuration

The pin configuration of the Registered DDR SDRAM DIMM is listed by function in **Table 4** (184 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 5** and **Table 6** respectively. The pin numbering is depicted in **Chapter 1**.

TABLE 4
Pin Configuration of RDIMM

Pin #	Name	Pin Type	Buffer Type	Function
Clock Signals				
137	CK0	I	SSTL	**Clock Signal**
138	$\overline{CK0}$	I	SSTL	**Complement Clock**
21	CKE0	I	SSTL	**Clock Enable Rank 0**
111	CKE1	I	SSTL	**Clock Enable Rank 1** *Note: 2-rank module*
	NC	NC	SSTL	*Note: 1-rank module*
Control Signals				
157	$\overline{S0}$	I	SSTL	**Chip Select of Rank 0**
158	$\overline{S1}$	I	SSTL	**Chip Select of Rank 1** *Note: 2-ranks module*
	NC	NC	–	*Note: 1-rank module*
154	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
65	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
63	$\overline{WE}$	I	SSTL	**Write Enable**
10	$\overline{RESET}$	I	LV-CMOS	**Register Reset** Forces registered inputs low *Note: For detailed description of the Power Up and Power Management see the Application Note at the end of data sheet*
Address Signals				
59	BA0	I	SSTL	**Bank Address Bus 1:0**
52	BA1	I	SSTL	
48	A0	I	SSTL	**Address Bus 11:0**
43	A1	I	SSTL	
41	A2	I	SSTL	
130	A3	I	SSTL	
37	A4	I	SSTL	**Address Bus 11:0**
32	A5	I	SSTL	
125	A6	I	SSTL	
29	A7	I	SSTL	
122	A8	I	SSTL	
27	A9	I	SSTL	
141	A10	I	SSTL	
	AP	I	SSTL	
118	A11	I	SSTL	
115	A12	I	SSTL	**Address Signal 12** *Note: Module based on 256 Mbit or larger dies*
	NC	NC	–	*Note: 128 Mbit based module*
167	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module*
	NC	NC	–	*Note: Module based on 512 Mbit or smaller dies*
Data Signals				
2	DQ0	I/O	SSTL	**Data Bus 63:0**
4	DQ1	I/O	SSTL	
6	DQ2	I/O	SSTL	
8	DQ3	I/O	SSTL	
94	DQ4	I/O	SSTL	
95	DQ5	I/O	SSTL	
98	DQ6	I/O	SSTL	
99	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
19	DQ10	I/O	SSTL	
20	DQ11	I/O	SSTL	
105	DQ12	I/O	SSTL	

Pin #	Name	Pin Type	Buffer Type	Function
106	DQ13	I/O	SSTL	**Data Bus 63:0**
109	DQ14	I/O	SSTL	
110	DQ15	I/O	SSTL	
23	DQ16	I/O	SSTL	
24	DQ17	I/O	SSTL	
28	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
114	DQ20	I/O	SSTL	
117	DQ21	I/O	SSTL	
121	DQ22	I/O	SSTL	
123	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
35	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
126	DQ28	I/O	SSTL	
127	DQ29	I/O	SSTL	
131	DQ30	I/O	SSTL	
133	DQ31	I/O	SSTL	
53	DQ32	I/O	SSTL	
55	DQ33	I/O	SSTL	
57	DQ34	I/O	SSTL	
60	DQ35	I/O	SSTL	
146	DQ36	I/O	SSTL	
147	DQ37	I/O	SSTL	
150	DQ38	I/O	SSTL	
151	DQ39	I/O	SSTL	
61	DQ40	I/O	SSTL	
64	DQ41	I/O	SSTL	
68	DQ42	I/O	SSTL	
69	DQ43	I/O	SSTL	
153	DQ44	I/O	SSTL	
155	DQ45	I/O	SSTL	
161	DQ46	I/O	SSTL	
162	DQ47	I/O	SSTL	
72	DQ48	I/O	SSTL	
73	DQ49	I/O	SSTL	
79	DQ50	I/O	SSTL	
80	DQ51	I/O	SSTL	
165	DQ52	I/O	SSTL	

Pin #	Name	Pin Type	Buffer Type	Function
166	DQ53	I/O	SSTL	**Data Bus 63:0**
170	DQ54	I/O	SSTL	
171	DQ55	I/O	SSTL	
83	DQ56	I/O	SSTL	
84	DQ57	I/O	SSTL	
87	DQ58	I/O	SSTL	
88	DQ59	I/O	SSTL	
174	DQ60	I/O	SSTL	
175	DQ61	I/O	SSTL	
178	DQ62	I/O	SSTL	
179	DQ63	I/O	SSTL	
44	CB0	I/O	SSTL	**Check Bits 7:0**
45	CB1	I/O	SSTL	
49	CB2	I/O	SSTL	
51	CB3	I/O	SSTL	
134	CB4	I/O	SSTL	
135	CB5	I/O	SSTL	
142	CB6	I/O	SSTL	
144	CB7	I/O	SSTL	
5	DQS0	I/O	SSTL	**Data Strobes 8:0** *Note: See block diagram for corresponding DQ signals*
14	DQS1	I/O	SSTL	
25	DQS2	I/O	SSTL	
36	DQS3	I/O	SSTL	
56	DQS4	I/O	SSTL	
67	DQS5	I/O	SSTL	
78	DQS6	I/O	SSTL	
86	DQS7	I/O	SSTL	
47	DQS8	I/O	SSTL	
97	DM0	I	SSTL	**Data Mask 0** *Note: ×8 based module*
	DQS9	I/O	SSTL	**Data Strobe 9** *Note: ×4 based module*
107	DM1	I	SSTL	**Data Mask 1** *Note: ×8 based module*
	DQS10	I/O	SSTL	**Data Strobe 10** *Note: ×4 based module*
119	DM2	I	SSTL	**Data Mask 2** *Note: ×8 based module*
	DQS11	I/O	SSTL	**Data Strobe 11** *Note: ×4 based module*

Pin #	Name	Pin Type	Buffer Type	Function
129	DM3	I	SSTL	**Data Mask 3** *Note: ×8 based module*
	DQS12	I/O	SSTL	**Data Strobe 12** *Note: ×4 based module*
149	DM4	I	SSTL	**Data Mask 4** *Note: ×8 based module*
	DQS13	I/O	SSTL	**Data Strobe 13** *Note: ×4 based module*
159	DM5	I	SSTL	**Data Mask 5** *Note: ×8 based module*
	DQS14	I/O	SSTL	**Data Strobe 14** *Note: ×4 based module*
169	DM6	I	SSTL	**Data Mask 6** *Note: ×8 based module*
	DQS15	I/O	SSTL	**Data Strobe 15** *Note: ×4 based module*
177	DM7	I	SSTL	**Data Mask 7** *Note: ×8 based module*
	DQS16	I/O	SSTL	**Data Strobe 16** *Note: ×4 based module*
140	DM8	I	SSTL	**Data Mask 8** *Note: ×8 based module*
	DQS17	I/O	SSTL	**Data Strobe 17** *Note: ×4 based module*
EEPROM				
92	SCL	I	CMOS	**Serial Bus Clock**
91	SDA	I/O	OD	**Serial Bus Data**
181	SA0	I	CMOS	**Slave Address Select Bus 2:0**
182	SA1	I	CMOS	
183	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	–	**I/O Reference Voltage**
184	V_{DDSPD}	PWR	–	**EEPROM Power Supply**

Pin #	Name	Pin Type	Buffer Type	Function
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	PWR	–	**Power Supply**
3	V_{SS}	GND	–	**Ground Plane**
11				
18				
26				
34				
42				
50				
58				
66				
74				
81				
89				
93				
100				

Pin #	Name	Pin Type	Buffer Type	Function
116	V_{SS}	GND	–	**Ground Plane**
124				
132				
139				
145				
152				
160				
176				
Other Pins				
82	V_{DDID}	O	OD	**V_{DD} Identification** *Note: Pin in tristate, indicating V_{DD} and V_{DDQ} nets connected on PCB*
9, 16, 17, 71, 75, 76, 90, 101, 102, 103, 113, 163, 173	NC	NC	–	**Not connected** Pins not connected on Qimonda RDIMM's

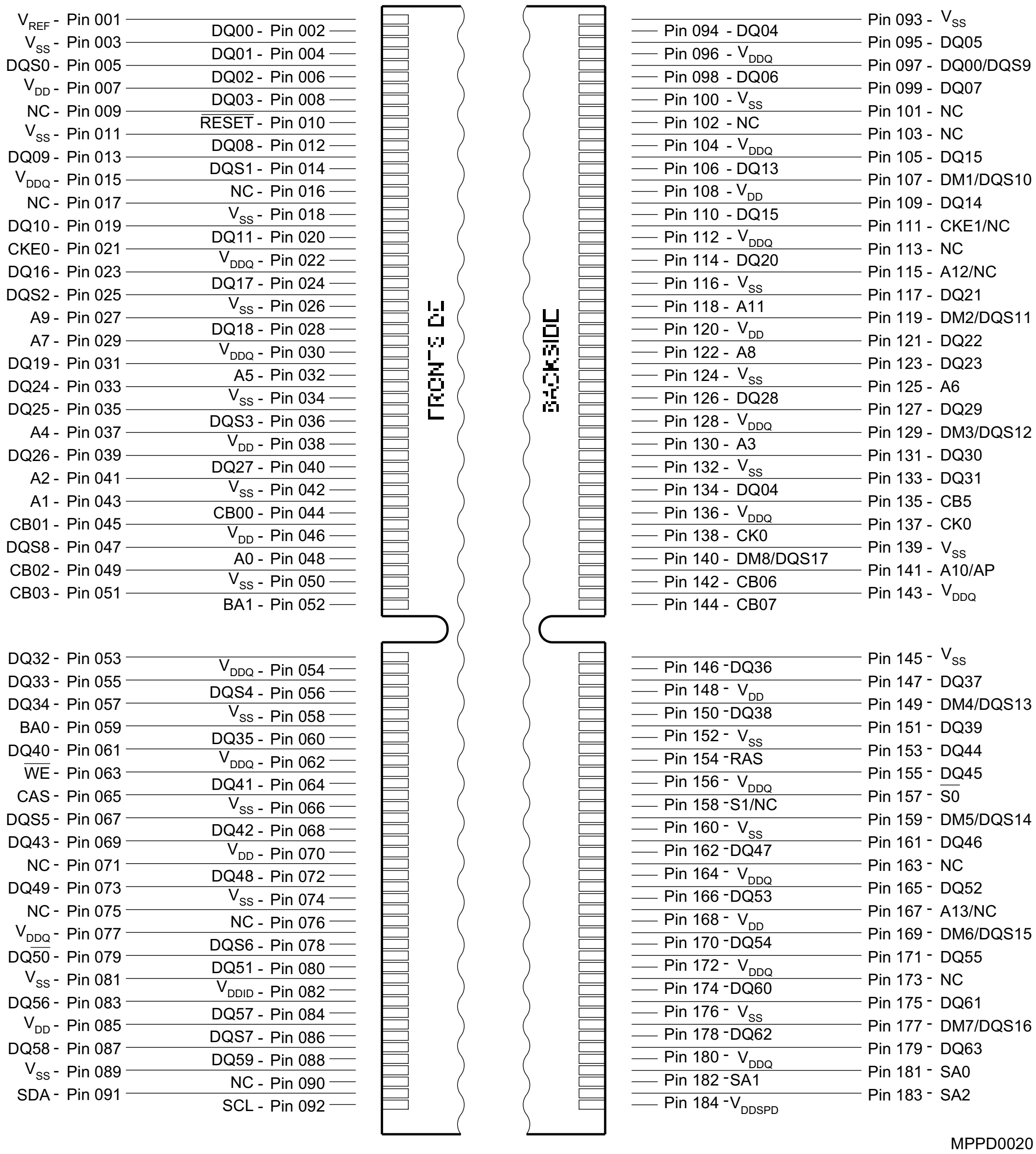
TABLE 5
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

TABLE 6
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminalted Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 1
Pin Configuration 184 Pins, Registered



3 Electrical Characteristics

3.1 Operating Conditions

TABLE 7
Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	PD	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

***Attention:** Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.*

TABLE 8
Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition[1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	$f_{CK} \le 166$ MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	$f_{CK} \le 166$ MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz [2][3]
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	[4]
I/O Termination Voltage (System)	V_{TT}	$V_{REF} - 0.04$		$V_{REF} + 0.04$	V	[5]
Input High (Logic1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$		$V_{DDQ} + 0.3$	V	[6]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3		$V_{REF} - 0.15$	V	[6]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3		$V_{DDQ} + 0.3$	V	[6]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		$V_{DDQ} + 0.6$	V	[6][7]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[8]
Input Leakage Current	I_I	–2		2	µA	Any input $0 V \le V_{IN} \le V_{DD}$; All other pins not under test = 0 V[9]
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; $0 V \le V_{OUT} \le V_{DDQ}$ [9]
Output High Current, Normal Strength Driver	I_{OH}	—		–16.2	mA	V_{OUT} = 1.95 V
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V;
2) DDR400 conditions apply for all clock frequencies above 166 MHz
3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
4) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF.DC}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
6) Inputs are not recognized as valid until V_{REF} stabilizes.
7) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
8) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
9) Values are shown per pin.

TABLE 9
I_{DD} Conditions

Parameter	Symbol
Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet.	I_{DD1}
Precharge Power-Down Standby Current all banks idle; power-down mode; CKE ≤ $V_{IL,MAX}$	I_{DD2P}
Precharge Floating Standby Current $\overline{CS}$ ≥ $V_{IH,,MIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$; address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ $V_{IH,MIN}$; V_{IN} = V_{REF} for DQ, DQS and DM; address and other control inputs stable at ≥ $V_{IH,MIN}$ or ≤ $V_{IL,MAX}$.	I_{DD2Q}
Active Power-Down Standby Current one bank active; power-down mode; CKE ≤ V_{ILMAX}; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD3P}
Active Standby Current one bank active; $\overline{CS}$ ≥ $V_{IH,MIN}$; CKE ≥ $V_{IH,MIN}$; t_{RC} = $t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; I_{OUT} = 0 mA	I_{DD4R}
Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	I_{DD4W}
Auto-Refresh Current t_{RC} = t_{RFCMIN}, burst refresh	I_{DD5}
Self-Refresh Current CKE ≤ 0.2 V; external clock on	I_{DD6}
Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet.	I_{DD7}

TABLE 10

I_{DD} Specification for HYS72D[64/128/256]xxxHBR–5–C

Product Type	HYS72D64301HBR–5–C		HYS72D128300HBR–5–C		HYS72D128321HBR–5–C		HYS72D256320HBR–5–C		Unit	Note [1)2)]
Organization	512 MB		1 GB		1 GB		2 GB			
	×72		×72		×72		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–5		–5		–5		–5			
Symbol	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I_{DD0}	1050	1240	1890	2210	1660	1910	3120	3570	mA	3)
I_{DD1}	1270	1470	2200	2530	1880	2140	3430	3890	mA	3)4)
I_{DD2P}	360	440	670	780	670	780	1290	1460	mA	5)
I_{DD2F}	830	940	1360	1510	1360	1510	2410	2650	mA	5)
I_{DD2Q}	510	600	960	1120	960	1120	1870	2140	mA	5)
I_{DD3P}	460	530	860	970	870	970	1670	1850	mA	5)
I_{DD3N}	920	1050	1540	1730	1540	1730	2770	3090	mA	5)
I_{DD4R}	1360	1510	2380	2620	1970	2190	3610	3980	mA	3)4)
I_{DD4W}	1400	1560	2470	2710	2020	2240	3700	4070	mA	3)
I_{DD5}	1670	2120	3280	4130	2290	2800	4510	5490	mA	3)
I_{DD6}	330	390	640	740	640	740	1270	1430	mA	5)
I_{DD7}	2390	2770	4450	5140	3010	3450	5680	6500	mA	3)4)

1) Module I_{DD} is calculated on the basis of component I_{DD} and includes Register and PLL currents
2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C
3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: **m** × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules
4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

TABLE 11

I_{DD} Specification for HYS72D[64/128/256]xxxHBR–6–C

Product Type	HYS72D64301HBR–6–C		HYS72D128300HBR–6–C HYS72D128900HBR–6–C		HYS72D128321HBR–6–C		HYS72D256320HBR–6–C HYS72D256920HBR–6–C		Unit	Note[1)2)]
Organization	512 MB		1 GB		1 GB		2 GB			
	×72		×72		×72		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–6		–6		–6		–6			
Symbol	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I_{DD0}	1000	1140	1790	2020	1530	1720	2860	3180	mA	3)
I_{DD1}	1160	1360	2000	2330	1700	1940	3060	3490	mA	3)4)
I_{DD2P}	340	410	600	700	600	700	1120	1280	mA	5)
I_{DD2F}	740	840	1180	1310	1180	1310	2060	2260	mA	5)
I_{DD2Q}	470	560	860	1000	860	1000	1630	1890	mA	5)
I_{DD3P}	430	500	770	880	770	880	1460	1640	mA	5)
I_{DD3N}	830	940	1370	1520	1370	1520	2440	2690	mA	5)
I_{DD4R}	1210	1410	2090	2420	1740	1990	3150	3580	mA	3)4)
I_{DD4W}	1250	1450	2180	2510	1790	2030	3240	3670	mA	3)
I_{DD5}	1510	1950	2930	3780	2040	2530	4000	4940	mA	3)
I_{DD6}	320	390	580	680	580	680	1110	1270	mA	5)
I_{DD7}	2150	2490	3980	4580	2690	3070	5040	5750	mA	3)4)

1) Module I_{DD} is calculated on the basis of component I_{DD} and includes Register and PLL currents
2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C
3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: **m** × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules
4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

3.2 A.C. Timing Parameters

TABLE 12
AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1)]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.5	+0.5	–0.7	+0.7	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock cycle time	t_{CK}	5	8	6	12	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK})+(t_{RP}/t_{CK})$				t_{CK}	2)3)4)5)6)
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.6	+0.6	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.40	ns	TFBGA 2)3)4)5)
Write command to 1st DQS latching transition	t_{DQSS}	0.72	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	ns	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})	—	min. (t_{CL}, t_{CH})	—	ns	2)3)4)5)
DQ & DQS high-impedance time from CK/$\overline{CK}$	t_{HZ}	—	+0.7	—	+0.7	ns	2)3)4)5)7)
Address and control input hold time	t_{IH}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)8)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)8)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)9)

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Address and control input setup time	t_{IS}	0.6	—	0.75	—	ns	fast slew rate [3][4][5][6][8]
		0.7	—	0.8	—	ns	slow slew rate [3][4][5][6][8]
DQ & DQS low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.7	–0.7	+0.7	ns	[2][3][4][5][7]
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	[2][3][4][5]
DQ/DQS output hold time from DQS	t_{QH}	t_{HP} –t_{QHS}	—	t_{HP} –t_{QHS}	—	ns	[2][3][4][5]
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.50	ns	TFBGA [2][3][4][5]
Active to Autoprecharge delay	t_{RAP}	t_{RCD}	—	t_{RCD}	—	ns	[2][3][4][5]
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	ns	[2][3][4][5]
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	ns	[2][3][4][5]
Active to Read or Write delay	t_{RCD}	15	—	18	—	ns	[2][3][4][5]
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	[2][3][4][5][10]
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	65	—	72	—	ns	[2][3][4][5]
Precharge command period	t_{RP}	15	—	18	—	ns	[2][3][4][5]
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	[2][3][4][5]
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	[2][3][4][5]
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	ns	[2][3][4][5]
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	[2][3][4][5]
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	[2][3][4][5][11]
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	[2][3][4][5][12]
Write recovery time	t_{WR}	15	—	15	—	ns	[2][3][4][5]
Internal write to read command delay	t_{WTR}	2	—	1	—	t_{CK}	[2][3][4][5]
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	[2][3][4][5]
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	[2][3][4][5]

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); $_{DDQ}$ = 2.6 V ± 0.1 V, $_{DD}$ = +2.6 V ± 0.1 V (DDR400)
2) Input slew rate ≥ 1 V/ns for DDR400, DDR333
3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.
4) Inputs are not recognized as valid until V_{REF} stabilizes.
5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.
6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.

9) These parameters guarantee device timing, but they are not necessarily tested on each device.

10) A maximun of eight Autorefresh commands can be posted to any given DDR SDRAM device

11) The specific requirement is that DQS be valid (HIGH,LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specificationsof the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW at this time, depending on t_{DQSS}.

12) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

4 SPD Codes

TABLE 13
SPD Codes for HYS72D[64/128/256]3[00/01/20/21]HBR–5–C

Product Type		HYS72D64301HBR–5–C	HYS72D128321HBR–5–C	HYS72D128300HBR–5–C	HYS72D256320HBR–5–C
Organization		512 MB	1 GByte	1 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×8)	2 Ranks (×8)	1 Rank (×4)	2 Ranks (×4)
Label Code		PC3200R–30331	PC3200R–30331	PC3200R–30331	PC3200R–30331
	JEDEC SPD Revision	Rev 1.0	Rev 1.0	Rev 1.0	Rev 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0C	0C
5	Number of DIMM Ranks	01	02	01	02
6	Data Width (LSB)	48	48	48	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70	70	70
11	Error Correction Support	02	02	02	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	04	04
14	Error Checking SDRAM Width	08	08	04	04
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04

Product Type		HYS72D64301HBR–5–C	HYS72D128321HBR–5–C	HYS72D128300HBR–5–C	HYS72D256320HBR–5–C
Organization		**512 MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**1 Rank (×4)**	**2 Ranks (×4)**
Label Code		**PC3200R–30331**	**PC3200R–30331**	**PC3200R–30331**	**PC3200R–30331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
18	CAS Latency	1C	1C	1C	1C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	26	26	26	26
22	Component Attributes	C1	C1	C1	C1
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	60	60	60	60
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70	70	70
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	75	75	75	75
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	70	70	70	70
27	t_{RPmin} [ns]	3C	3C	3C	3C
28	t_{RRDmin} [ns]	28	28	28	28
29	t_{RCDmin} [ns]	3C	3C	3C	3C
30	t_{RASmin} [ns]	28	28	28	28
31	Module Density per Rank	80	80	01	01
32	t_{AS}, t_{CS} [ns]	60	60	60	60
33	t_{AH}, t_{CH} [ns]	60	60	60	60
34	t_{DS} [ns]	40	40	40	40
35	t_{DH} [ns]	40	40	40	40
36 - 40	not used	00	00	00	00
41	t_{RCmin} [ns]	37	37	37	37
42	t_{RFCmin} [ns]	41	41	41	41
43	t_{CKmax} [ns]	28	28	28	28
44	$t_{DQSQmax}$ [ns]	28	28	28	28
45	t_{QHSmax} [ns]	50	50	50	50
46	not used	00	00	00	00
47	DIMM PCB Height	01	01	01	01

Product Type		**HYS72D64301HBR–5–C**	**HYS72D128321HBR–5–C**	**HYS72D128300HBR–5–C**	**HYS72D256320HBR–5–C**
Organization		**512 MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**1 Rank (×4)**	**2 Ranks (×4)**
Label Code		**PC3200R–30331**	**PC3200R–30331**	**PC3200R–30331**	**PC3200R–30331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
48 - 61	not used	00	00	00	00
62	SPD Revision	10	10	10	10
63	Checksum of Byte 0-62	C7	C8	41	42
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	37	37	37	37
74	Part Number, Char 2	32	32	32	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	31	31	32
77	Part Number, Char 5	34	32	32	35
78	Part Number, Char 6	33	38	38	36
79	Part Number, Char 7	30	33	33	33
80	Part Number, Char 8	31	32	30	32
81	Part Number, Char 9	48	31	30	30
82	Part Number, Char 10	42	48	48	48
83	Part Number, Char 11	52	42	42	42
84	Part Number, Char 12	35	52	52	52
85	Part Number, Char 13	43	35	35	35
86	Part Number, Char 14	20	43	43	43

Product Type		**HYS72D64301HBR–5–C**	**HYS72D128321HBR–5–C**	**HYS72D128300HBR–5–C**	**HYS72D256320HBR–5–C**
Organization		**512 MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**1 Rank (×4)**	**2 Ranks (×4)**
Label Code		**PC3200R–30331**	**PC3200R–30331**	**PC3200R–30331**	**PC3200R–30331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx	xx	xx
99 - 127	not used	00	00	00	00

TABLE 14
SPD Codes for HYS72D[64/128/256]3[00/01/20/21]HBR–6–C

Product Type		**HYS72D64301HBR–6–C**	**HYS72D128321HBR–6–C**	**HYS72D128300HBR–6–C**	**HYS72D256320HBR–6–C**
Organization		**512 MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**1 Rank (×4)**	**2 Ranks (×4)**
Label Code		**PC2700R–25331**	**PC2700R–25331**	**PC2700R–25331**	**PC2700R–25331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0C	0C
5	Number of DIMM Ranks	01	02	01	02
6	Data Width (LSB)	48	48	48	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	60	60	60	60
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70	70	70
11	Error Correction Support	02	02	02	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	04	04
14	Error Checking SDRAM Width	08	08	04	04
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	0C	0C	0C	0C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	26	26	26	26
22	Component Attributes	C1	C1	C1	C1

Product Type		**HYS72D64301HBR–6–C**	**HYS72D128321HBR–6–C**	**HYS72D128300HBR–6–C**	**HYS72D256320HBR–6–C**
Organization		**512 MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**1 Rank (×4)**	**2 Ranks (×4)**
Label Code		**PC2700R–25331**	**PC2700R–25331**	**PC2700R–25331**	**PC2700R–25331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	75	75	75	75
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70	70	70
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	00	00	00	00
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	00	00	00	00
27	t_{RPmin} [ns]	48	48	48	48
28	t_{RRDmin} [ns]	30	30	30	30
29	t_{RCDmin} [ns]	48	48	48	48
30	t_{RASmin} [ns]	2A	2A	2A	2A
31	Module Density per Rank	80	80	01	01
32	$t_{AS,}$ t_{CS} [ns]	75	75	75	75
33	$t_{AH,}$ t_{CH} [ns]	75	75	75	75
34	t_{DS} [ns]	45	45	45	45
35	t_{DH} [ns]	45	45	45	45
36 - 40	not used	00	00	00	00
41	t_{RCmin} [ns]	3C	3C	3C	3C
42	t_{RFCmin} [ns]	48	48	48	48
43	t_{CKmax} [ns]	30	30	30	30
44	$t_{DQSQmax}$ [ns]	28	28	28	28
45	t_{QHSmax} [ns]	50	50	50	50
46	not used	00	00	00	00
47	DIMM PCB Height	01	01	01	01
48 - 61	not used	00	00	00	00
62	SPD Revision	10	10	10	10
63	Checksum of Byte 0-62	61	62	DB	DC
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F

Product Type		**HYS72D64301HBR–6–C**	**HYS72D128321HBR–6–C**	**HYS72D128300HBR–6–C**	**HYS72D256320HBR–6–C**
Organization		**512 MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**1 Rank (×4)**	**2 Ranks (×4)**
Label Code		**PC2700R–25331**	**PC2700R–25331**	**PC2700R–25331**	**PC2700R–25331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	37	37	37	37
74	Part Number, Char 2	32	32	32	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	31	31	32
77	Part Number, Char 5	34	32	32	35
78	Part Number, Char 6	33	38	38	36
79	Part Number, Char 7	30	33	33	33
80	Part Number, Char 8	31	32	30	32
81	Part Number, Char 9	48	31	30	30
82	Part Number, Char 10	42	48	48	48
83	Part Number, Char 11	52	42	42	42
84	Part Number, Char 12	36	52	52	52
85	Part Number, Char 13	43	36	36	36
86	Part Number, Char 14	20	43	43	43
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x

Product Type		HYS72D64301HBR–6–C	HYS72D128321HBR–6–C	HYS72D128300HBR–6–C	HYS72D256320HBR–6–C
Organization		**512 MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**1 Rank (×4)**	**2 Ranks (×4)**
Label Code		**PC2700R–25331**	**PC2700R–25331**	**PC2700R–25331**	**PC2700R–25331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx	xx	xx
99 - 127	not used	00	00	00	00

TABLE 15
SPD Codes for HYS72D[128/256]90x0HBR–6–C

Product Type		HYS72D128900HBR–6–C	HYS72D256920HBR–6–C
Organization		1 GByte	2 GByte
		×72	×72
		1 Rank (×4)	2 Ranks (×4)
Label Code		PC2700R–25331	PC2700R–25331
	JEDEC SPD Revision	Rev 1.0	Rev 1.0
Byte#	Description	HEX	HEX
0	Programmed SPD Bytes in E2PROM	80	80
1	Total number of Bytes in E2PROM	08	08
2	Memory Type (DDR = 07h)	07	07
3	Number of Row Addresses	0D	0D
4	Number of Column Addresses	0C	0C
5	Number of DIMM Ranks	01	02
6	Data Width (LSB)	48	48
7	Data Width (MSB)	00	00
8	Interface Voltage Levels	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	60	60
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70
11	Error Correction Support	02	02
12	Refresh Rate	82	82
13	Primary SDRAM Width	04	04
14	Error Checking SDRAM Width	04	04
15	t_{CCD} [cycles]	01	01
16	Burst Length Supported	0E	0E
17	Number of Banks on SDRAM Device	04	04
18	CAS Latency	0C	0C
19	CS Latency	01	01
20	Write Latency	02	02
21	DIMM Attributes	26	26
22	Component Attributes	C1	C1
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	75	75

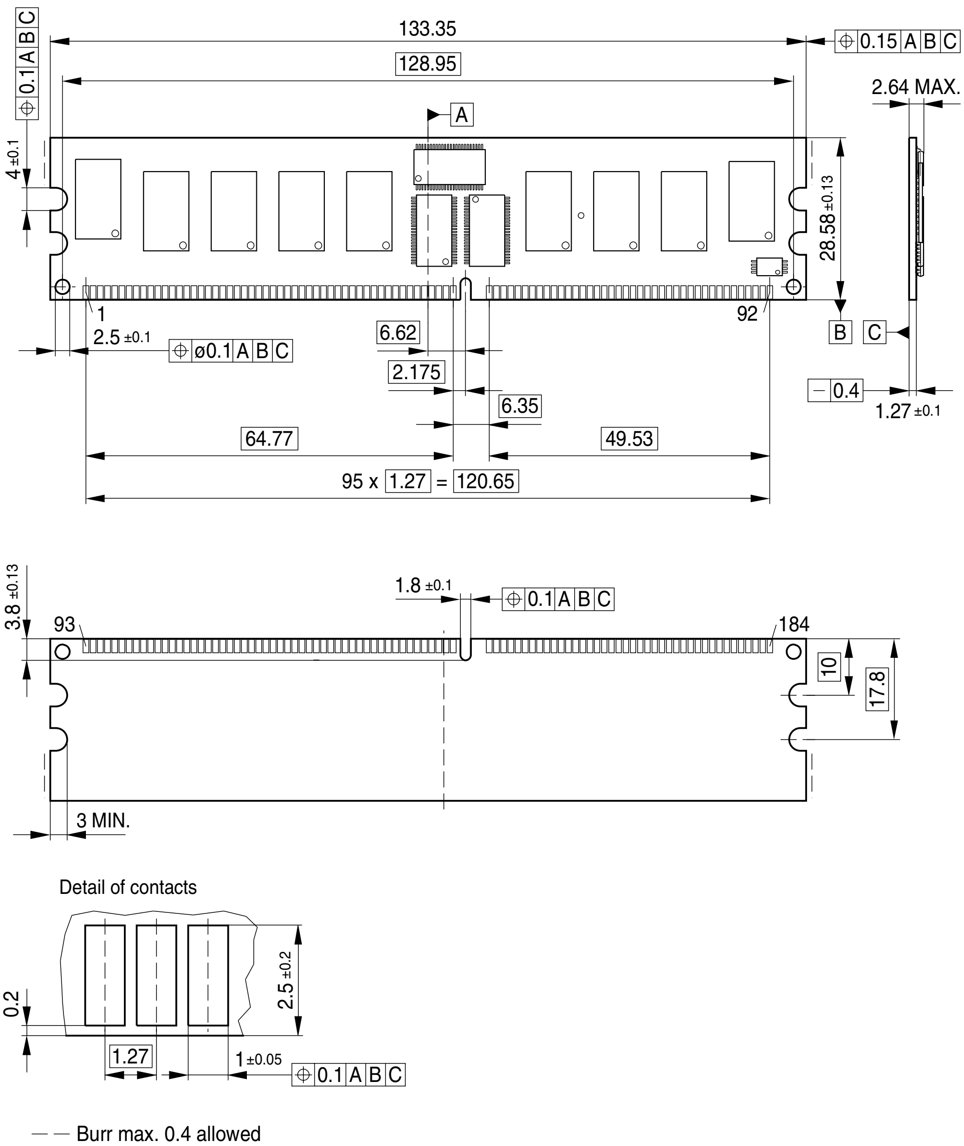
Product Type		**HYS72D128900HBR–6–C**	**HYS72D256920HBR–6–C**
Organization		**1 GByte**	**2 GByte**
		×72	**×72**
		1 Rank (×4)	**2 Ranks (×4)**
Label Code		**PC2700R–25331**	**PC2700R–25331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	00	00
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	00	00
27	t_{RPmin} [ns]	48	48
28	t_{RRDmin} [ns]	30	30
29	t_{RCDmin} [ns]	48	48
30	t_{RASmin} [ns]	2A	2A
31	Module Density per Rank	01	01
32	$t_{AS,}$ t_{CS} [ns]	75	75
33	$t_{AH,}$ t_{CH} [ns]	75	75
34	t_{DS} [ns]	45	45
35	t_{DH} [ns]	45	45
36 - 40	not used	00	00
41	t_{RCmin} [ns]	3C	3C
42	t_{RFCmin} [ns]	48	48
43	t_{CKmax} [ns]	30	30
44	$t_{DQSQmax}$ [ns]	28	28
45	t_{QHSmax} [ns]	50	50
46	not used	00	00
47	DIMM PCB Height	01	01
48 - 61	not used	00	00
62	SPD Revision	10	10
63	Checksum of Byte 0-62	DB	DC
64	Manufacturer’s JEDEC ID Code (1)	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F

Product Type		**HYS72D128900HBR–6–C**	**HYS72D256920HBR–6–C**
Organization		**1 GByte**	**2 GByte**
		×72	**×72**
		1 Rank (×4)	**2 Ranks (×4)**
Label Code		**PC2700R–25331**	**PC2700R–25331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**
67	Manufacturer’s JEDEC ID Code (4)	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Part Number, Char 1	37	37
74	Part Number, Char 2	32	32
75	Part Number, Char 3	44	44
76	Part Number, Char 4	31	32
77	Part Number, Char 5	32	35
78	Part Number, Char 6	38	36
79	Part Number, Char 7	39	39
80	Part Number, Char 8	30	32
81	Part Number, Char 9	30	30
82	Part Number, Char 10	48	48
83	Part Number, Char 11	42	42
84	Part Number, Char 12	52	52
85	Part Number, Char 13	36	36
86	Part Number, Char 14	43	43
87	Part Number, Char 15	20	20
88	Part Number, Char 16	20	20
89	Part Number, Char 17	20	20
90	Part Number, Char 18	20	20
91	Module Revision Code	1x	1x
92	Test Program Revision Code	xx	xx

Product Type		**HYS72D128900HBR–6–C**	**HYS72D256920HBR–6–C**
Organization		**1 GByte**	**2 GByte**
		×72	**×72**
		1 Rank (×4)	**2 Ranks (×4)**
Label Code		**PC2700R–25331**	**PC2700R–25331**
	JEDEC SPD Revision	**Rev 1.0**	**Rev 1.0**
Byte#	**Description**	**HEX**	**HEX**
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx
99 - 127	not used	00	00

5 Package Outlines

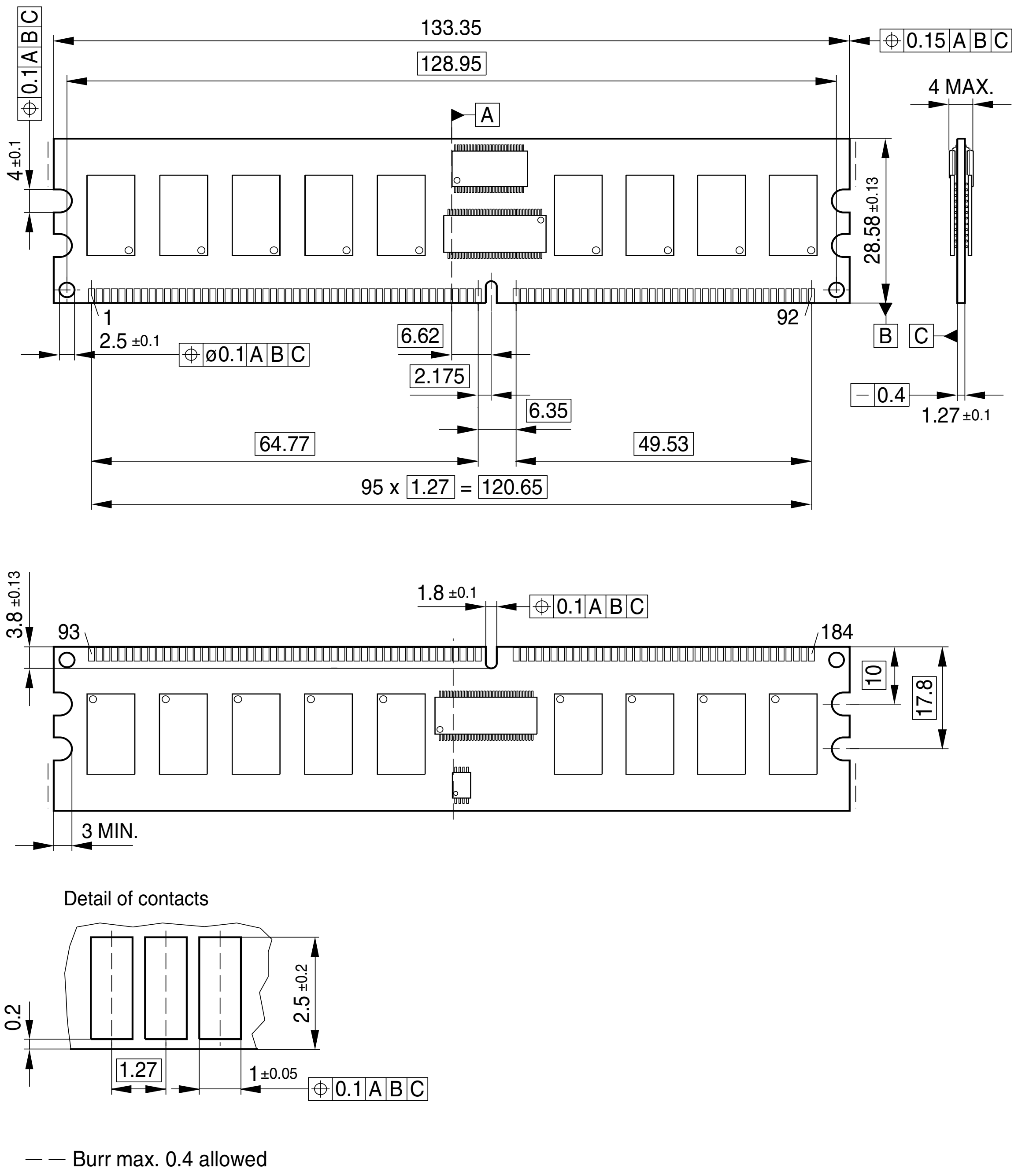
FIGURE 2
Package Outline Raw Card A - L-DIM-184-21



Notes

1. *General tolerances +/- 0.15*
2. *Drawing according to ISO 8015*

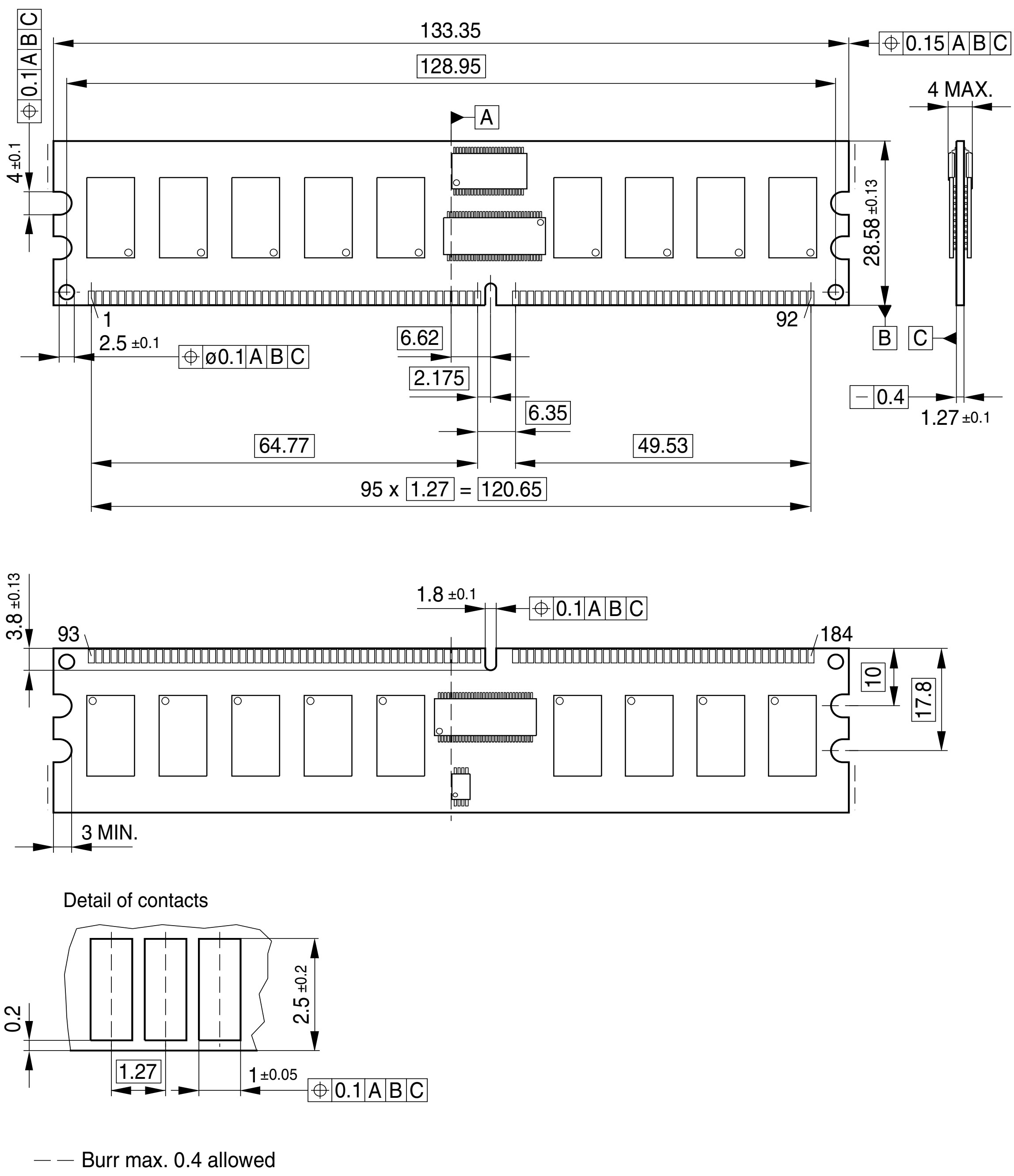
FIGURE 3
Package Outline Raw Card C - L-DIM-184-22



Notes

1. *General tolerances +/- 0.15*
2. *Drawing according to ISO 8015*

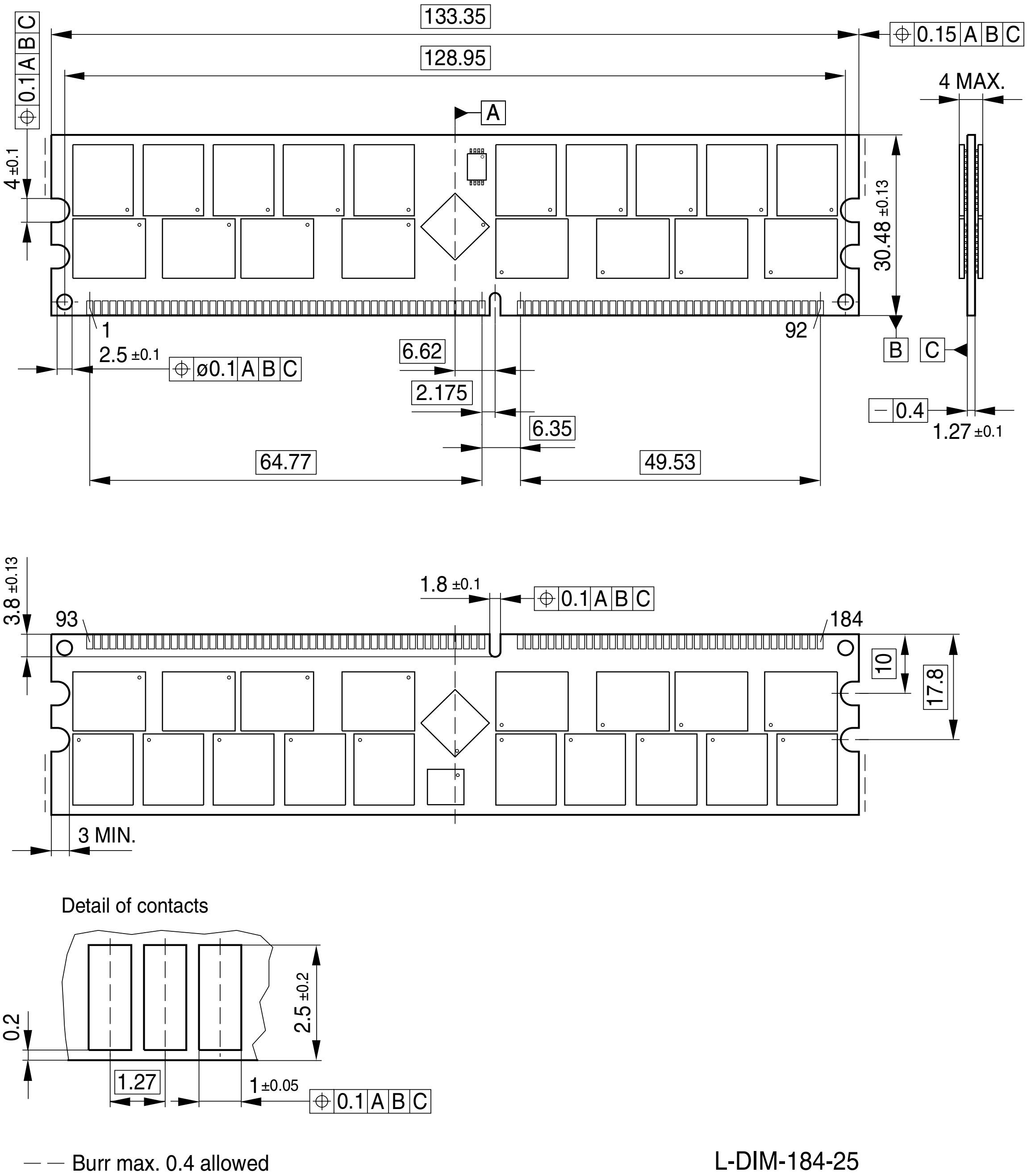
FIGURE 4
Package Outline Raw Card B - L-DIM-184-23



Notes

1. *General tolerances +/- 0.15*
2. *Drawing according to ISO 8015*

FIGURE 5
Package Outline Raw Card F – L-DIM-184-25



Notes

1. *General tolerances +/- 0.15*
2. *Drawing according to ISO 8015*

6 Application Note

Power Up and Power Management on DDR Registered DIMMs

(according to JEDEC ballot JC-42.5 Item 1173)

184-pin Double Data Rate (DDR) Registered DIMMs include two new features to facilitate controlled power-up and to minimize power consumption during low power mode. One feature is externally controlled via a system-generated RESET signal; the second is based on module detection of the input clocks. These enhancements permit the modules to power up with SDRAM outputs in a High-Z state (eliminating risk of high current dissipations and/or dotted I/Os), and result in the powering-down of module support devices (registers and Phase-Locked Loop) when the memory is in Self-Refresh mode.

The new RESET pin controls power dissipation on the module’s registers and ensures that CKE and other SDRAM inputs are maintained at a valid ‘low’ level during power-up and self refresh. When RESET is at a low level, all the register outputs are forced to a low level, and all differential register input receivers are powered down, resulting in very low register power consumption. The $\overline{\text{RESET}}$ pin, located on DIMM tab #10, is driven from the system as an asynchronous signal according to the attached details. Using this function also permits the system and DIMM clocks to be stopped during memory Self Refresh operation, while ensuring that the SDRAMs stay in Self Refresh mode.

TABLE 16
Function for RESET

Register Inputs				Register Outputs[1)]
RESET	CK	$\overline{\text{CK}}$	Data in (D)	Data out (Q)
H	Rising	Falling	H	H
H	Rising	Falling	L	L
H	L or H	L or H	X	Qo
H	High Z	High Z	X	Illegal input conditions
L	X or Hi-Z	X or Hi-Z	X or Hi-Z	L

1) X : Don’t care, Hi-Z : High Impedance, Qo: Data latched at the previous of CK risning and CK falling

As described in the table above, a low on the $\overline{\text{RESET}}$ input ensures that the Clock Enable (CKE) signal(s) are maintained low at the SDRAM pins (CKE being one of the 'Q' signals at the register output). Holding CKE low maintains a high impedance state on the SDRAM DQ, DQS and DM outputs — where they will remain until activated by a valid ‘read’ cycle. CKE low also maintains SDRAMs in Self Refresh mode when applicable.

The DDR PLL devices automatically detect clock activity above 20MHz. When an input clock frequency of 20MHz or greater is detected, the PLL begins operation and initiates clock frequency lock (the minimum operating frequency at which all specifications will be met is 95MHz). If the clock input frequency drops below 20MHz (actual detect frequency will vary by vendor), the PLL VCO (Voltage Controlled Oscillator) is stopped, outputs are made High-Z, and the differential inputs are powered down — resulting in a total PLL current consumption of less than 1mA. Use of this low power PLL function makes the use of the PLL $\overline{\text{RESET}}$ (or G pin) unnecessary, and it is tied inactive on the DIMM.

This application note describes the required and optional system sequences associated with the DDR Registered DIMM '$\overline{\text{RESET}}$' function. It is important to note that all references to CKE refer to both CKE0 and CKE1 for a 2-bank DIMM. Because $\overline{\text{RESET}}$ applies to all DIMM register devices, it is therefore not possible to uniquely control CKE to one physical DIMM bank through the use of the $\overline{\text{RESET}}$ pin.

Power-Up Sequence with RESET — Required

1. The system sets RESET at a valid low level. This is the preferred default state during power-up. This input condition forces all register outputs to a low state independent of the condition on the register inputs (data and clock), ensuring that CKE is at a stable low-level at the DDR SDRAMs.
2. The power supplies should be initialized according to the JEDEC-approved initialization sequence for DDR SDRAMs.
3. Stabilization of Clocks to the SDRAM The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches 20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds. When a stable clock is present at the SDRAM input (driven from the PLL), the DDR SDRAM requires 200 µsec prior to SDRAM operation.
4. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector). CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the JEDEC initialization sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
5. The system switches RESET to a logic 'high' level. The SDRAM is now functional and prepared to receive commands. Since the RESET signal is asynchronous, setting the RESET timing in relation to a specific clock edge is not required (during this period, register inputs must remain stable).
6. The system must maintain stable register inputs until normal register operation is attained. The registers have an activation time that allows their clock receivers, data input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in step 5. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of RESET from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
7. The system can begin the JEDEC-defined DDR SDRAM power-up sequence (according to the JEDEC-pproved initialization sequence).

Self Refresh Entry (RESET low, clocks powered off) — Optional

Self Refresh can be used to retain data in DDR SDRAM DIMMs even if the rest of the system is powered down and the clocks are off. This mode allows the DDR SDRAMs on the DIMM to retain data without external clocking. Self Refresh mode is an ideal time to utilize the RESET pin, as this can reduce register power consumption (RESET low deactivates register CK and CK, data input receivers, and data output drivers).

- The system applies Self Refresh entry command. (CKE→Low, CS→Low, RAS → Low, CAS→ Low, WE→ High)

Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don't Cares— with the exception of CKE.

- The system sets RESET at a valid low level. This input condition forces all register outputs to a low state, independent of the condition on the registerm inputs (data and clock), and ensures that CKE, and all other control and address signals, are a stable low-level at the DDR SDRAMs. Since the RESET signal is asynchronous, setting the RESET timing in relation to a specific clock edge is not required.
- The system turns off clock inputs to the DIMM. (Optional) a. In order to reduce DIMM PLL current, the clock inputs to the DIMM are turned off, resulting in High-Z clock inputs to both the SDRAMs and the registers. This must be done after the RESET deactivate time of the register (t (INACT)). The deactivate time defines the time in which the clocks and the control and address signals must maintain valid levels after RESET low has been applied and is specified in the register and DIMM documentation. b. The system may release DIMM address and control inputs to High-Z. This can be done after the RESET deactivate time of the register. The deactivate time defines the time in which the clocks and the control and the address signals must maintain valid levels after RESET low has been applied. It is highly recommended that CKE continue to remain low during this operation.

- The DIMM is in lowest power Self Refresh mode.

Self Refresh Exit (RESET low, clocks powered off) — Optional

1. Stabilization of Clocks to the SDRAM. The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches ~20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds.
2. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector). CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM ‘NOP’ command (with CKE low), as this is the first command defined by the JEDEC Self Refresh Exit sequence (ideally this would be a ‘NOP Deselect’ command). A second option is to apply low levels on all of the register inputs, to be consistent with the state of the register outputs.
3. The system switches $\overline{\text{RESET}}$ to a logic ‘high’ level. The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, $\overline{\text{RESET}}$ timing relationship to a specific clock edge is not required (during this period, register inputs must remain stable).
4. The system must maintain stable register inputs until normal register operation is attained. The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 2. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of $\overline{\text{RESET}}$ from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
5. System can begin the JEDEC-defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks running) — Optional

Although keeping the clocks running increases power consumption from the on-DIMM PLL during self refresh, this is an alternate operating mode for these DIMMs.

1. System enters Self Refresh entry command. (CKE→ Low, $\overline{\text{CS}}$→ Low, $\overline{\text{RAS}}$→ Low, $\overline{\text{CAS}}$→ Low, $\overline{\text{WE}}$→ High)

Note: *The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don’t Cares — with the exception of CKE.*

- The system sets $\overline{\text{RESET}}$ at a valid low level. This input condition forces all register outputs to a low state, independent of the condition on the data and clock register inputs, and ensures that CKE is a stable low-level at the DDR SDRAMs.
- The system may release DIMM address and control inputs to High-Z. This can be done after the $\overline{\text{RESET}}$ deactivate time of the register (t (INACT)). The deactivate time describes the time in which the clocks and the control and the address signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied. It is highly recommended that CKE continue to remain low during the operation.
- The DIMM is in a low power, Self Refresh mode.

Self Refresh Exit ($\overline{\text{RESET}}$ low, clocks running) — Optional

1. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector). CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM ‘NOP’ command (with CKE low), as this is the first command defined by the Self Refresh Exit sequence (ideally this would be a ‘NOP Deselect’ command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.

2. The system switches $\overline{\text{RESET}}$ to a logic 'high' level. The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, it does not need to be tied to a particular clock edge (during this period, register inputs must continue to remain stable).
3. The system must maintain stable register inputs until normal register operation is attained. The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 1. It is also a functional requirement that the registers maintain a low state at the CKE outputs in order to guarantee that the DDR SDRAMs continue to receive a low level on CKE. This activation time, from asynchronous switching of $\overline{\text{RESET}}$ from low to high, until the registers are stable and ready to accept an input signal, is t (ACT) as specified in the register and DIMM documentation.
4. The system can begin JEDEC defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry/Exit ($\overline{\text{RESET}}$ high, clocks running) — Optional

As this sequence does not involve the use of the $\overline{\text{RESET}}$ function, the JEDEC standard SDRAM specification explains in detail the method for entering and exiting Self Refresh for this case.

Self Refresh Entry ($\overline{\text{RESET}}$ high, clocks powered off) — Not Permissible

In order to maintain a valid low level on the register output, it is required that either the clocks be running and the system drive a low level on CKE, or the clocks are powered off and $\overline{\text{RESET}}$ is asserted low according to the sequence defined in this application note. In the case where $\overline{\text{RESET}}$ remains high and the clocks are powered off, the PLL drives a High-Z clock input into the register clock input. Without the low level on $\overline{\text{RESET}}$ an unknown DIMM state will result.

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