

256K x 16-Bit EDO-DRAM

HYB 514175BJ -50/-55/-60

256K x 16-Bit EDO-DRAM

HYB 514175BJL-50/-55/-60

(Low power version with Self Refresh)

Advanced Information

- 262 144 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
- $\overline{\text{RAS}}$ access time:
 - 50 ns (-50 version)
 - 55 ns (-55 version)
 - 60 ns (-60 version)
- $\overline{\text{CAS}}$ access time:
 - 13ns (-50 & -55 version)
 - 15 ns (-60 version)
- Cycle time:
 - 89 ns (-50 version)
 - 94 ns (-55 version)
 - 104 ns (-60 version)
- Hype page mode (EDO) cycle time
 - 20 ns (-50 & -55 version)
 - 25 ns (-60 version)
- High data rate
 - 50 MHz (-50 & -55 version)
 - 40 MHz (-60 version)
- Single + 5 V ($\pm 10\%$) supply with a built-in VBB generator
- Low Power dissipation
 - max. 1100 mW active (-50 version)
 - max. 1045 mW active (-55 version)
 - max. 935 mW active (-60 version)
- Standby power dissipation
 - 11 mW standby (TTL)
 - 5.5 mW max. standby (CMOS)
 - 1.1 mW max. standby (CMOS) for Low Power Version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write, CAS-before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh, hidden-refresh and hyper page (EDO) mode capability
- 2 $\overline{\text{CAS}}$ / 1 $\overline{\text{WE}}$ control
- Self Refresh (L-Version)
- All inputs and outputs TTL-compatible
- 512 refresh cycles / 16 ms
- 512 refresh cycles / 128 ms
- Low Power Version only
- Plastic Packages:
 - P-SOJ-40-1 400mil width

The HYB 514175BJ/BJL is the new generation dynamic RAM organized as 262 144 words by 16-bit. The HYB 514175BJ/BJL utilizes CMOS silicon gate process as well as advanced circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514175BJ/BJL to be packed in a standard plastic 400mil wide P-SOJ-40-1 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include Self Refresh (L-Version), single + 5 V ($\pm 10\%$) power supply, direct interfacing with high performance logic device families such as Schottky TTL.

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Ordering Information

Type	Ordering Code	Package	Description
HYB 514175BJ-50	Q67100 - Q2072	P-SOJ-40-1	50 ns 256 K x 16 EDO-DRAM
HYB 514175BJ-55	Q67100 - Q2100	P-SOJ-40-1	55 ns 256 K x 16 EDO-DRAM
HYB 514175BJ-60	Q67100 - Q2073	P-SOJ-40-1	60 ns 256 K x 16 EDO-DRAM
HYB 514175BJL-50	on request	P-SOJ-40-1	50 ns 256 K x 16 EDO- DRAM
HYB 514175BJL-55	on request	P-SOJ-40-1	55 ns 256 K x 16 EDO- DRAM
HYB 514175BJL-60	on request	P-SOJ-40-1	60 ns 256 K x 16 EDO-DRAM

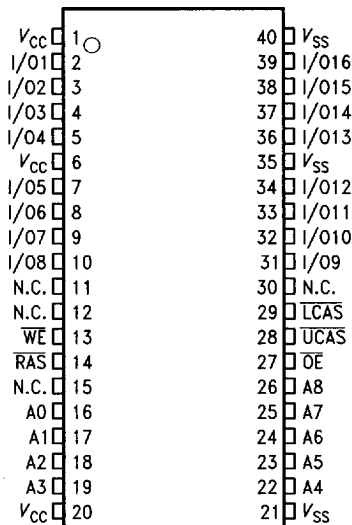
Truth Table

RAS	LCAS	UCAS	WE	OE	I/O1-I/O8	I/O9-I/O16	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	

Pin Names

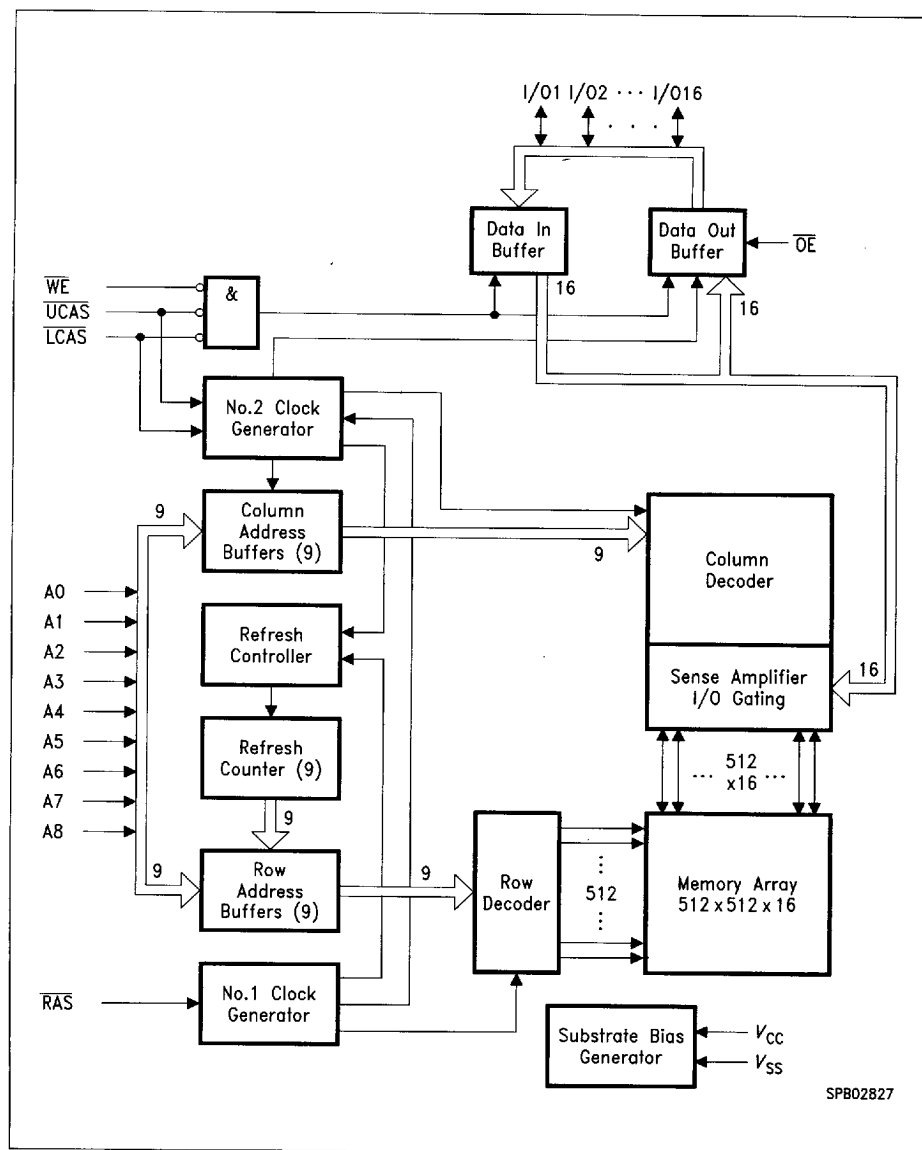
A0-A8	Address Inputs
RAS	Row Address Strobe
UCAS, LCAS	Column Address Strobe
WE	Read/Write Input
OE	Output Enable
I/O1 – I/O16	Data Input/Output
V _{CC}	Power Supply (+ 5 V)
V _{SS}	Ground (0 V)
N.C.	No Connection

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Pin Configuration
(top view)**P-SOJ-40-1**

SPP02811

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Block Diagram

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Absolute Maximum Ratings

Operating temperature range	0 to + 70 °C
Storage temperature range	- 55 to + 150 °C
Input/output voltage	- 1 to + 7 V
Power supply voltage	- 1 to + 7 V
Data out current (short circuit)	50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{CC} = 5$ V ± 10 %, $t_T = 2$ ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	$V_{CC} + 0.5$	V	1
Input low voltage	V_{IL}	- 1.0	0.8	V	1
Output high voltage ($I_{OUT} = - 5.0$ mA)	V_{OH}	2.4	-	V	1
Output low voltage ($I_{OUT} = 4.2$ mA)	V_{OL}	-	0.4	V	1
Input leakage current, any input (0 V $< V_{IN} < 7$ V, all other inputs = 0 V)	I_{IL}	- 10	10	μ A	1
Output leakage current (DO is disabled, 0 V $< V_{OUT} < V_{CC}$)	I_{OL}	- 10	10	μ A	1
Average V_{CC} supply current -50 version -55 version -60 version	I_{CC1}	-	200 190 170	mA	2, 3, 4
Standby V_{CC} supply current (RAS = LCAS = UCAS = WE = V_{IH})	I_{CC2}	-	2	mA	-
Average V_{CC} supply current during RAS-only refresh cycles -50 version -55 version -60 version	I_{CC3}	-	200 190 170	mA	2, 4

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DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during hyper page mode (EDO) operation: -50 version -55 version -60 version	I_{CC4}	—	190 180 170	mA	2, 3, 4
Standby V_{CC} supply current ($\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{WE} = V_{CC} - 0.2\text{ V}$)	I_{CC5}	—	1	mA	1
Average V_{CC} supply current during CAS-before-RAS refresh mode: -50 version -55 version -60 version	I_{CC6}	—	200 190 170	mA	2, 4
Standby V_{CC} current (L-version) ($\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{WE} = V_{CC} - 0.2\text{ V}$)	I_{CC5}	—	200	μA	
Self Refresh Current (L-version) ($\overline{RAS}, \overline{LCAS}, \overline{UCAS} = 0.2\text{ V}$ $A0 - A8 = V_{CC} - 0.2\text{ V}$ or 0.2 V)	I_{CCS}	—	250	μA	

Capacitance

$T_A = 0$ to 70°C ; $V_{CC} = 5\text{ V} \pm 10\%$, $f = 1\text{ MHz}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A8)	C_{I1}	—	5	pF
Input capacitance ($\overline{RAS}, \overline{UCAS}, \overline{LCAS}, \overline{WE}, \overline{OE}$)	C_{I2}	—	7	pF
Output capacitance (I/O1 to I/O16)	C_{I0}	—	7	pF

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AC Characteristics ^{5) 6)} $T_A = 0$ to $70\text{ }^{\circ}\text{C}$; $V_{SS} = 0\text{ V}$; $V_{CC} = 5\text{ V} \pm 10\%$, $t_T = 2\text{ ns}$

Parameter	Symbol	Limit Values						Unit	Note
		-50		-55		-60			
		min.	max.	min.	max.	min.	max.		

Common Parameters

Random read or write cycle time	t_{RC}	89	—	94	—	104	—	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	35	—	35	—	40	—	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	50	10k	55	10k	60	10k	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	8	10k	8	10k	10	10k	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	8	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	8	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delaytime	t_{RCD}	12	37	12	43	14	45	ns	
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	10	25	10	30	12	30	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	13	—	13	—	15	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	40	—	45	—	50	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
Transition time(rise and fall)	t_T	1	50	1	50	1	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	55	—	60	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	13	—	15	ns	8, 9
Access time from column address	t_{AA}	—	25	—	25	—	30	ns	8, 10
$\overline{\text{OE}}$ access time	t_{OEA}	—	13	—	13	—	15	ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	—	25	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	11

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Parameter	Symbol	Limit Values						Unit	Note
		-50		-55		-60			
		min.	max.	min.	max.	min.	max.		
Read command hold time ref. to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	11
$\overline{\text{CAS}}$ to output inlow-Z	t_{CLZ}	0	—	0	—	0	—	ns	8
Output buffer turn-off delay from $\overline{\text{CAS}}$	t_{OFF}	0	13	0	13	0	15	ns	12
Output buffer turn-off delay from $\overline{\text{OE}}$	t_{OEZ}	0	13	0	13	0	15	ns	12
Data to $\overline{\text{OE}}$ low delay	t_{DZO}	0	—	0	—	0	—	ns	13
$\overline{\text{CAS}}$ high to data delay	t_{CDD}	10	—	10	—	13	—	ns	14
$\overline{\text{OE}}$ high to data delay	t_{ODD}	10	—	10	—	13	—	ns	14

Write Cycle

Write command hold time	t_{WCH}	8	—	8	—	10	—	ns	
Write command pulse width	t_{WP}	8	—	8	—	10	—	ns	
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	15
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	13	—	13	—	15	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	13	—	13	—	15	—	ns	
Data setup time	t_{DS}	0	—	0	—	0	—	ns	16
Data hold time	t_{DH}	8	—	8	—	10	—	ns	16
Data to $\overline{\text{CAS}}$ low delay	t_{DZC}	0	—	0	—	0	—	ns	13

Read-modify-Write Cycle

Read-write cycle time	t_{RWC}	118	—	122	—	138	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	64	—	69	—	77	—	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	27	—	27	—	32	—	ns	15
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	39	—	39	—	47	—	ns	15
$\overline{\text{OE}}$ command hold time	t_{OEH}	10	—	10	—	13	—	ns	

Hyper Page Mode (EDO) Cycle

Hyper page mode cycle time	t_{HPC}	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	8	—	8	—	10	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}	—	27	—	27	—	32	ns	7

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Parameter	Symbol	Limit Values						Unit	Note
		-50		-55		-60			
		min.	max.	min.	max.	min.	max.		
Output data hold time	t_{COH}	5	—	5	—	5	—	ns	
RAS pulse width in hyper page mode	t_{RAS}	50	200k	55	200k	60	200k	ns	
RAS hold time from CAS precharge	t_{RHCP}	27	—	27	—	32	—	ns	

Hyper Page Mode (EDO) Read-Modify-Write Cycle

Hyper page mode read/write cycle time	t_{PRWC}	58	—	58	—	68	—	ns	
CAS precharge to WE delay time	t_{CPWD}	41	—	41	—	49	—	ns	

CAS before RAS Refresh Cycle

CAS setup time	t_{CSR}	5	—	5	—	5	—	ns	
CAS hold time	t_{CHR}	10	—	10	—	10	—	ns	
RAS to CAS precharge time	t_{RPC}	5	—	5	—	5	—	ns	
Write to RAS precharge time	t_{WRP}	10	—	10	—	10	—	ns	
Write to RAS hold time	t_{WRH}	10	—	10	—	10	—	ns	

CAS-before-RAS Counter Test Cycle

CAS precharge time	t_{CPT}	35	—	35	—	40	—	ns	
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Self Refresh Cycle (L-Version only)

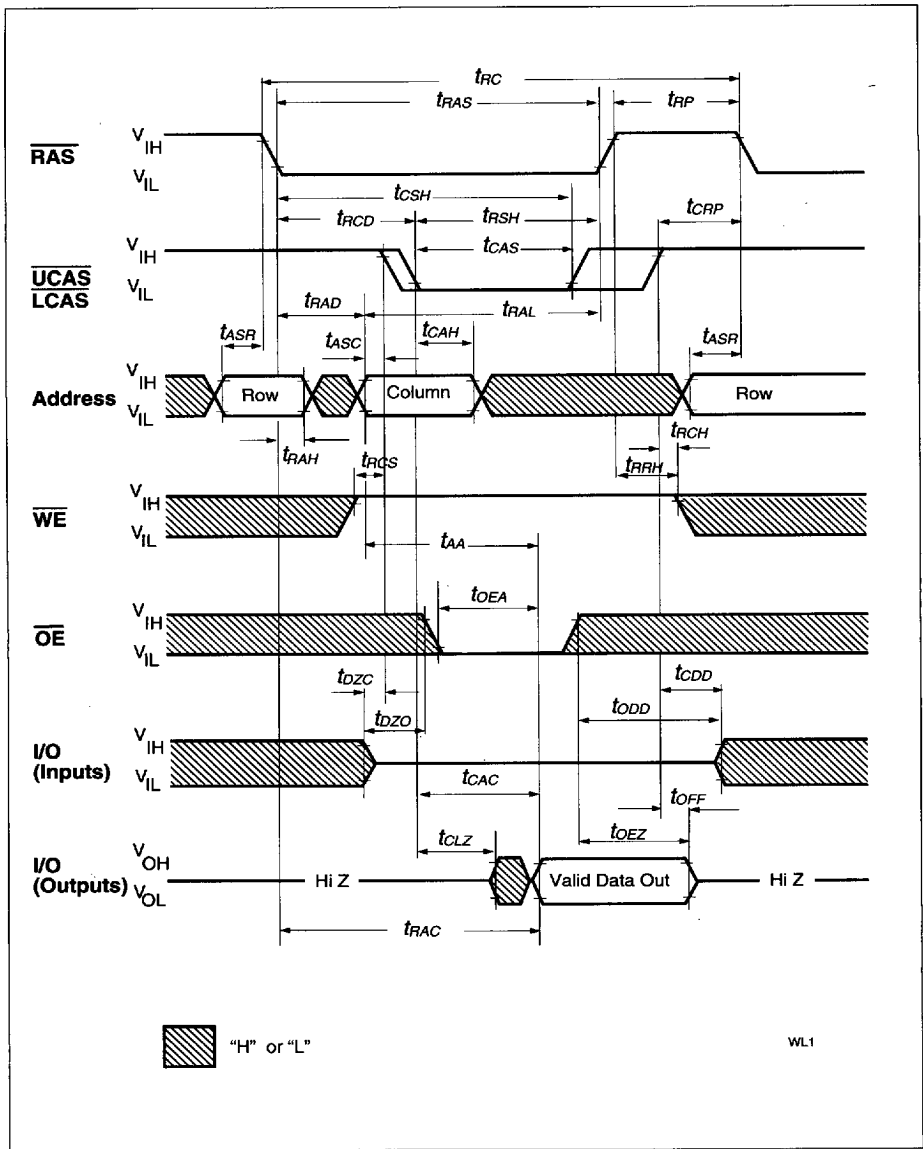
RAS pulse width	t_{RASS}	100	—	100	—	100	—	μs	
RAS precharge time	t_{RPS}	95	—	110	—	110	—	ns	
CAS hold time	t_{CHS}	— 50	—	— 50	—	— 50	—	ns	

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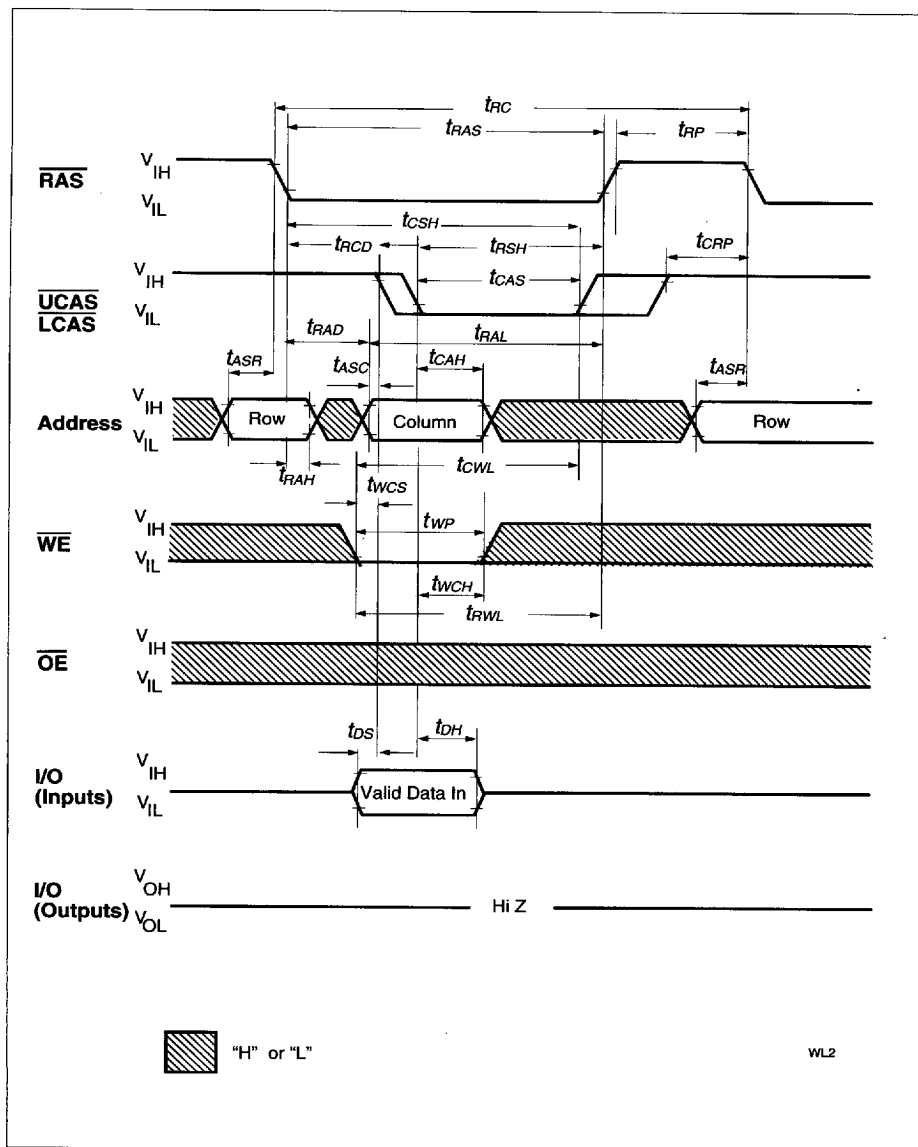
Notes:

- 1) All voltages are referenced to V_{SS} .
- 2) I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate.
- 3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while $RAS = V_{il}$. In case of I_{CC4} it can be changed once or less during a hyper page mode (EDO) cycle.
- 5) An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
- 6) AC measurements assume $t_T = 2$ ns.
- 7) $V_{IH (min.)}$ and $V_{IL (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
- 8) Measured with the specified current load and 100 pF at $V_{ol} = 0.8$ V and $V_{oh} = 2.0$ V. Access time is determined by the latter of t_{RAC} , t_{CAC} , t_{AA} , t_{CPA} , t_{OEA} . t_{CAC} is measured from tristate.
- 9) Operation within the $t_{RCD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RCD (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD (max.)}$ limit, then access time is controlled by t_{CAC} .
- 10) Operation within the $t_{RAD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RAD (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD (max.)}$ limit, then access time is controlled by t_{AA} .
- 11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 12) $t_{OFF (max.)}$, $t_{OEZ (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of RAS or CAS, whichever occurs last.
- 13) Either t_{DZC} or t_{DZO} must be satisfied.
- 14) Either t_{CDD} or t_{ODD} must be satisfied.
- 15) t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD (min.)}$, $t_{CWD} > t_{CWD (min.)}$ and $t_{AWD} > t_{AWD (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
- 16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

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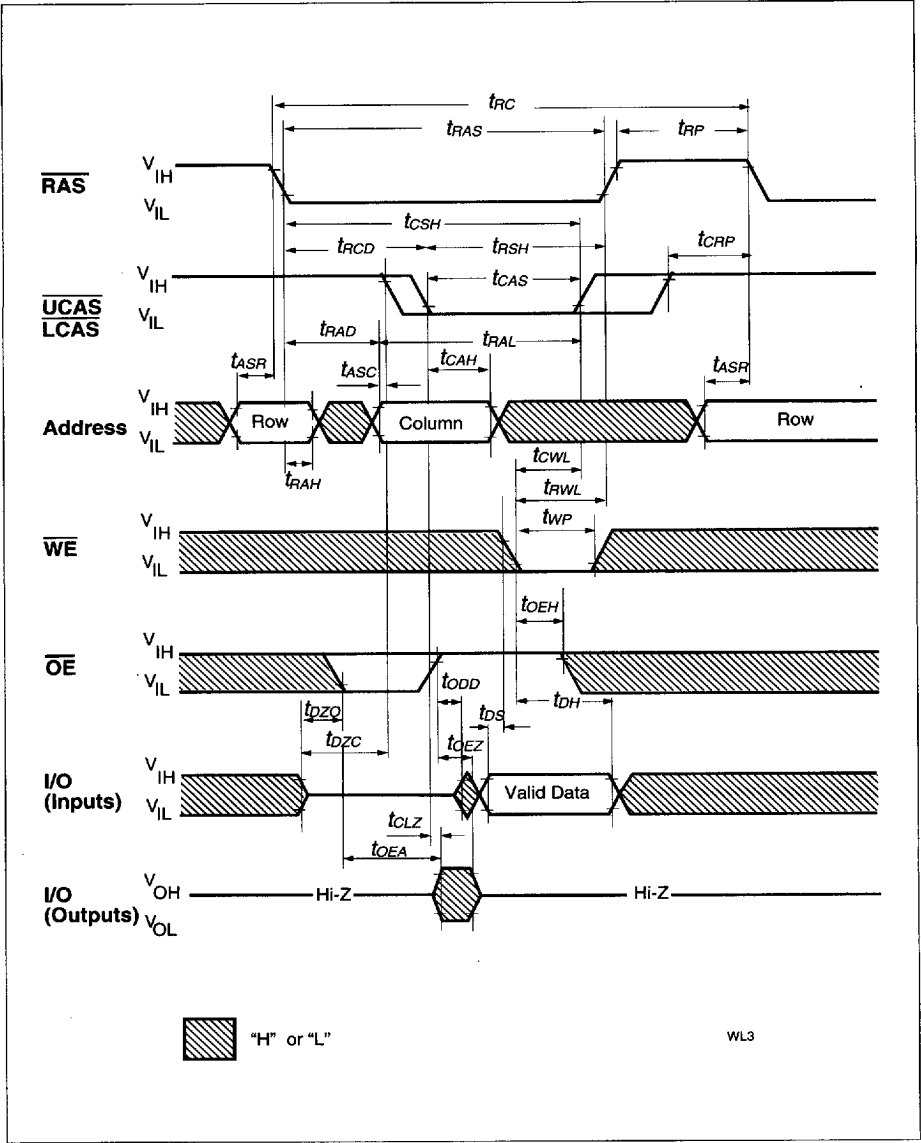


Read Cycle



Write Cycle (Early Write)

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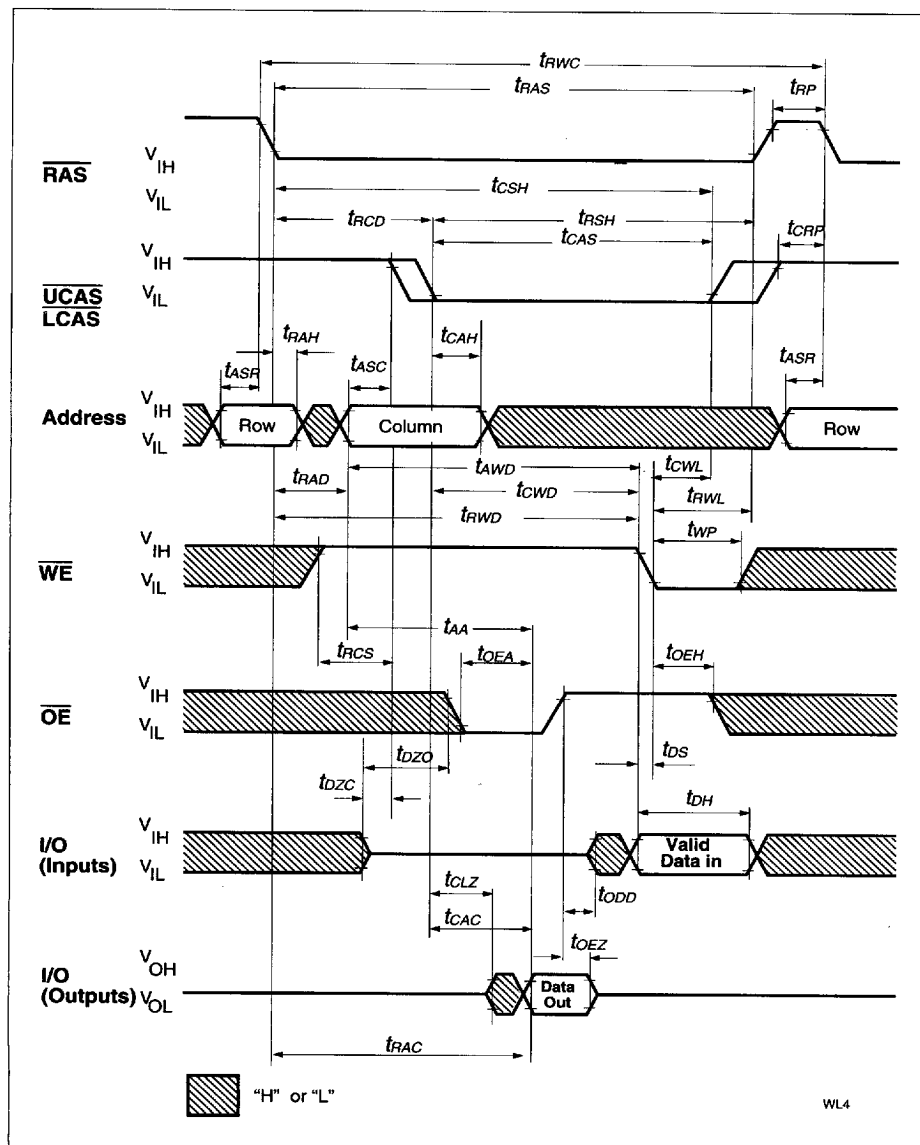


Write Cycle ($\overline{OE}$ Controlled Write)

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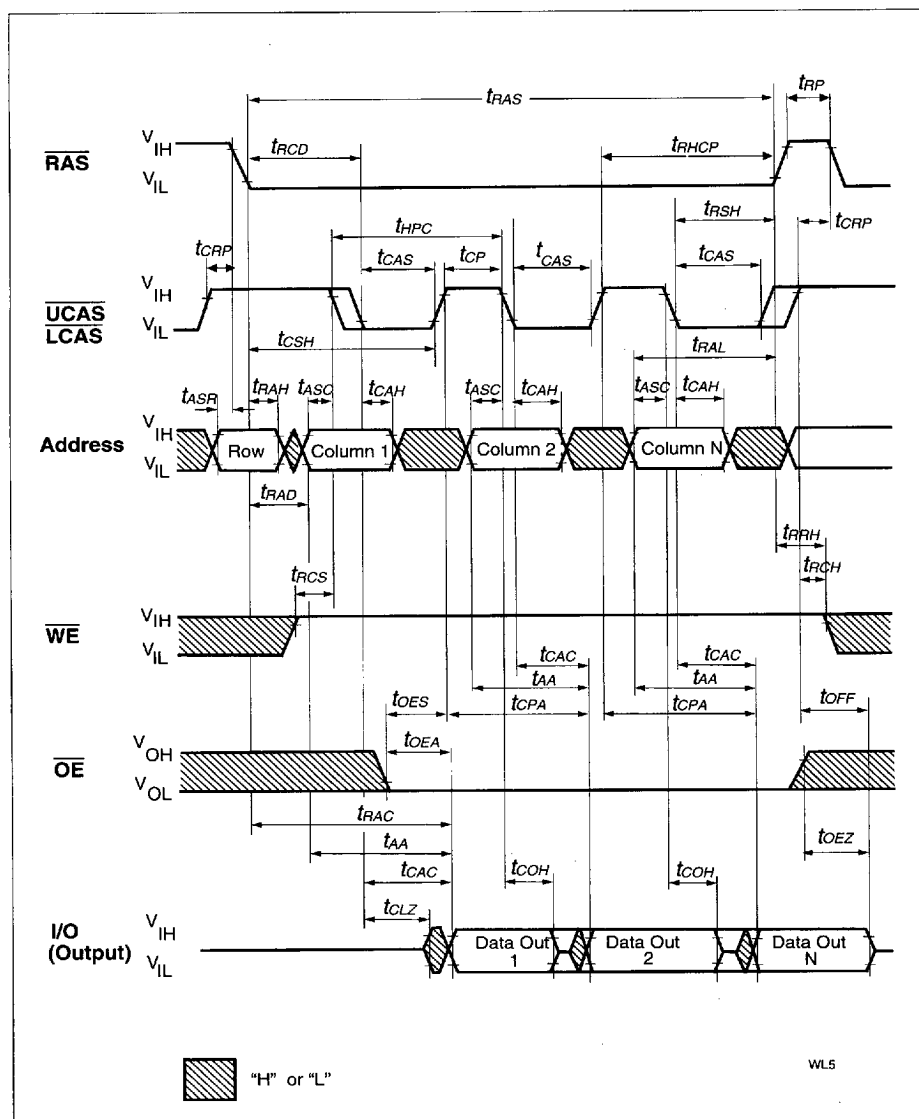
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Read-Write (Read-Modify-Write) Cycle

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Hyper Page Mode (EDO) Read Cycle

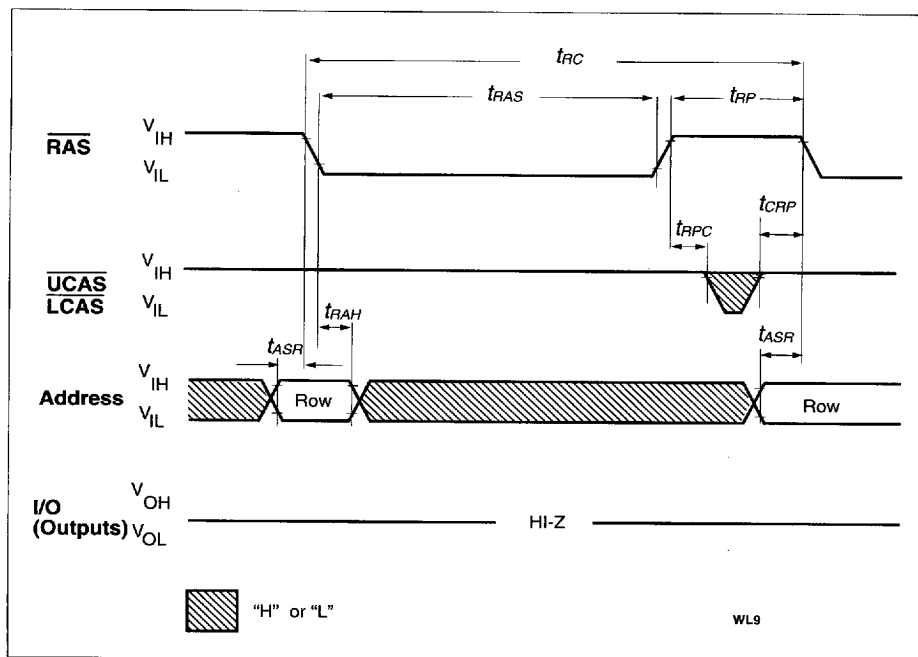
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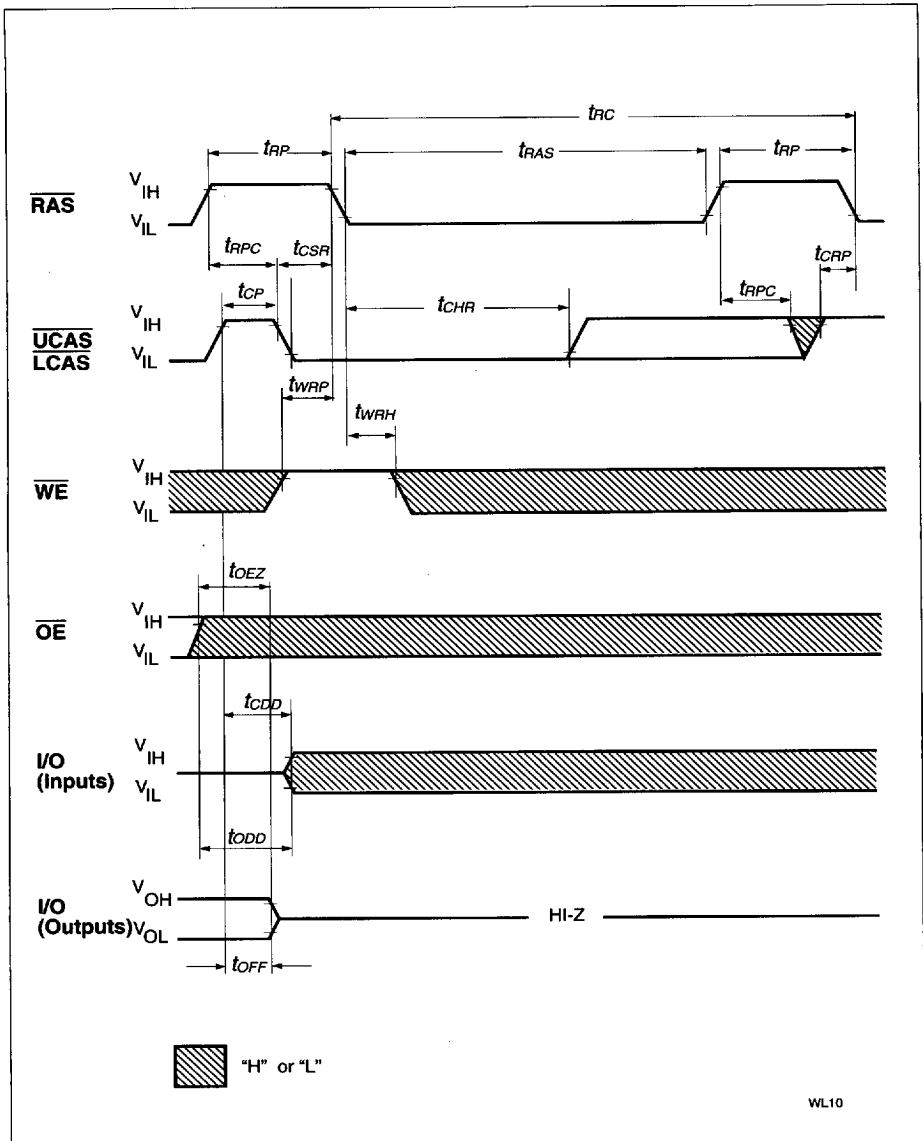


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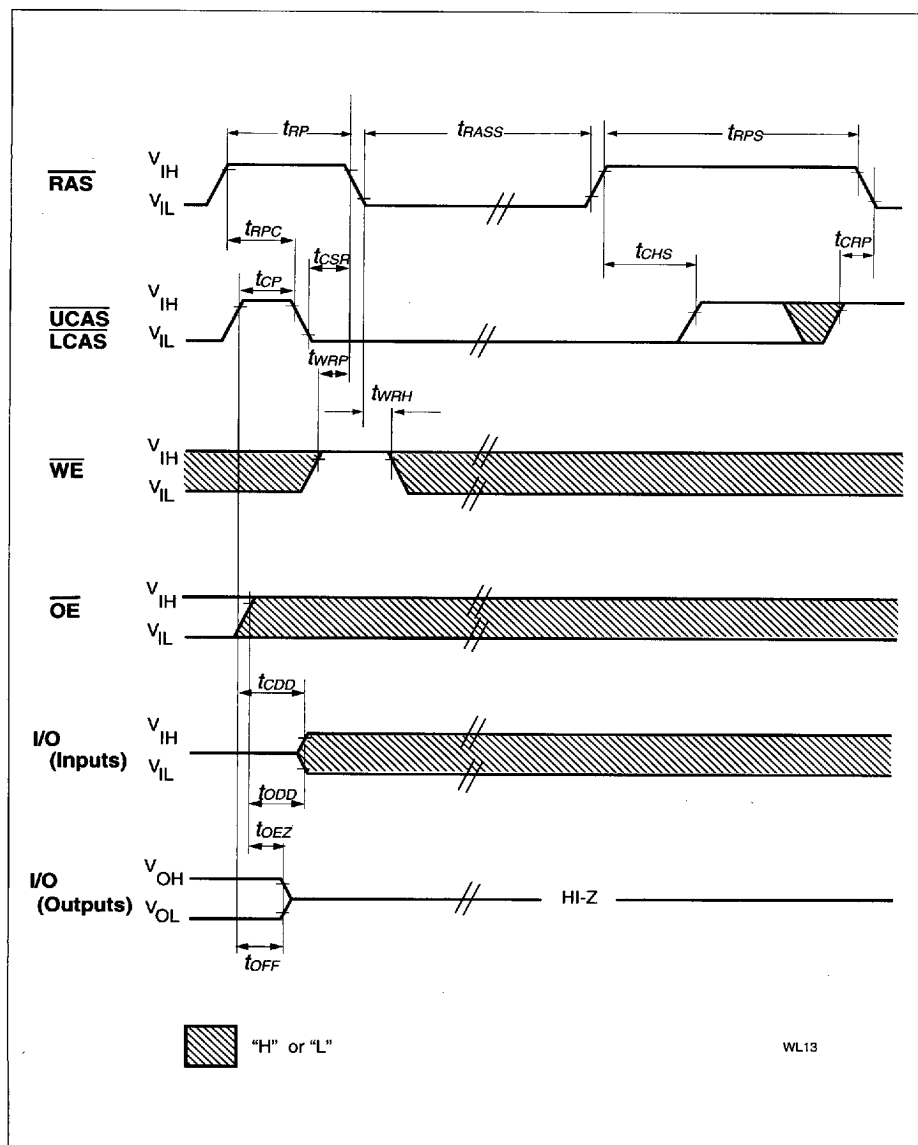
RAS-Only Refresh Cycle

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CAS-Before-RAS Refresh Cycle

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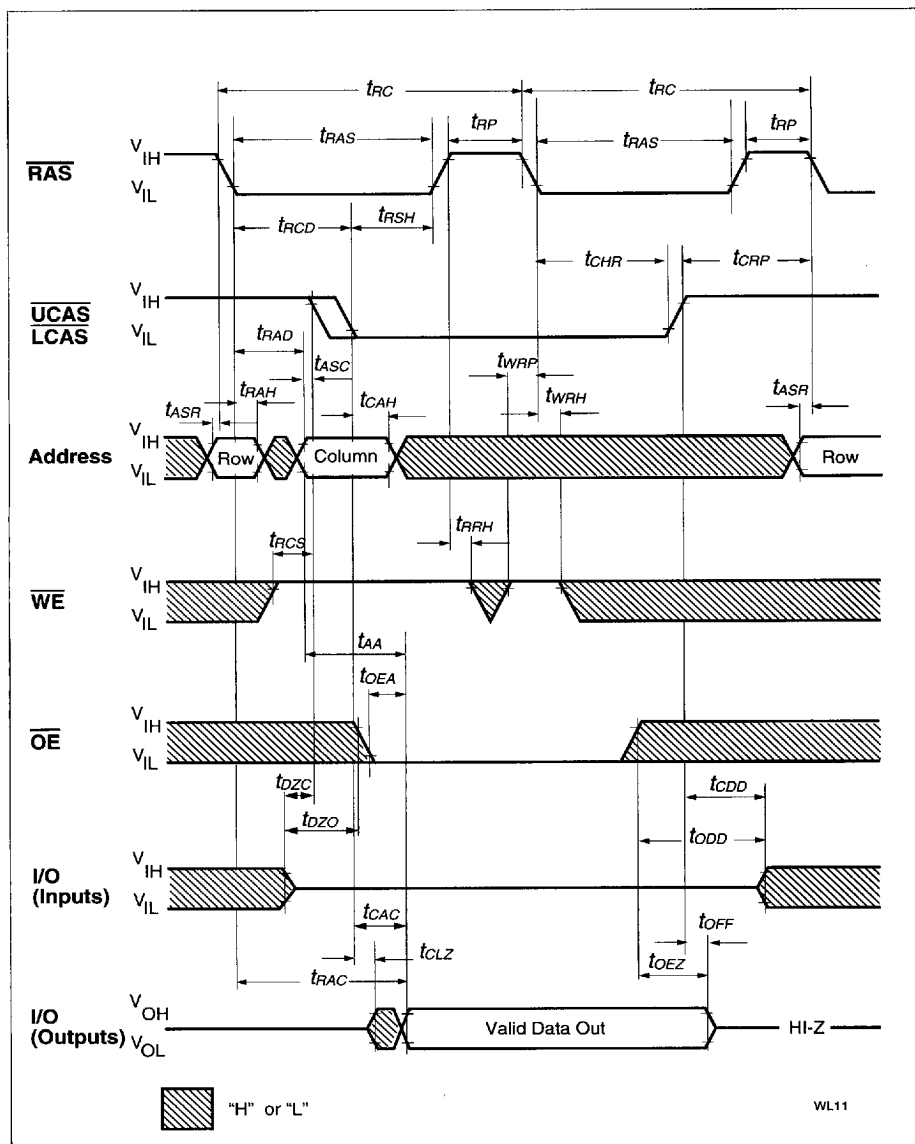


$\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle (L-version only)

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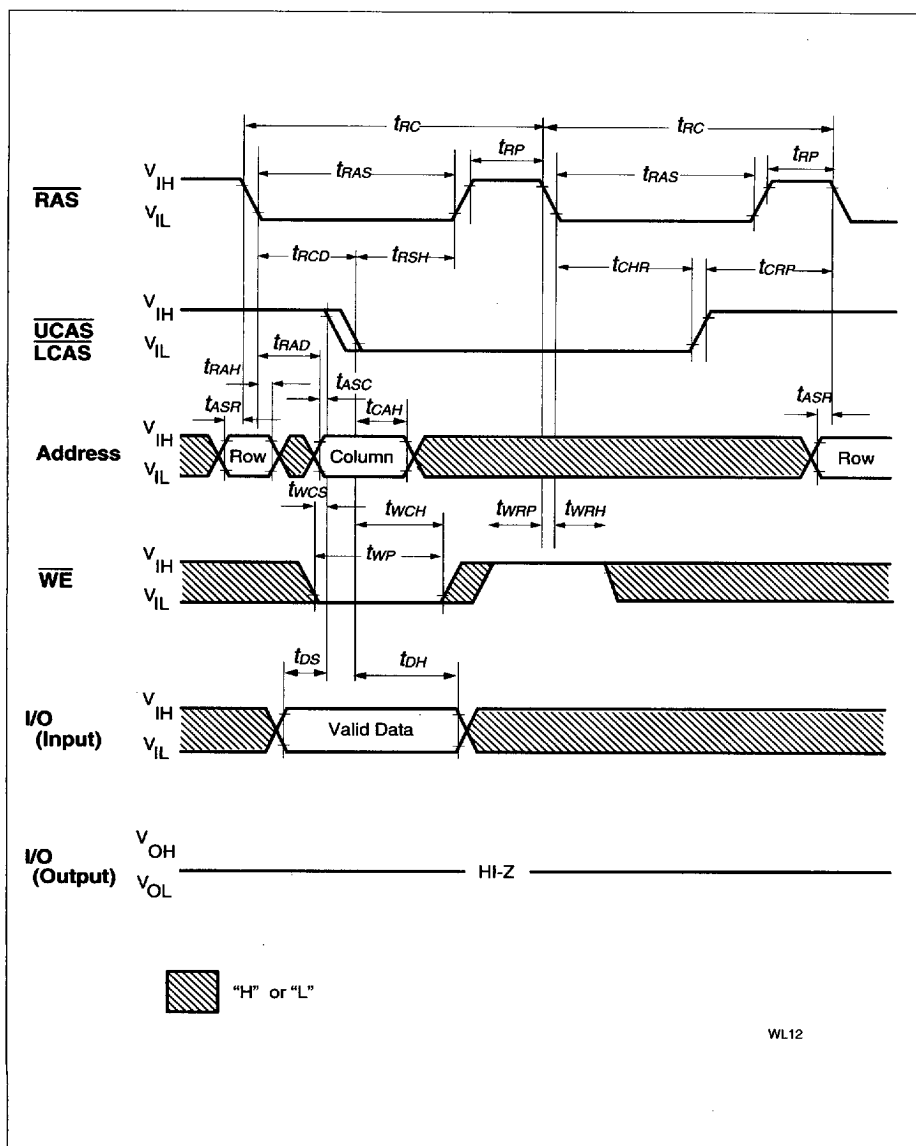
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Hidden Refresh Cycle (Read)

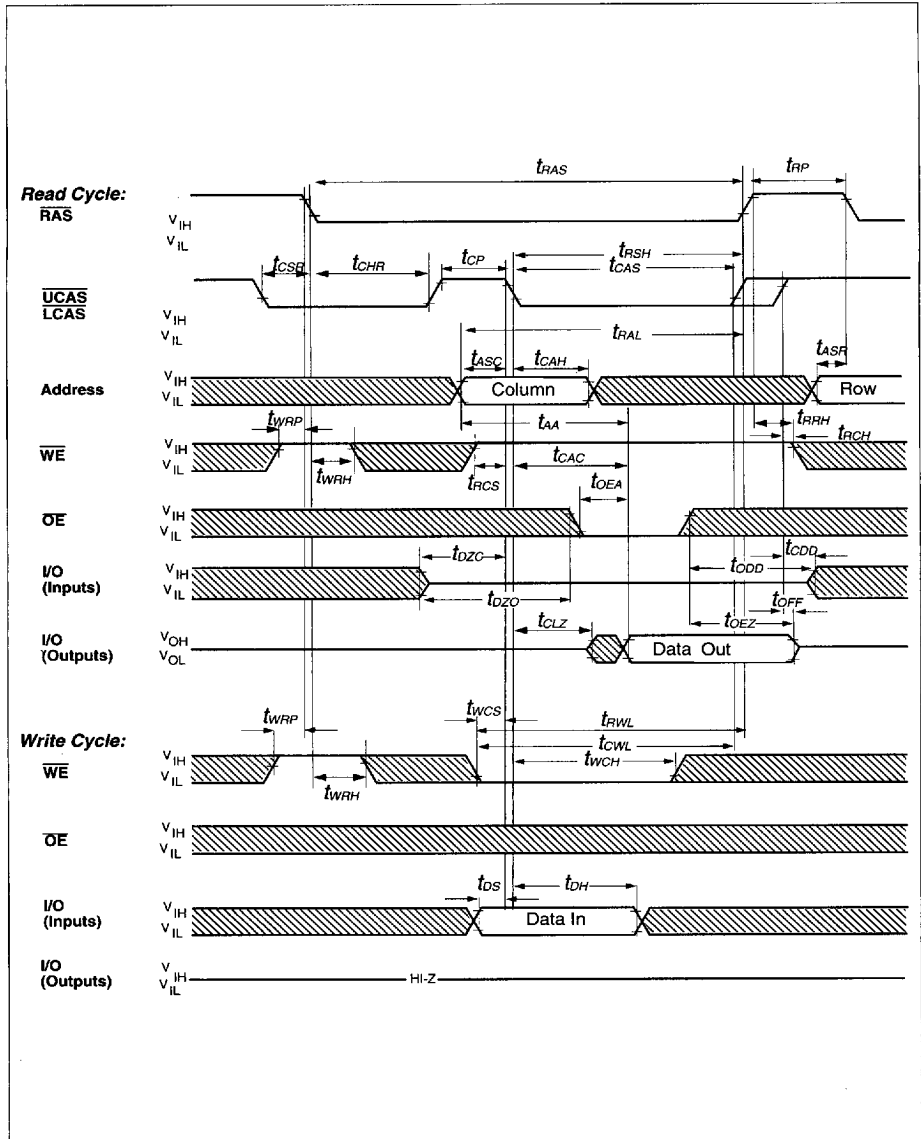
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WL12

Hidden Refresh Cycle (Early Write)

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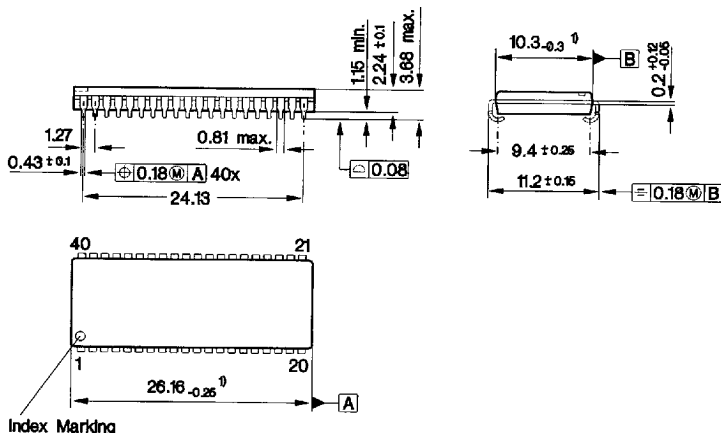
CAS-Before-RAS Refresh Counter Test Cycle

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Package Outlines

P-SOJ-40-1

(Small Outline J-Leaded Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPJ09018

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

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