HN62448I Series

524288-word × 16-bit/1048576-word × 8-bit CMOS Mask Programmable ROM

HITACHI

ADE-203-772A (Z)
Rev. 1.0
Apr. 24, 1997

Description

The Hitachi HN62448I series is a 8-Mbit CMOS mask-programmable ROM organized either as 524288-word × 16-bit or 1048576-word × 8-bit. It has a high speed normal access time of 100 ns. It is suitable for program and data memory for micro computer systems. It has package variations of standard 42-pin plastic DIP and standard 44-pin plastic SOP.

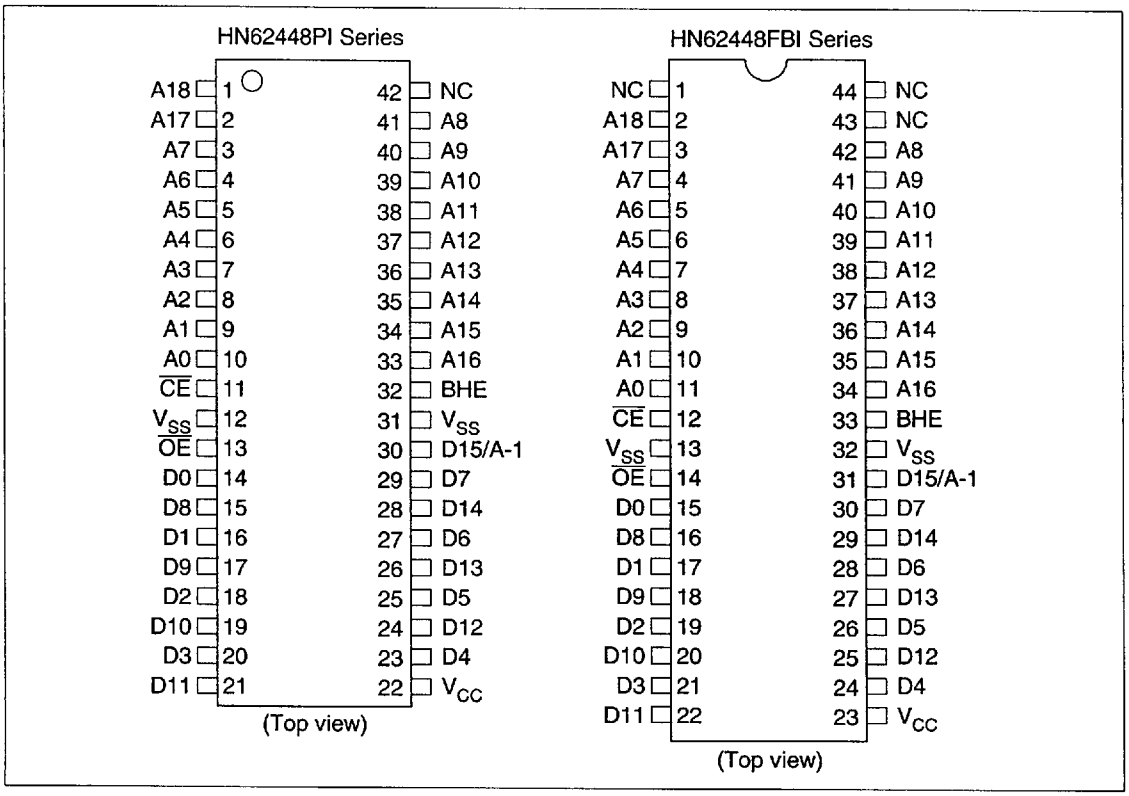
Features

- Single 5 V supply : 5.0 V ± 10%
- Access time:
  — Normal access time: 100 ns (max)
- Power dissipation
  — Active: 550 mW (max)
  — Standby: 165 µW (max)
- Byte-wide or word-wide data organization with byte/word selection (BHE)
- Three-state data output for wired or-tying
- Directly TTL compatible all inputs and outputs
- Operating temperature rage: –40 to +85°C

Ordering Information

Type No.	Access time	Package
HN62448PI-10	100 ns	600mil 42-pin plastic DIP (DP-42)
HN62448FBI-10	100 ns	600mil 44-pin plastic SOP (FP-44D)

Pin Arrangement



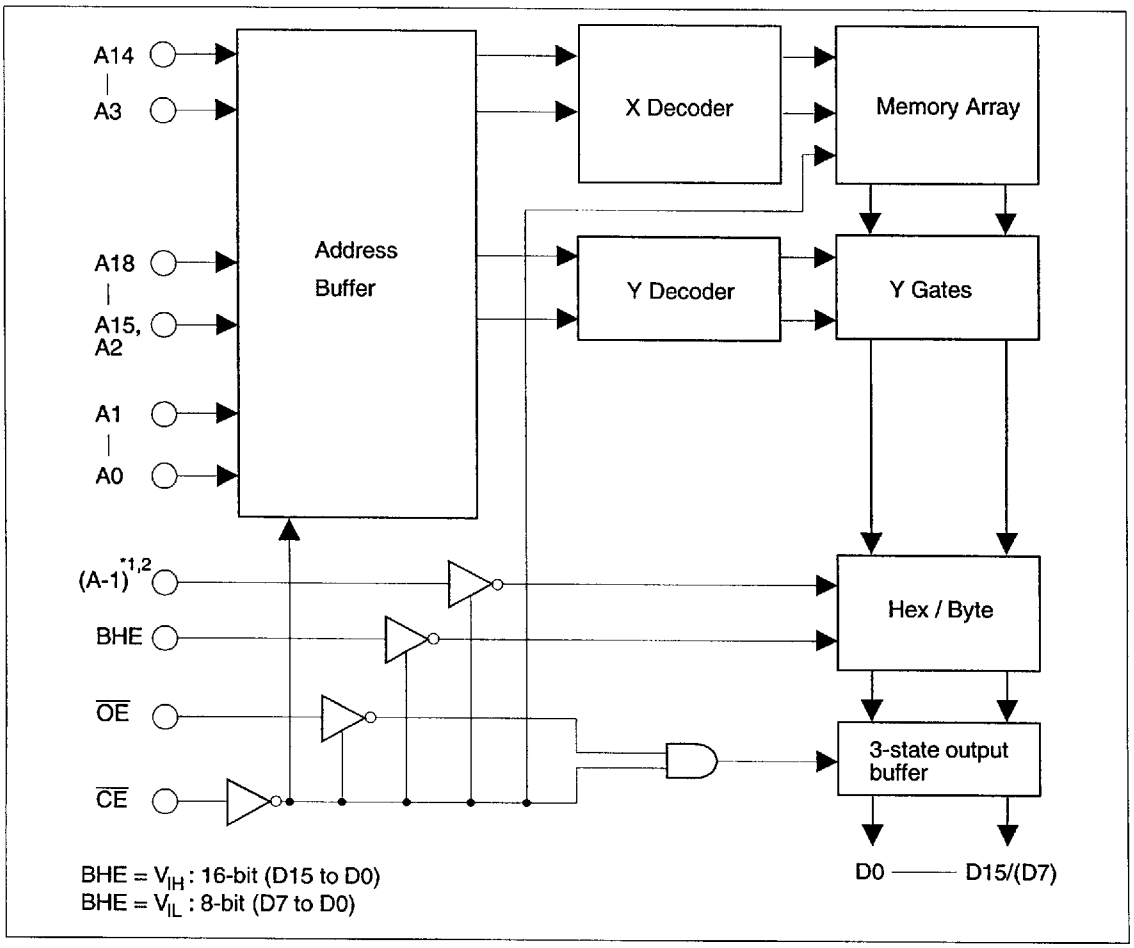
Pin Description

Pin name	Function
A-1, A0 to A18	Address input
D0 to D15	Data output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word selection
V_{cc}	Power supply
V_{ss}	Ground
NC	No connection

Block Diagram

Notes: 1. A-1 is least significant address.

2. When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.



Mode Selection

	Pin							
					Data output		Address input	
Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	×*1	×	×	High-Z	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A18
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A18
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A18

Note: 1. ×: Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.3 to +7.0	V
All input and output voltage relative to V_{SS}	Vin, Vout	–0.3 to V_{CC} +0.3	V
Operating temperature range	Topr	–40 to 85	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–40 to +85	°C

DC Operating Conditions (Ta = –40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = –40 to +85°C)

Parameter	Symbol	Min	Max	Unit	Test conditions
Operating V_{CC} current	I_{CC}	—	100	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 100 ns
Standby V_{CC} current	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ –0.2 V
	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE}$ = 2.2 V
Input leakage current	$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current	$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output high voltage	V_{OH}	2.4	—	V	I_{OH} = –205 µA
Output low voltage	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance	Cin	—	10	pF
Output capacitance	Cout	—	15	pF

AC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = –40 to + 85°C)

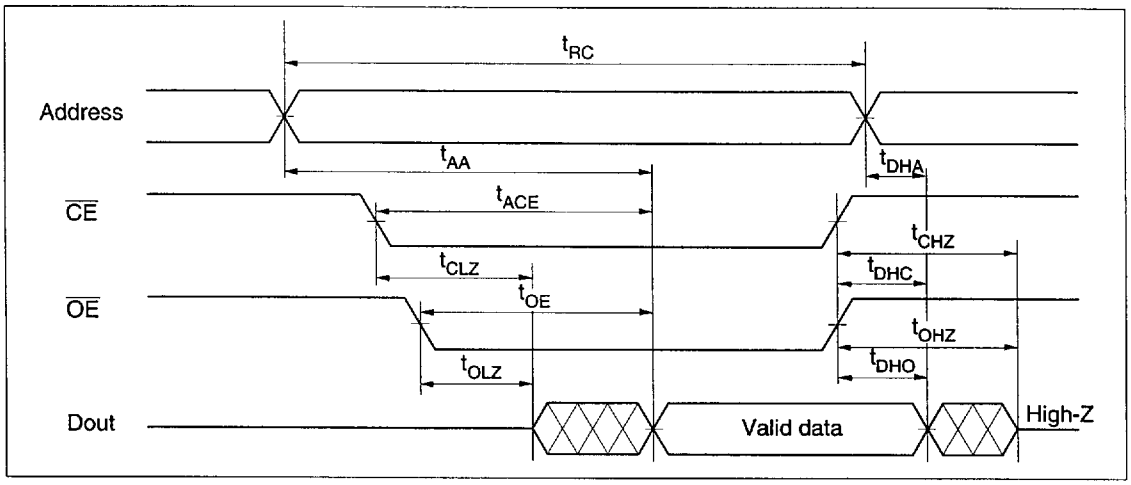
- Input pulse levels: 0.4 to 2.8 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1TTL + C_L = 100 pF (including jig)

		HN62448I-10			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	Notes
Read cycle time	t_{RC}	100	—	ns	
Address access time	t_{AA}	—	100	ns	3
$\overline{CE}$ access time	t_{ACE}	—	100	ns	3
$\overline{OE}$ access time	t_{OE}	—	40	ns	3
BHE access time	t_{BHE}	—	100	ns	
Output hold time from address change	t_{DHA}	0	—	ns	2
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns	2
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns	2
Output hold time from BHE	t_{DHB}	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}*1	—	40	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}*1	—	40	ns	1
BHE to output in high-Z	t_{BHZ}*1	—	40	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	ns	4
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	ns	4
BHE to output in low-Z	t_{BLZ}	5	—	ns	

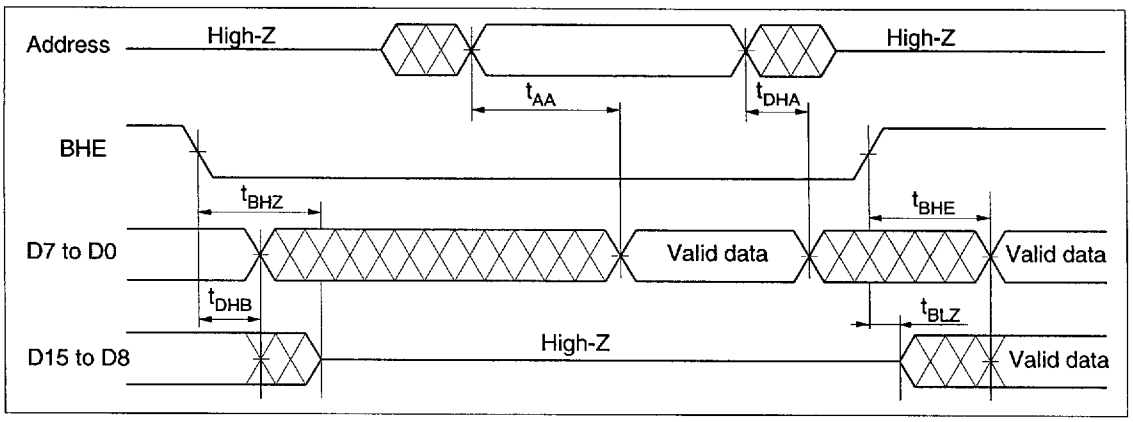
Notes: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.
2. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
3. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
4. t_{CLZ}, t_{OLZ}: Determined by slower.
5. $\overline{CE}$ and $\overline{OE}$ are enable A18 to A0 are valid.
6. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must be applied to them.
7. This device is used ATD (Address Transient Detector). Therefore, transfer either $\overline{CE}$ or address (A2 to A18) after power up to 4.5 V.

Timing Waveforms

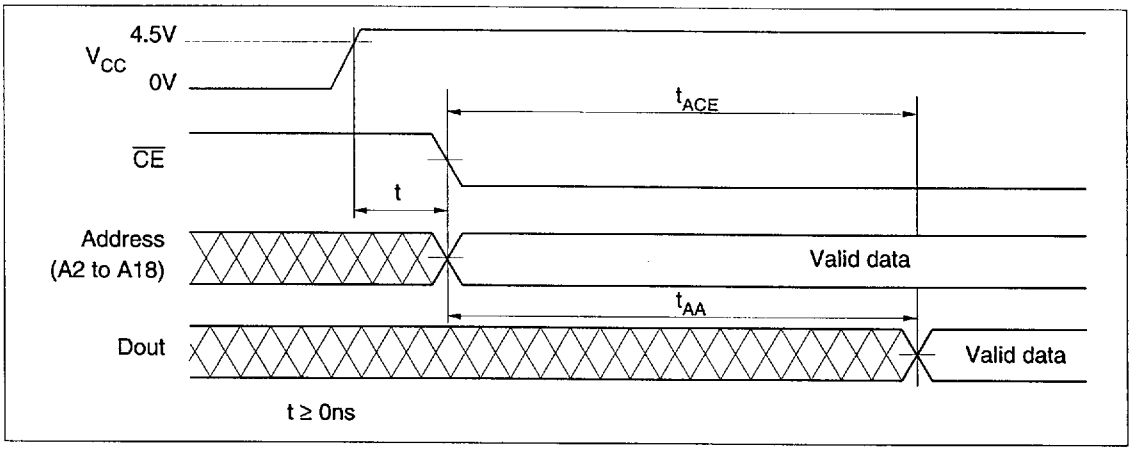
Word Mode (BHE = 'V_{IH}') **or Byte Mode** (BHE = 'V_{IL}')*[2, 3, 4]



Word Mode, Byte Mode Switch*[5, 6]



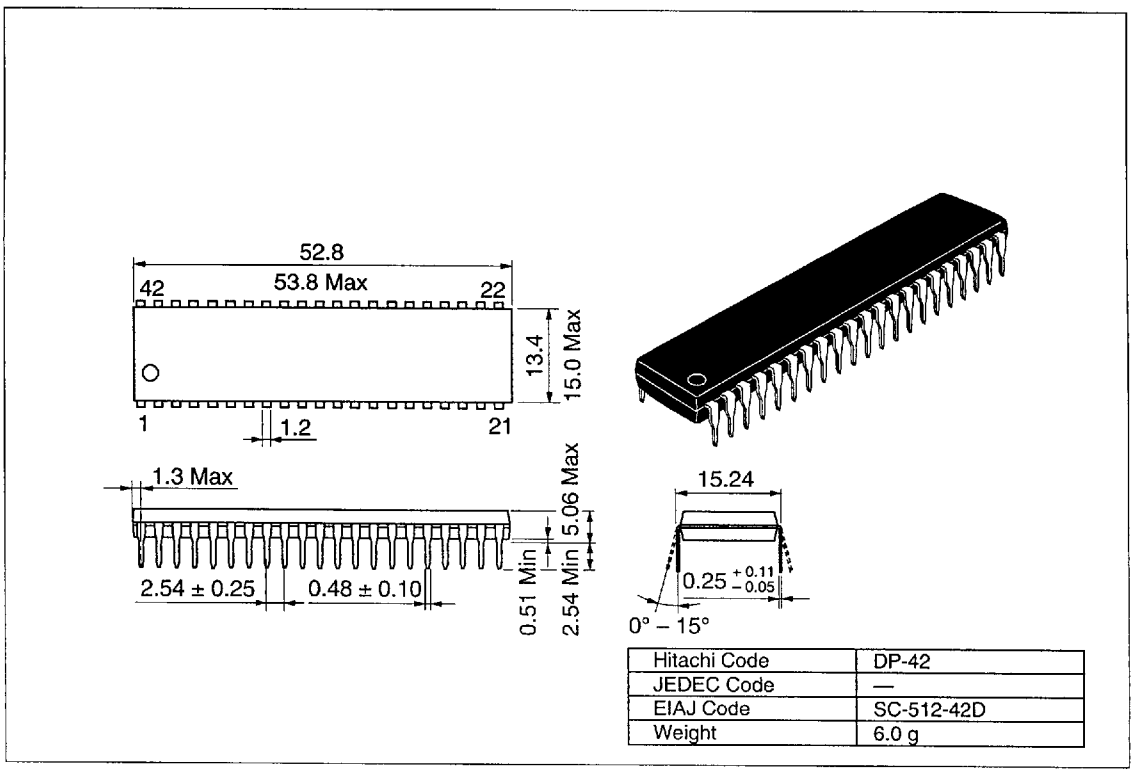
Power Up Sequence[*7]



Package Dimensions

HN62448PI Series (DP-42)

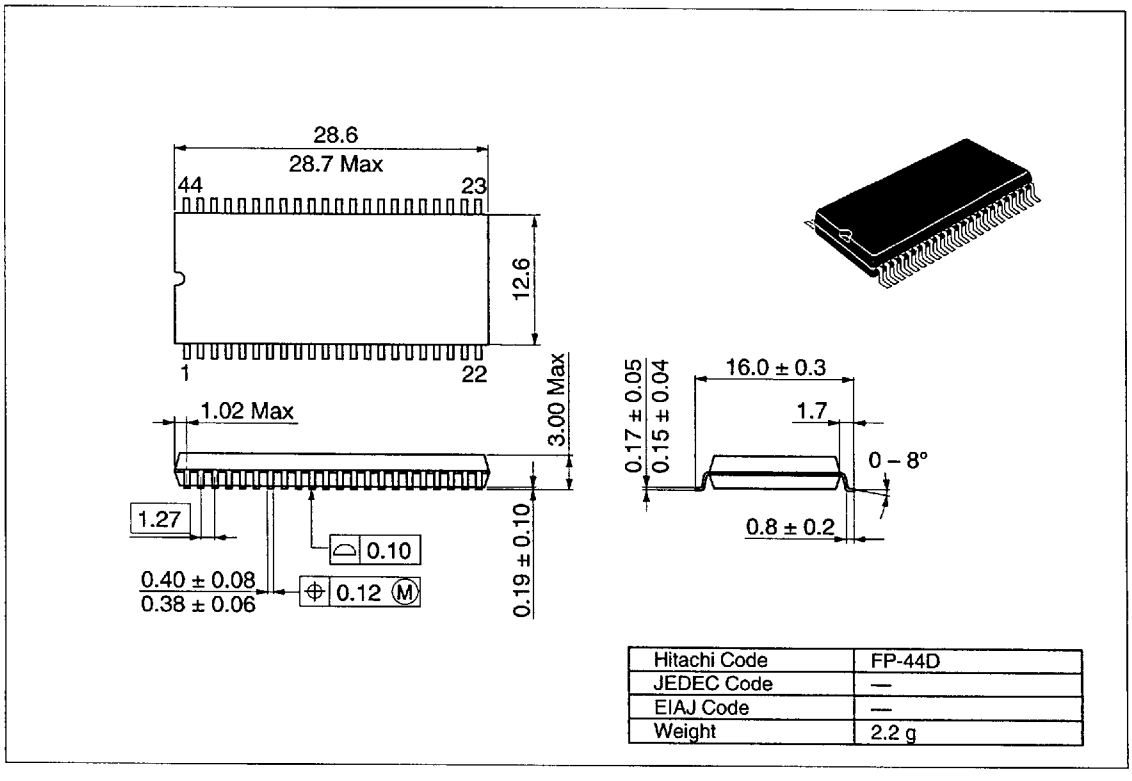
Unit: mm



Hitachi Code	DP-42
JEDEC Code	—
EIAJ Code	SC-512-42D
Weight	6.0 g

HN62448FBI Series (FP-44D)

Unit: mm



Hitachi Code	FP-44D
JEDEC Code	—
EIAJ Code	—
Weight	2.2 g

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Sales Offices

HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Apr. 24, 1997	Initial issue		