ZARLINK™
SEMICONDUCTOR

ZL10038
Advanced Modulation Satellite Tuner

Data Sheet

July 2004

Features

- Single-chip L band to zero IF quadrature down converter compliant with 1-45 Msps DVB-S2
- High dynamic range of -92 dBm to -10 dBm without RF attenuator or RSSI
- High total composite power handling
- Excellent immunity to adjacent channel interference through programmable and autocalibrated channel filters
- Integrated *power and forget* LO oscillators
- 2 degree integrated phase jitter enables excellent performance for 8 PSK and 16 QAM applications
- Less than +/- 3° and +/-0.6 dB I/Q quadrature balance
- Integrated RF loop through for cascaded tuner applications
- Power saving mode

Applications

- Advanced modulation DVB-S and DSS satellite receivers requiring upgrade for DVB-S2, 8 PSK / 16 QAM

Ordering Information

ZL10038/LDG	40-pin QFN	(trays)
ZL10038/LDG1	40-pin QFN*	(trays)
ZL10038/LDF	40-pin QFN	(tape and reel)
ZL10038/LDF1	40-pin QFN*	(tape and reel)

*Pb free

-10°C to +85°C

Description

ZL10038 is a fully integrated tuner for advanced modulation satellite receivers, operating over 950 - 2150 MHz and symbol rates in the range 1 - 45 MS/s.

It contains a selectable RF bypass for connecting to a second receiver module. ZL10038 simply requires a crystal reference and operates from a 5 V supply. It is designed as a 'simple to use' stand-alone tuner, requiring no training algorithms or user/demodulator intervention to optimize performance.

The ZL10038 can be used with an advanced modulation demodulator to create a highly-integrated front-end solution, operating from 1-45 MS/s.

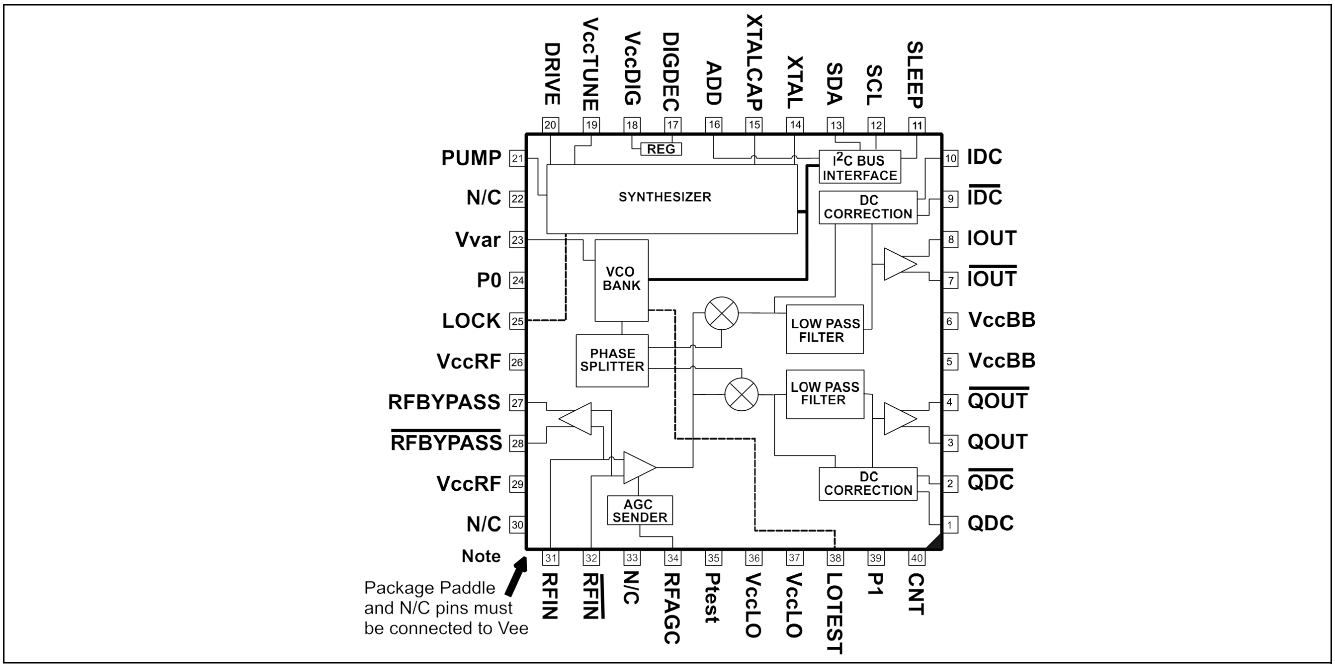

Figure 1 - Block Diagram

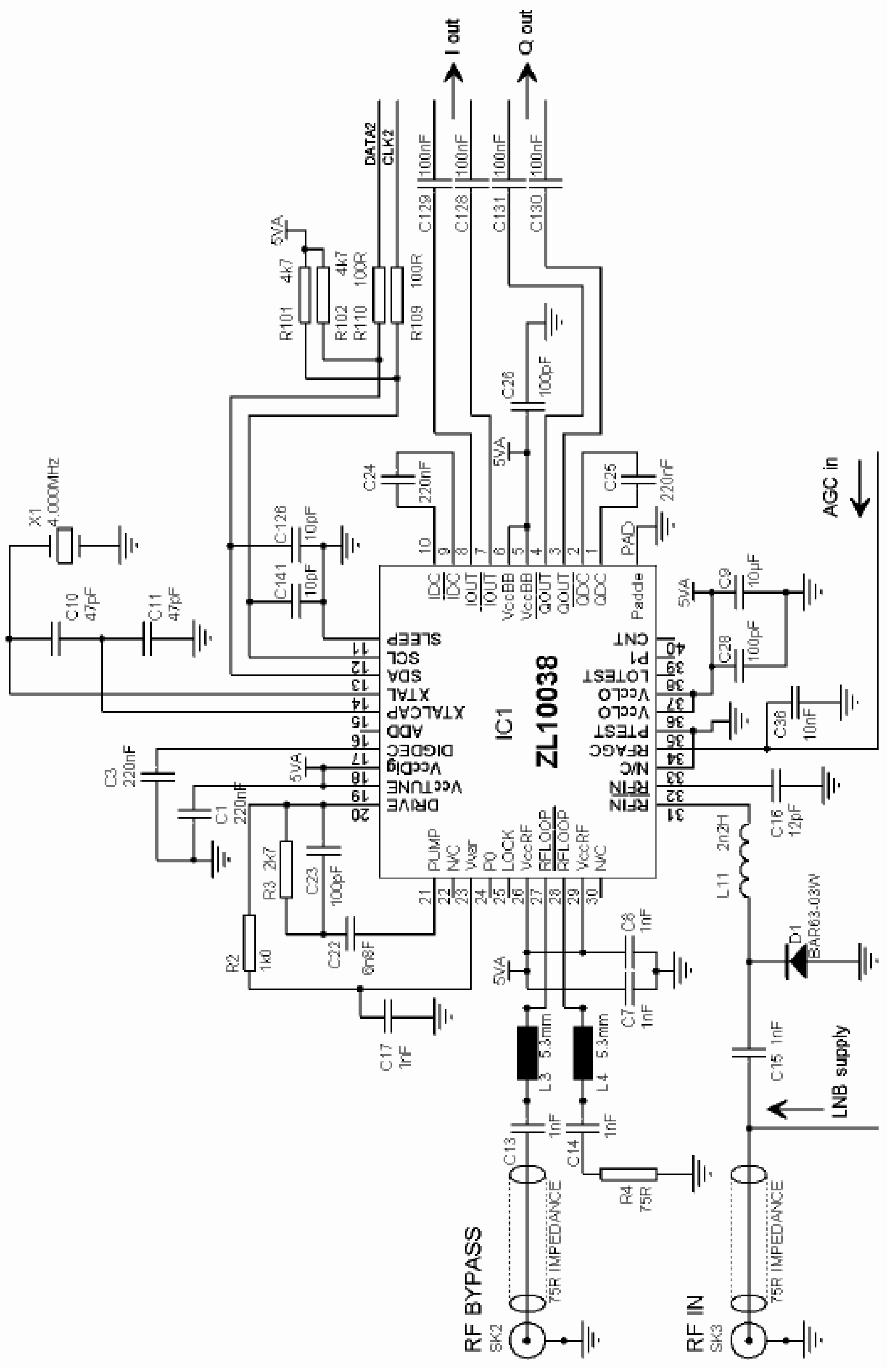

Figure 2 - Typical Application Circuit

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1.0 Overview

1.1 Conventions in this Manual

Hexadecimal values are typically shown as 0xABCDEF. Binary values (usually of register bits) are shown as 01100_2. All other numbers should be considered to be decimal values unless specified otherwise.

1.2 Pin Listings

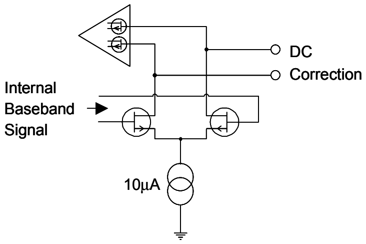
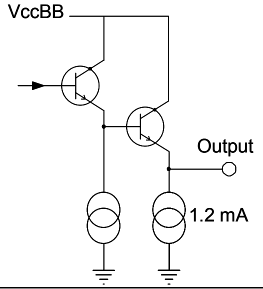
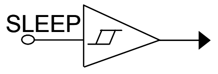
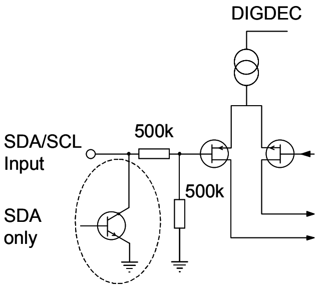
No.	Name	No.	Name	No.	Name	No.	Name
1	QDC	11	SLEEP	21	PUMP	31	RFIN
2	$\overline{\text{QDC}}$	12	SCL	22	N/C	32	$\overline{\text{RFIN}}$
3	QOUT	13	SDA	23	Vvar	33	N/C
4	$\overline{\text{QOUT}}$	14	XTAL	24	P0	34	RFAGC
5	VccBB	15	XTALCAP	25	LOCK	35	PTEST
6	VccBB	16	ADD	26	VccRF	36	VccLO
7	$\overline{\text{IOUT}}$	17	DIGDEC	27	RFBYPASS	37	VccLO
8	IOUT	18	VccDIG	28	$\overline{\text{RFBYPASS}}$	38	LOTEST
9	$\overline{\text{IDC}}$	19	VccTUNE	29	VccRF	39	P1
10	IDC	20	DRIVE	30	N/C	40	CNT

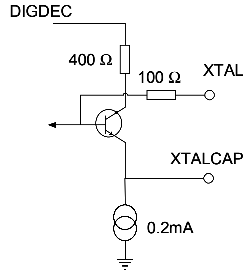
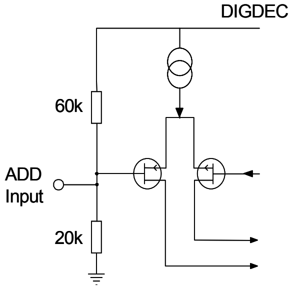
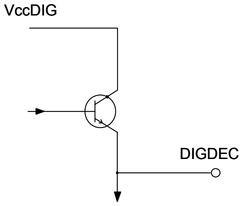
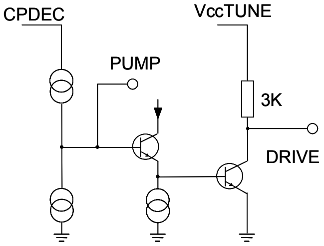
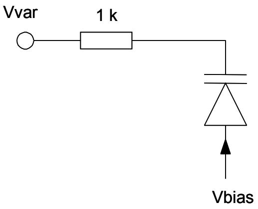
Table 1 - Pins by Number Order

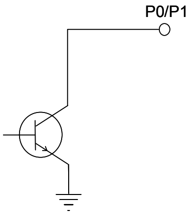
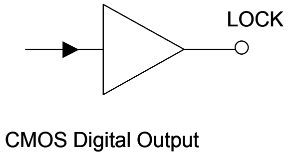
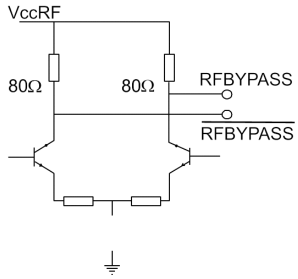
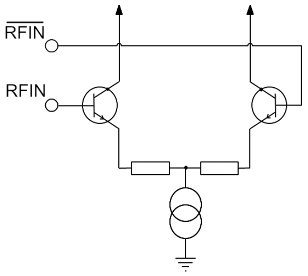
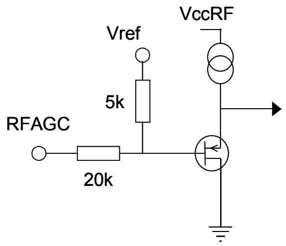
Name	No.	Name	No.	Name	No.	Name	No.
ADD	16	N/C	22	$\overline{\text{QOUT}}$	4	VccBB	6
CNT	40	N/C	30	RFAGC	34	VccDIG	18
DIGDEC	17	N/C	33	RFIN	31	VccLO	36
DRIVE	20	P0	24	$\overline{\text{RFIN}}$	32	VccLO	37
$\overline{\text{IDC}}$	9	P1	39	RFBYPASS	27	VccRF	26
IDC	10	PTEST	35	$\overline{\text{RFBYPASS}}$	28	VccRF	29
IOUT	7	PUMP	21	SCL	12	VccTUNE	19
IOUT	8	QDC	1	SDA	13	Vvar	23
LOCK	25	$\overline{\text{QDC}}$	2	SLEEP	11	XTAL	14
LOTEST	38	QOUT	3	VccBB	5	XTALCAP	15

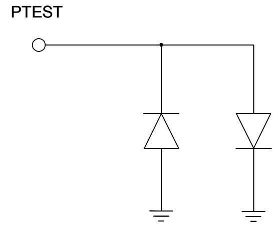
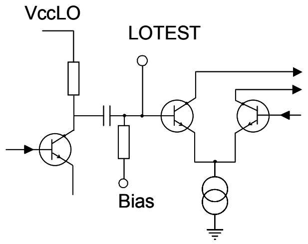
Table 2 - Pins by Name Order

1.3 Pin Descriptions

Pin	Symbol	Direction	Function	Schematics
1	**QDC**	NA	Q Channel DC offset correction capacitor. Configuration and value as per application diagram (see Figure 2).	
2	**$\overline{\text{QDC}}$**	NA		
3	**QOUT**	Out	Q Channel baseband differential outputs. AC couple outputs as per applications diagram (see Figure 2).	
4	**$\overline{\text{QOUT}}$**	Out		
5	**VccBB**		+5 v voltage supply for Baseband	
6	**VccBB**		+5 v voltage supply for Baseband	
7	**$\overline{\text{IOUT}}$**	Out	I Channel baseband differential outputs AC couple outputs as per applications diagram (Figure 2).	Same configuration as pins 3 & 4
8	**IOUT**	Out		
9	**$\overline{\text{IDC}}$**	NA	I Channel DC offset correction capacitor. Configuration and value as per application diagram (Figure 2).	Same configuration as pins 1 & 2
10	**IDC**	NA		
11	**SLEEP**	In	Hardware power down input. Logic '0' – normal mode. Logic '1' - analogue sections are powered down. This function is OR'ed with the PD control function, see section 3.1.2.	 CMOS Digital Input
12	**SCL**	In	I²C serial clock input	
13	**SDA**	Out	I²C serial data input/output	

Pin	Symbol	Direction	Function	Schematics
14	**XTAL**	In	Reference oscillator crystal inputs. Selected crystal frequency must be programmed in BR4 to BR0 for correct baseband filter bandwidth operation. XTAL pin is used for external reference input via 10nF capacitor.	
15	**XTALCAP**	Out		
16	**ADD**	In	Variable I²C address selection allowing the use of more than one device per I²C bus system by the voltage on this pin. See Table 3 for programming details.	
17	**DIGDEC**	Out	Decouple pin for internal digital 3.3 V regulator	
18	**VccDIG**		+5 v voltage supply for digital logic	
19	**VccTune**		Varactor tuning +5 v supply	
20	**DRIVE**	IO	Loop amplifier output and input pins	
21	**PUMP**	IO		
22	**N/C**		Not connected. Ground externally.	
23	**Vvar**	In	LO tuning voltage input	

Pin	Symbol	Direction	Function	Schematics
24	**P0**	Out	Switching port P0. ‘0’ = disabled (high impedance). ‘1’ = enabled.	
25	**LOCK**	Out	Output which indicates that phase comparator phase and frequency lock has been obtained and that the varactor voltage is within ‘tune unlock’ window. This powers up in logic ‘0’ state.	
26	**VccRF**		+5 v voltage supply for RF	
27	**RFBYPASS**	Out	RF Bypass differential outputs. AC couple outputs. Matching circuitry as per applications diagram (Figure 2). In applications where RF Bypass is not required, pins should not be connected.	
28	**$\overline{\text{RFBYPASS}}$**	Out		
29	**VccRF**		+5 v voltage supply for RF	
30	**N/C**		Not connected. Ground externally.	
31	**RFIN**	In	RF differential inputs. AC couple input. Matching circuitry as per applications diagram.	
32	**$\overline{\text{RFIN}}$**	In		
33	**N/C**		Not connected. Ground externally.	
34	**RFAGC**	In	RF analogue gain control input	

Pin	Symbol	Direction	Function	Schematics
35	**PTEST**	In	Connected to internal circuit for monitoring die temperature	
36	**VccLO**		+5 v voltage supply for LO	
37	**VccLO**		+5 v voltage supply for LO	
38	**LOTEST**	IO	Bi-directional test port for accessing internal LO AC couple input.	
39	**P1**	Out	Switching port P1 '0' = disabled (high impedance) '1' = enabled	Same configuration as pin 24, P0
40	**CNT**		Bonded to paddle. Production continuity test for paddle soldering	

Note: Exposed paddle on rear of package must be connected to GND.

2.0 Functional Description

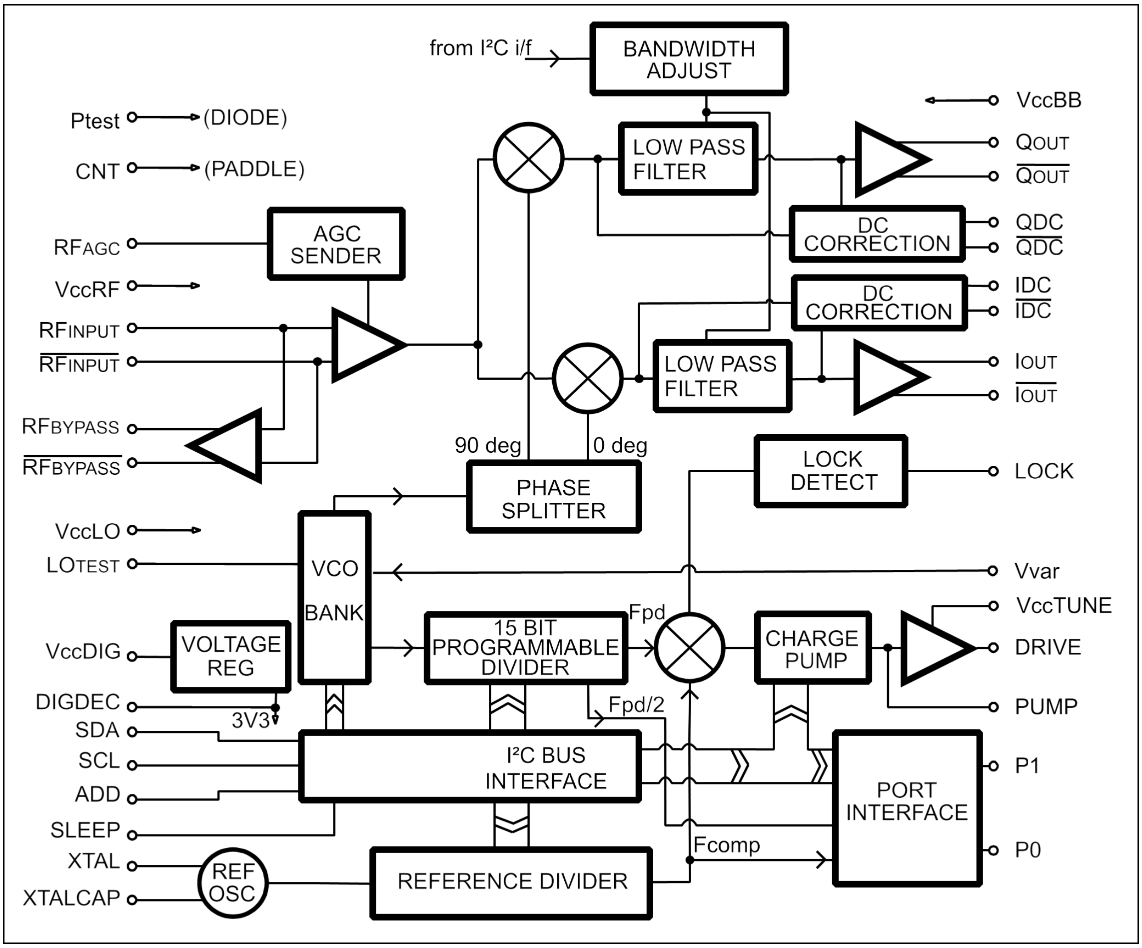


Figure 3 - Detailed Block Diagram

2.1 Quadrature Down-Converter

In normal applications the tuner RF input frequency of 950 - 2150 MHz is fed directly to the ZL10038 RF input preamplifier stage, through an appropriate impedance match. The input preamplifier is optimized for NF, S11 and signal handling.

The signal handling of the front end is designed such that no tracking filter is required to offer immunity to input composite overload.

2.2 AGC Functions

The ZL10038 contains an analogue RF AGC combined with digitally controlled gain for RF, baseband pre-filter and post-filter, as described in Figure 4. The baseband AGC is controlled by the I²C bus and is divided into pre- and post-baseband filter stages, each of which have 12.6 dB of gain adjust in 4.2 dB steps.

The RF AGC is provided as the dynamic system gain adjust under control of the baseband analogue AGC output function whereas the digitally controlled gains are provided to maximize performance under different signal conditions. The total AGC gain range will guarantee an operating dynamic range of -92 to -10 dBm.

The digitally controlled RF gain adjust and the baseband pre-filter stage can be adjusted in sympathy to maintain a fixed overall conversion gain. The lower RF gain setting would be used in situations where for example there is a high degree of cable tilt or high desired to undesired ratio, whereas the higher RF gain setting would be used in situations where for example it is desirable to minimize NF.

The baseband post-filter gain stage can be used to provide additional gain to maintain desired output amplitude with lower symbol rate applications.

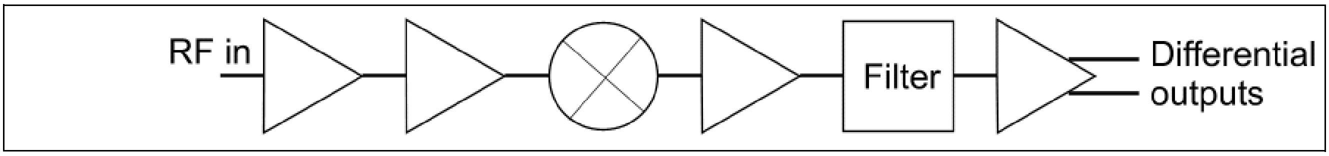


Figure 4 - AGC Control Structure

Normalized gain range in dB:	0 - 72	0 or +4	0 to 12.6 in 4.2 dB steps	0 to 12.6 in 4.2 dB steps
Gain function:	RF AGC	Stepped	Stepped	Stepped
Control function:	Analogue voltage	I²C bus	I²C bus	I²C bus

2.2.1 RF

The RF input amplifier feeds an AGC stage, which provides for RF gain control.

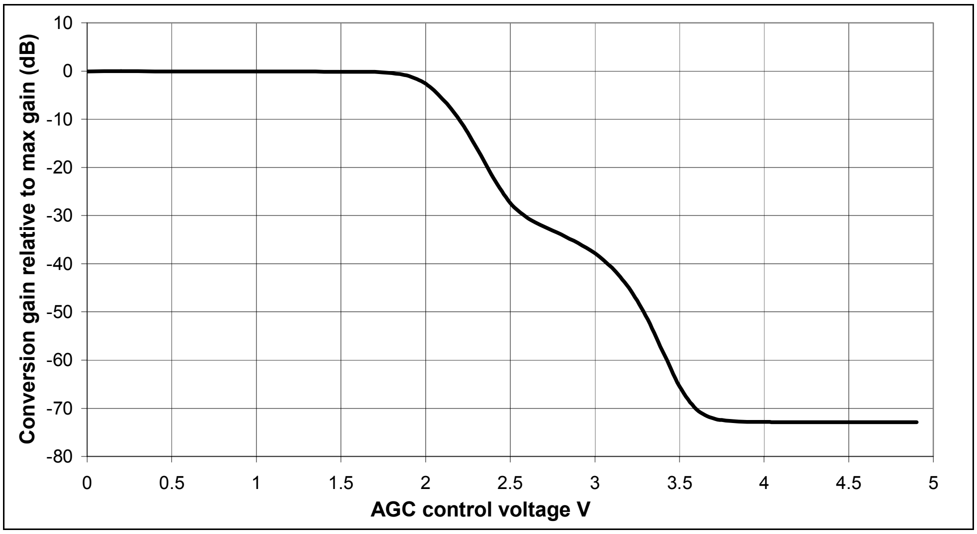


Figure 5 - Typical First Stage RF AGC Response

The RF AGC is divided into two stages. The first stage is a continually variable gain control stage, which is controlled by the AGC sender and provides the main system AGC set under control of the analogue AGC signal generated by the demodulator section. The second stage is a bus programmable. two-position gain set previous to the quadrature mixer and provides for 4 dB of gain adjust under software control.

The analogue RF AGC is optimized for S/N and S/I performance across the full dynamic range. The RF AGC characteristic, variation of IIP2, IIP3 and NF are contained in Figure 6, Figure 7 & Figure 8 respectively.

The RF preamplifier is also coupled to the selectable RF bypass, which is described in 2.3, “RF Bypass“. The specified electrical parameters of the RF input are unaffected by the RF bypass state.

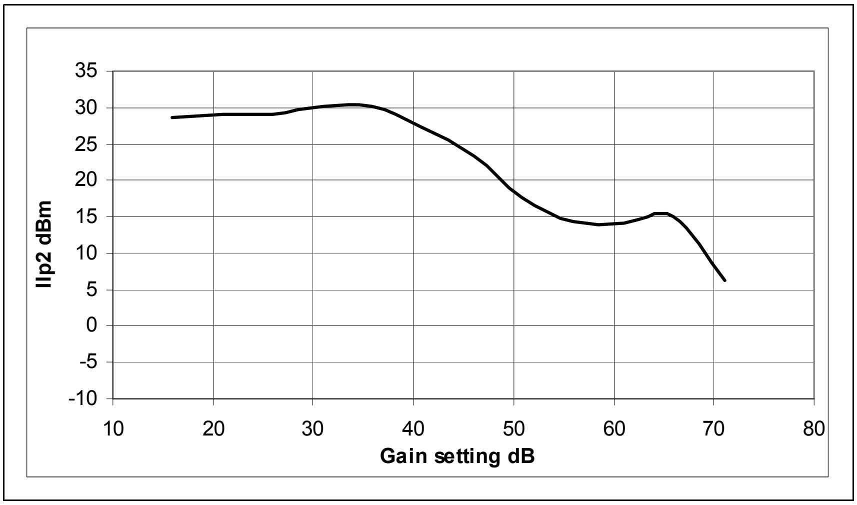


Figure 6 - Variation in IIP2 with AGC Setting

(RF gain adjust = +0 dB, prefilter = +4.2 dB and postfilter = 4.2 dB, baseband filter bandwidth = 22 MHz)

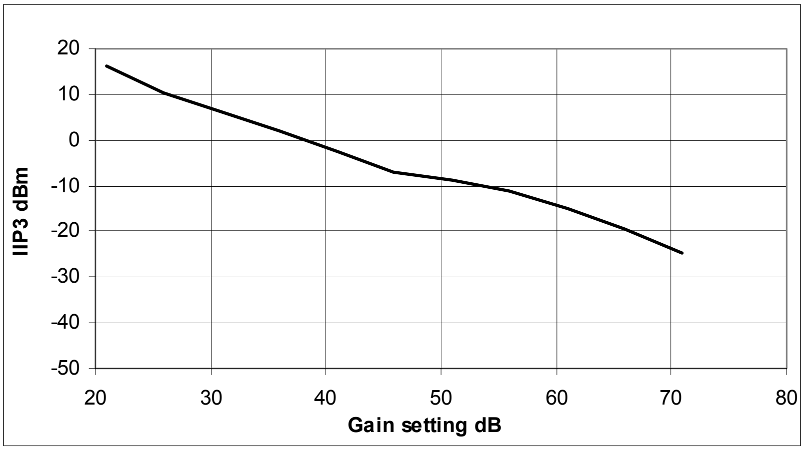


Figure 7 - Variation in IIP3 with AGC Setting

(RF gain adjust = +0 dB, prefilter = +4.2 dB and postfilter = 4.2 dB, baseband filter bandwidth = 22 MHz)

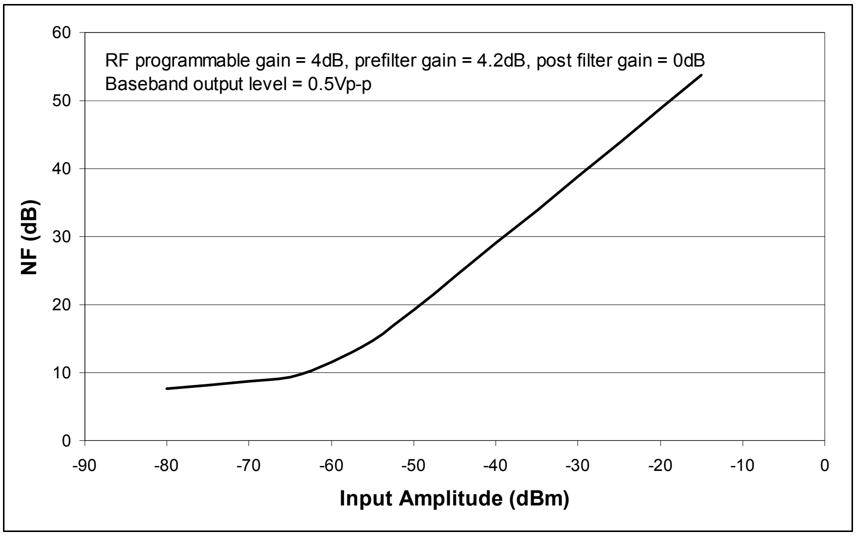


Figure 8 - Variation in NF with Input Amplitude (typical)

The output of the RF AGC stage is coupled to the quadrature mixer where the RF input is mixed with quadrature LO (local oscillator) signals generated by the on-board LO. Operation and control of the LO is described further in section 2.5 on page 17.

2.2.2 Baseband

The mixer outputs are coupled to the baseband quadrature channel amplifier and filter stage, which is of 7th order topology. Operation and control of the baseband filter is contained in Section 2.4 on page 16.

The baseband paths are DC coupled, and include a DC correction loop. The high pass characteristic for the DC correction loop is defined by the off chip capacitor connected to pins ‘IDC/$\overline{\text{IDC}}$’ and ‘QDC/$\overline{\text{QDC}}$’. The output of each channel stage is designed for low impedance drive capability and low intermodulation and can be loaded either differentially or single-ended; in the case of single-ended load the unused output should be unloaded. The maximum output load is defined in the Electrical Characteristics Table.

2.3 RF Bypass

The ZL10038 provides an independent bypass function, which can be used for driving a second receiver module. The electrical characteristics of the RF input are unchanged by the state of the RF bypass.

The bypass provides a differential buffered output from the input signal with a nominal 3.5 dB gain. The unused output should be terminated as in Figure 2 on page 2.

The bypass function is enabled by a single register bit and is not disabled by either the **PD** bit or the SLEEP pin. When disabled the bypass function is in a ‘power-down’ state. On power up the bypass function is enabled.

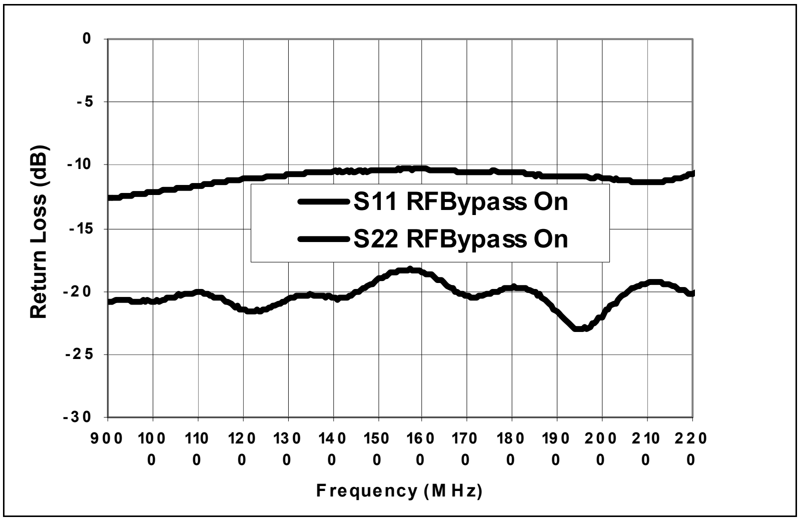


Figure 9 - RF Input and Output (bypass) Return Losses

2.4 Baseband Filter

The filter bandwidth is controlled by a Frequency Locked Loop (FLL) the timing of which is derived from the reference crystal source by a reference divider. Five control bits set the system reference division ratio and the baseband filter bandwidth can be programmed with a further six control bits for a nominal range of 4 - 40 MHz[1].

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[1] specification compliant over the range 8 - 35 MHz.

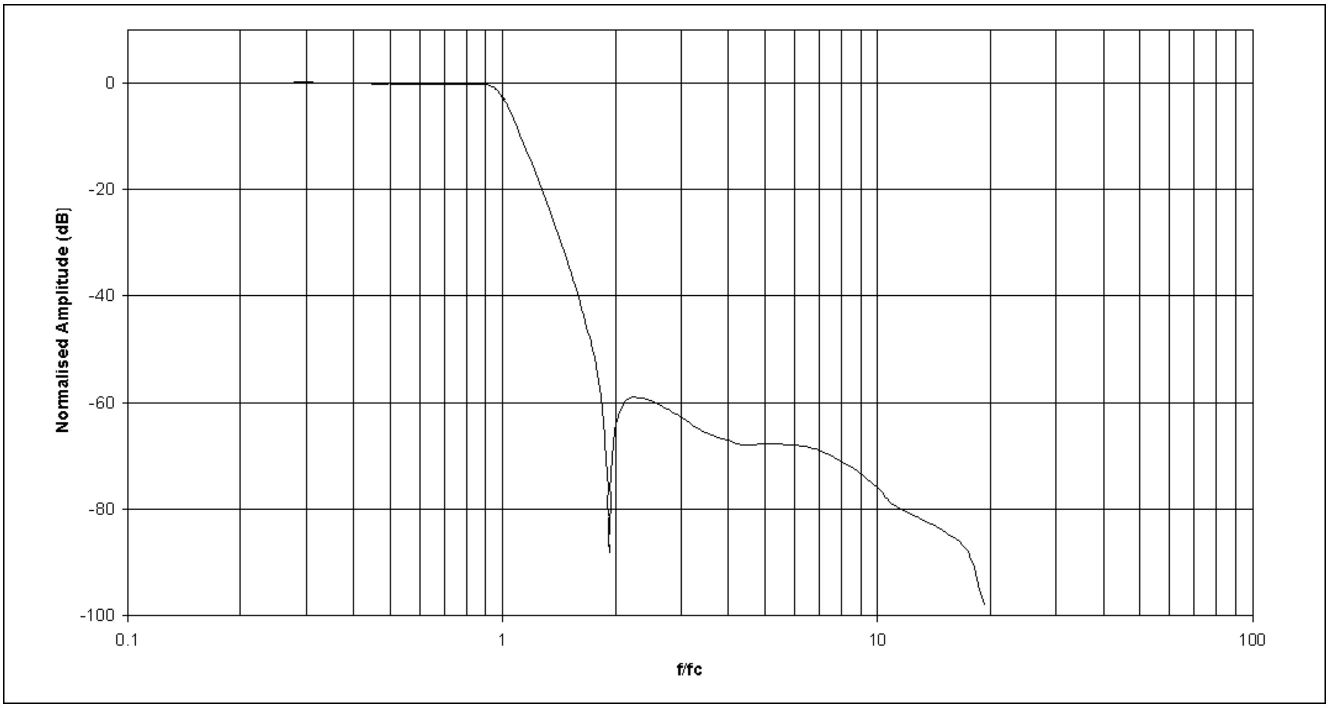

Figure 10 - Normalized Filter Transfer Characteristic (setting 20 MHz)

The -3 dB bandwidth of the filter (Hz) is given by the following expression: $f_{-3dB} = \frac{f_{xtal}}{BR} \times (BF + 1) \times \frac{1}{K}$

Where:

f_{-3dB} = Baseband filter –3 dB bandwidth (Hz) which should be within the range $8MHz \le f_{-3dB} \le 35MHz$.

f_{xtal} = Crystal oscillator reference frequency (Hz).

K = 1.257 (constant).

BF = Decimal value of the register bits BF6:BF1, range 0 - 62.

BR = Decimal value of the bits BR4:BR0 (baseband filter reference divider ratio), range 4 - 27.

$\frac{f_{xtal}}{BR}$ = 575 kHz to 2.5 MHz.

Methods for determining the values of BR and BF are given in the section on software, please see sect. 4.3 on page 30.

2.5 Local Oscillator

The LO on the ZL10038 is fully integrated and consists of three oscillator stages, each with 16 sub-bands. These are arranged such that the regions of operation for optimum phase noise are continuous over the required tuning range of 950 to 2150 MHz and over the specified operating ambient conditions and process spread.

The local oscillators operate at a harmonic of the required frequency and are divided down to the required LO conversion frequency. For each of the three oscillators, the LO prescaler ratio (N_{LP}) is set to ÷4 or ÷2. The required divider ratio is automatically selected by the LO control logic, hence programming of the required conversion frequency across the oscillator bands is automatic and requires no intervention by the user.

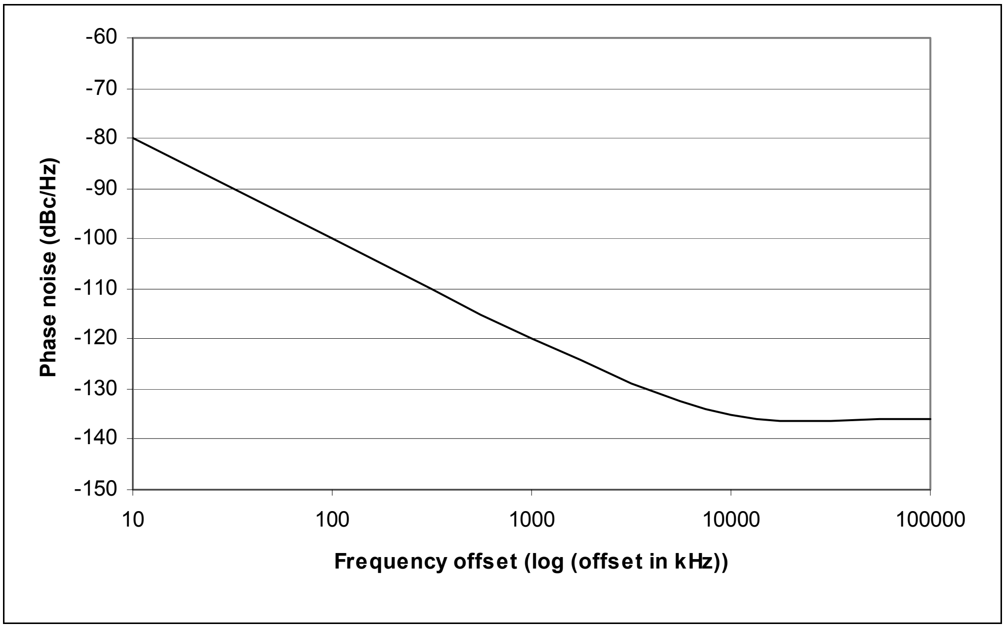

Figure 11 - Free Running LO Phase Noise Performance

The oscillators are designed to deliver good free running phase noise at 10 kHz offset, therefore the required integrated phase jitter from the LO can be achieved without the requirement for running with a high comparison frequency and hence large tuning increment and wide loop bandwidth.

The LO section contains an internal tuning controller, which will automatically tune to the appropriate VCO and sub band for optimum phase noise performance. The internal LO controller function is transparent to the user and no user intervention is required. The tuning controller will automatically switch bands when required, however this function can be disabled with the '**VSD**' bit (see "3.4.15"). This enables the user to select the appropriate VCO and sub band if required to achieve optimum phase noise performance. For QPSK, automatic mode will be adequate and should be used. In general for 8 PSK modulation, the automatic mode will also be adequate depending on the demodulator requirements. 16 QAM may require manual mode to optimize phase noise performance at frequencies above 1800 MHz.

2.5.1 LO Programming

The controller tunes across the oscillator bands, until lock is achieved. The algorithm for tuning utilises the LO tuning voltage, Vvar, which is compared at a programmable sample rate against a 'tune lock' voltage window and a 'tune unlock' voltage window. The sampling rate default on power up is Fcomp/8 however this can be programmed into further rates through bits LS2-LS0 in byte-10, see "3.4.17" on page 29. The 'tune lock' and 'tune unlock' windows are set at default values, however, these can be adjusted by bits **WS**, **WH2:0** and **WL2:0** in byte 11, see "3.4.18" on page 29.

In the event that the controller is unable to find lock the 'tune lock' window will be automatically widened. This facility can be disabled by setting bit **WRE** in byte 11 to logic '0'. See 3.4.19 on page 30.

The device has a lock indicator flag, **FL**, which is derived from a time averaged phase comparison between the LO divider and reference divider inputs to the phase comparator. The **FL** flag is read in the status byte. See 3.3.2 on page 21.

There is a further hardware lock flag (LOCK output, pin 25; see "3.1.1" on page 20) which generates a logic '0' if the tuning controller detects the varactor line voltage lies within the 'tune unlock' window and if **FL** is set to logic '1'. In other states this output is high impedance.

The tune lock window is centralised within the tuner unlock window. The tuning controller selects the VCO and sub band so that the varactor voltage is within this window. If this is not possible the lock windows are relaxed (assuming the WRE bit is set to '1'). The tuning algorithm maintains a level of hysteresis to prevent short term drift causing switching to an adjacent band.

The LO control logic has provision for master reset to restore initial set up conditions. This is controlled by bit CLR within data byte 13, see “3.4.10” on page 25.

2.6 PLL Frequency Synthesizer

The PLL frequency synthesizer section contains all the elements necessary, with the exception of a frequency reference and loop filter to control a varicap tuned LO, so forming a complete PLL frequency synthesized source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. The loop can also be operated up to comparison frequencies of 2 MHz enabling application of a wide loop bandwidth for maximizing the close in phase noise performance.

The LO input signal is multiplexed from the selected oscillator band to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces direct with the 15-bit fully programmable divider, which is of MN+A architecture. A 16/17 dual modulus prescaler is used.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on-board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider, which is programmable into one of 29 ratios as detailed in Table 14 on page 26.

The typical application for the crystal oscillator is contained in Figure 2. The output of the phase detector feeds a charge pump and loop amplifier section. This combined with an external loop filter integrates the current pulses into the varactor line voltage with an output range of Vee to VccTUNE. The varactor line voltage is externally coupled to the oscillator section through the input Vvar, enabling application of a third order loop.

Control of the charge pump current can be made in two ways as described in Table 13 on page 26. Either the set charge pump current can be used at all times, or the charge pump current can be scaled automatically according to the LO sub-band. The second case allows for reduced loop bandwidth variation as the VCO gain varies with sub-band.

2.7 Control Logic

The ZL10038 is controlled by an I²C data bus and can function as a slave receiver or slave transmitter compatible with 3V3 or 5 V levels.

Data and Clock are input on the SDA and SCL lines respectively as defined by I²C bus standard. The device can either accept data (slave receiver, write mode), or send data (slave transmitter, read mode). The LSB of the address byte ($R/\overline{W}$) sets the device into write mode if it is logic ‘0’, and read mode if it is logic ‘1’. Table 4 and Table 7 illustrate the format of the read and write data respectively. The device can be programmed to respond to one of four addresses, which enables the use of more than one device in an I²C bus system if required for use in PVR[1] systems, for example. Table 3 shows how the address is selected by applying a voltage to the address, ‘**ADD**’, input. When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

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[1] PVR - Personal Video Recorder where dual tuners allow the viewer to watch one channel and record another simultaneously, usually to a hard-disk recording system.

All the ZL10038 functions are controlled by register bits written through the I²C bus interface. The **SLEEP** pin can be used to power-down the device, but it can also be put into the power-down mode with the **PD** register bit, the two functions being logically OR'ed.

Feedback on the status of the ZL10038 is provided through eight bits in the status byte register and the phase lock state is also available on the **LOCK** output pin (as well as the **FL** register bit).

3.0 User Control

3.1 I/O Pins

The I²C interface controls all the major functions. Apart from the various analogue functions, the only pins that either control the ZL10038, or are controlled by the internal logic, are the **LOCK**, **SLEEP**, **P1, P0** and **ADD** pins. Details follow:

3.1.1 LOCK - Pin 25

This is an output which indicates phase frequency lock on the correct VCO sub band for optimum phase noise. The CMOS output can directly drive a low power LED if required.

3.1.2 SLEEP - Pin 11

The **SLEEP** pin shuts down the analogue sections of the device to give a considerable power saving, typically reducing the power to about one third of its normal level. The RF-bypass function is entirely separate and is unaffected by the state of this pin. The **SLEEP** pin's function is OR'ed with the **PD** register bit (see "3.4.9" on page 25), so that if either is a logic one, the ZL10036 will be powered down, or alternatively, both must be at logic zero for normal operation.

3.1.3 Output Ports, P1 & P0 - Pins 39 & 24

Two open-collector ports are provided for general purpose use, under control of register bits **P1** and **P0**. The default at power-up is for the **P1** & **P0** register bits to be low, hence the outputs will be off, i.e., in their high-impedance states. If connected to a pull-up resistor this will therefore result in a logic high. Setting a register bit high will turn the corresponding output on and therefore pull the logic level to near 0 V giving a logic low.

3.2 Device Address Selection

Two internal logic levels, **MA1** and **MA0**, can be set to one of four possible logic states by the voltage applied to the **ADD** pin (#16). These four states in turn define four different read and write addresses on the I²C bus, so that as many as four separate devices can be individually addressed on one bus. This is of particular use in a multi-tuner environment as required by PVR applications.

ADD pin voltage	MA1	MA0	Write Address		Read Address	
			Hex.	Dec.	Hex.	Dec.
Vee (0 V or Gnd)	0	0	0xC0	192	0xC1	193
Open circuit	0	1	0xC2	194	0xC3	195
0.5 * DIGDEC (±20%)[1]	1	0	0xC4	196	0xC5	197
DIGDEC	1	1	0xC6	198	0xC7	199

Table 3 - Address Selection

[1] can be programmed with a single 30 kΩ resistor to DIGDEC

3.3 Read Register

The ZL10038 status can be read by addressing the device in its slave transmitter mode by setting the LSB of the address byte (the R/$\overline{W}$ bit) to a one. After the master transmits the correct address byte, the ZL10038 will acknowledge its address, and transmit data in response to further clocks on the SCL input. If the master responds with an acknowledge and further clocks, the status byte will be retransmitted until such time as the master fails to send an acknowledge, when the ZL10038 will release the data bus, allowing the master to generate a stop condition.

Bit No.	**7** (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0** (LSB)
Address	1	1	0	0	0	MA1	MA0	1
Status	POR	FL	SB3	SB2	SB1	SB0	TU1	TU0

Table 4 - Read Data Bit Format (MSB is Transmitted First)

The individual bits in the status register have the following meanings:

3.3.1 Power-On Reset Indicator (POR Bit)

This bit is set to a logic ‘1’ if the VccDIG supply to the PLL section has dropped below typically 3.6 V, e.g., when the device is initially turned on. The bit is reset to ‘0’ when the read sequence is terminated by a STOP command. When the POR bit is high, this indicates that the programmed information may have been corrupted and the device reset to power up condition.

3.3.2 Frequency (& Phase) Lock (FL Bit)

Bit 6 (FL) indicates whether the synthesizer is phase locked, a logic ‘1’ is present if the device is locked and a logic ‘0’ if the device is unlocked.

3.3.3 VCO Sub-Band (SB3:0 Bit)

These bits indicate the vco sub-band value chosen by the LO tuning algorithm when tuning the oscillators automatically. If manual tuning is used then SB3-SB0 will match bits S3-S0 written to register byte 9 (see “3.4.16” for sub-band details).

3.3.4 Tune Unlock State (TU1:0 Bit)

These bits define the ‘tune unlock’ window state as below:

TU1	**TU0**	**‘Tune unlock’ window state**
0	0	Vvar between lower and upper voltage thresholds
0	1	Vvar above upper voltage threshold
1	0	Vvar below lower voltage threshold
1	1	Undefined - do not use

Table 5 - TU1/0 Functions

See “LO Window Level (WS, WH2:0 & WL2:0 Bits)” on page 29 for further information on the threshold voltages.

3.4 Write Registers

The ZL10038 has twelve registers which can be programmed by addressing the device in its slave receiver mode, setting the LSB of the address byte (the R/$\overline{W}$ bit) to a zero. After the master transmits the correct address byte, the ZL10038 will acknowledge its address, and accept data in response to further clocks on the SCL line. At the end of each byte, the ZL10038 will generate the acknowledge bit. The master can at this point, generate a stop condition, or further clocks on the SCL line if further registers are to be programmed. If data is written after the twelfth register (byte-13), it will be ignored.

3.4.1 Register Sub-Addressing

If some register bits require changing, but not all, it is not necessary to write to all the registers. The registers can be addressed in pairs starting with the even numbered bytes, i.e., 2 & 3, 4 & 5, etc. Table 6 below shows the protocol required to address any of the even numbered register bytes. It therefore follows that to write to register byte-7 for instance, byte-6 must also be written first. Register pairs may be written in any order, as required by the software, e.g., 10/11 may be followed by 4/5.

Data Bits				**Byte Selected**
7 (MSB)	**6**	**5**	**4**	
0	X	X	X	2
1	0	X	X	4
1	1	0	0	6
1	1	0	1	8
1	1	1	0	10
1	1	1	1	12
‘X’ = *Don’t care (content defines a register bit).*				

Table 6 - Byte Address Allocation in Write Mode

3.4.2 Register Mapping

Byte	Bit No. Function	7 (MSB)	6	5	4	3	2	1	0 (LSB)	Reset state (hex.)[1]	Further information
1	Device address	1	1	0	0	0	MA1	MA0	0		Table 3 on page 20
2	Programmable Divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	0x00	See 3.4.3 on page 24
3		2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0x00	
4	Control Data	1	0	RFG	BA1	BA0	BG1	BG0	LEN	0x80	“3.4.4” to “3.4.7” on p. 25
5		P0	C1	C0	R4	R3	R2	R1	R0	0x00	pp. 25 & 26
6		1	1	0	0	RSD	0	0	0	0xC0	see “3.4.13” on page 27
7		P1	BF6	BF5	BF4	BF3	BF2	BF1	0	0x20	pp. 25 & 27
8		1	1	0	1	0	CC	1	1	0xDB	page 26
9		VSD	V2	V1	V0	S3	S2	S1	S0	0x30	page 28
10		1	1	1	0	0	LS2	LS1	LS0	0xE1	page 29
11		WS	WH2	WH1	WH0	WL2	WL1	WL0	WRE	0x75/F5	page 29
12		1	1	1	1	0	0	0	0	0xF0	test function only
13		PD	BR4	BR3	BR2	BR1	BR0	CLR	TL	0x28	pp. 25, 27 & 30

Table 7 - Bit Allocations in the Write Registers

[1] This is the power-on default register value - recommended operating values may be different, see “4.1” on page 30.

Symbol	Definition	Symbol	Definition
2^{14}-2^{0}	Programmable division ratio control bits	R4-R0	Reference division ratio select
BA1-0	Baseband prefilter gain adjust	RFG	RF programmable gain adjust
BF6-1	Baseband bandwidth adjust	RSD	Resistor switch disable
BG1-0	Baseband postfilter gain adjust	S3-0	LO sub-band select
BR4-0	Baseband filter FLL reference frequency select	TL	Buffered LO output select
C1,C0	Charge pump current select	PD	Power down
CC	Charge pump control	V2-0	LO main band select
CLR	Control logic reset	VSD	LO tuning algorithm disable
LEN	RF bypass enable	WH2-0	LO window high level adjust
LS2-0	Tuning control sampling rate adjust	WL2-0	LO window low level adjust
MA1,MA0	Variable address bits	WRE	Tuning Window Relaxation Enable
P0, P1	External switching ports	WS	Tuning window select

Table 8 - Key to Table 7

3.4.3 Synthesizer Division Ratio (2^{14}:2^0 Bits)

The PLL synthesizer interfaces with the LO multiplex output and runs at the desired frequency for down-conversion. The step size at the desired conversion frequency, is equal to the loop comparison frequency.

The programmable division ratio, **2^{14}** to **2^0**, required for a desired conversion frequency, can be calculated from the following formula:

Desired conversion frequency = $\Delta f_{step} \times (2^{14} + 2^{13} + 2^{12} \rightarrow 2^{2} + 2^{1} + 2^{0})$

where: Δf_{step} = Fcomp

3.4.4 RF Gain (RFG Bit)

The RF gain is programmed by setting the **RFG** bit, bit-5 of register byte-4 as required. See also Figure 4, “AGC Control Structure” on page 13.

RFG	Gain Adjust (dB)	
0	0	(reset state)
1	+4	

Table 9 - RFG Register Bit Function

3.4.5 Baseband Pre-Filter Gain Adjust (BA1:0 Bits)

The baseband pre-filter gain is programmed by setting **BA1:0**, bits-4 & 3 of register byte-4 as required. See also Figure 4, “AGC Control Structure” on page 13.

BA1	BA0	Pre-Filter Gain Adjust (dB)	
0	0	0.0	(reset state)
0	1	+4.2	
1	0	+8.4	
1	1	+12.6	

Table 10 - BA1/0 Register Bits Function

3.4.6 Baseband Post-Filter Gain (BG1:0 Bits)

The baseband post-filter gain is programmed by setting **BG1:0**, bits-2 & 1 of register byte-4 as required. See also Figure 4, “AGC Control Structure” on page 13.

BG1	BG0	Post-Filter Gain Adjust (dB)	
0	0	0.0	(reset state)
0	1	+4.2	
1	0	+8.4	
1	1	+12.6	

Table 11 - BG1/0 Register Bits Function

3.4.7 RF Bypass Disable (LEN Bit)

The RF bypass function is disabled by setting **LEN**, bit-0 of register byte-4 to a logic ‘1’. By default, this bit is at a logic ‘0’ at power-up, and therefore the function is enabled. If the function is not required, a power saving of approximately 15% can be made by setting this bit. See also section 2.3 on page 16.

3.4.8 Output Port Controls (P1 & P0 Bits)

Register bits **P1** and **P0**, bit-7 in register bytes-7 & 5 respectively, control the output port pins, P1 & P0, pin numbers 39 & 24 respectively.

Bit P1 or P0	Port state	Logic state (if connected to a pull-up)	
0	High impedance	1	(reset state)
1	Low impedance to Vee (Gnd)	0	

Table 12 - Port Control Bits

3.4.9 Power Down (PD Bit)

Bit-7 of byte-13 controls the **PD** register bit which is an alternative to the SLEEP pin (see “SLEEP - Pin 11” on page 20). Setting the **PD** bit to a logic ‘1’ shuts down the analogue sections of the ZL10038 effecting a saving of about 2/3rds of the power required for normal operation. A logic ’0’ restores normal operation. With either hardware or software power-down, all register settings are unaffected.

3.4.10 Logic Reset (CLR Bit)

Bit-1 of byte-13 controls the **CLR** register bit. When set to a logic ‘1’, this self-clearing bit resets the ZL10036 control logic. Writing a logic ‘0’ has no effect. The following register numbers are reset to their power-on state: 7, 9, 10, 11, 12 & 13. All other register’s contents are unaffected.

3.4.11 Charge Pump Control and Charge Pump Current (CC, C1 & C0 Bits)

Register bit **CC** is programmed by setting bit-2 of register byte-8 and bits **C1** and **C0** by setting bits-6 & 5 of register byte-5. These bits determine the charge pump current that is used on the output of the frequency synthesizer phase detector.

			Typical current in µA	
CC	**C1**	**C0**	**VCO sub-bands 0 - 7**	**VCO sub-bands 8 - 15**
0	0	0	±365	±210
0	0	1	±625	±365
0	1	0	±1065	±625
0	1	1	Invalid Setting	
1	0	0	±210	
1	0	1	±365	
1	1	0	±625	
1	1	1	±1065	

(reset state)

Current limits		
Min.	**Typ.**	**Max.**
±160	±210	±290
±280	±365	±510
±470	±625	±860
±820	±1065	±1470

Table 13 - Charge Pump Currents

3.4.12 Reference Division Ratios (R4:0 Bits)

Register bits **R4:0** control the reference divider ratios as shown in Table 14. They are programmed through bit-4 to bit-0 respectively, in byte-5.

		R4	**0**	**0**	**1**	**1**
		R3	**0**	**1**	**0**	**1**
R2	**R1**	**R0**	**Division Ratios**			
0	**0**	**0**	2	***Illegal states***		
0	**0**	**1**	4	5	6	7
0	**1**	**0**	8	10	12	14
0	**1**	**1**	16	20	24	28
1	**0**	**0**	32	40	48	56
1	**0**	**1**	64	80	96	112
1	**1**	**0**	128	160	192	224
1	**1**	**1**	256	320	384	448

Table 14 - Division Ratios Set with Bits R4 - R0

3.4.13 Baseband Filter Resistor Switching (RSD)

The baseband filters use a resistor switching technique that improves bandwidth and phase matching between the I and Q channels. The bandwidth range is effectively separated into 3 sub-ranges with different resistor values being used in each sub-range. It is possible for the filter bandwidth accuracy to be degraded if the bandwidth setting happens to coincide with one of the two transition points between these regions. This can be overcome by disabling the resistor switching using the **RSD** bit. For optimum filter performance the **RSD** bit should first be enabled so that the correct resistor value is automatically set for the selected bandwidth.

The **RSD** bit (bit-3 of byte-6) controls the resistor switching. With the default setting of logic '0' it is enabled and the correct resistor value automatically chosen. With the **RSD** bit set to a logic '1' then the switching is disabled and this freezes the resistors at their chosen value. The procedure when selecting a new bandwidth setting is to enable then disable the switching; set **RSD** to logic '0' then to logic '1'.

3.4.14 Baseband Filter Bandwidth (BF6:1 & BR4:0 Bits)

Bits 6 to 1 of byte-7 configure bits **BF6** to **BF1** respectively. These bits set a decimal number in the range 0 to 62 (63 is not allowed) to determine the baseband filter bandwidth in conjunction with other values.

Bits 6 to 2 of byte-13 configure bits **BR4** to **BR0** respectively. These bits set the reference divider ratio for the baseband filter. A number in the range 4 to 27 inclusive (values outside this range are not allowed) can be set, with the proviso that the value of f_{xtal}/BR4:0 must also be in the range 575 kHz to 2,500 kHz.

For further details, please also see “Baseband Filter” (sect. 2.4) on page 16 and “Symbol Rate and Filter Calculations” (sect. 4.3) on page 30.

3.4.15 Band Switch Algorithm (VSD Bit)

The controller, which tunes to the appropriate LO and sub band for optimum phase noise performance, can be disabled with the **VSD** bit, if required, allowing manual control. The **VSD** bit is programmed using byte-9, bit-7. The default is for the controller to be enabled, **VSD** = ‘0’, and to disable the controller a logic ‘1’ is written to this bit.

3.4.16 LO Main- & Sub-Band Selection (V2:0 & S3:0 Bits)

If manual control of the LO is selected with the **VSD** bit, bits **V2:0** (main-band) and **S3:0** (sub-band) can be used to set the LO frequency band. Values of **V2:0** from 1 to 6 are valid, values 0 and 7 being used for test purposes only. The prescaler ratio, NLP, is set to '4' for values of **V2:0** from 1 to 3 and to '2' for **V2:0** from 4 to 6.

Table 15 shows typical minimum and maximum frequencies for each VCO and sub band for a varactor voltage (Vvar) range of 3 to 4.5 volts. This is the normal varactor operating voltage, however the VCO will operate at lower voltages if required. The VCO gain is also shown at 3.5 volts varactor voltage.

				VCO1			**VCO2**			**VCO3**		
			Divider	**4**			**4**			**4**		
			V2	**0**			**0**			**0**		
			V1	**0**			**1**			**1**		
			V0	**1**			**0**			**1**		
S3	**S2**	**S1**	**S0**	Min	Max	Kvco	Min	Max	Kvco	Min	Max	Kvco
0	**0**	**0**	**0**	690	699	6.9	881	892	8.9	1068	1081	10.0
0	**0**	**0**	**1**	697	708	7.3	892	905	9.3	1080	1094	10.6
0	**0**	**1**	**0**	706	716	7.8	904	917	9.7	1093	1108	11.2
0	**0**	**1**	**1**	714	726	8.3	917	930	10.1	1107	1122	11.9
0	**1**	**0**	**0**	725	737	8.9	931	946	10.9	1122	1139	13.1
0	**1**	**0**	**1**	735	748	9.6	945	960	11.6	1138	1156	14.1
0	**1**	**1**	**0**	746	761	10.3	959	976	12.4	1154	1174	15.1
0	**1**	**1**	**1**	759	774	11.2	975	992	13.4	1173	1194	16.4
1	**0**	**0**	**0**	769	786	12.2	986	1005	14.5	1182	1205	17.5
1	**0**	**0**	**1**	783	801	13.2	1003	1024	15.8	1203	1227	19.1
1	**0**	**1**	**0**	798	817	14.4	1021	1044	17.2	1224	1251	20.8
1	**0**	**1**	**1**	814	836	15.7	1041	1066	19.0	1248	1278	22.9
1	**1**	**0**	**0**	834	857	17.4	1063	1092	21.7	1275	1309	26.4
1	**1**	**0**	**1**	853	879	19.0	1087	1119	24.4	1303	1341	29.6
1	**1**	**1**	**0**	874	902	20.8	1112	1148	27.5	1334	1376	33.3
1	**1**	**1**	**1**	896	927	23.1	1141	1182	31.6	1368	1415	37.7

				VCO1			**VCO2**			**VCO3**		
			Divider	**2**			**2**			**2**		
			V2	**1**			**1**			**1**		
			V1	**0**			**0**			**1**		
			V0	**0**			**1**			**0**		
S3	**S2**	**S1**	**S0**	Min	Max	Kvco	Min	Max	Kvco	Min	Max	Kvco
0	**0**	**0**	**0**	1380	1399	13.8	1761	1785	17.8	2136	2162	19.9
0	**0**	**0**	**1**	1395	1415	14.6	1785	1809	18.6	2161	2188	21.2
0	**0**	**1**	**0**	1411	1433	15.5	1809	1835	19.3	2186	2215	22.4
0	**0**	**1**	**1**	1429	1451	16.5	1834	1861	20.3	2214	2245	23.9
0	**1**	**0**	**0**	1450	1474	17.9	1862	1891	21.9	2244	2278	26.1
0	**1**	**0**	**1**	1470	1496	19.2	1889	1920	23.2	2276	2312	28.1
0	**1**	**1**	**0**	1493	1521	20.7	1918	1951	24.8	2309	2348	30.2
0	**1**	**1**	**1**	1517	1548	22.4	1949	1985	26.8	2345	2388	32.7
1	**0**	**0**	**0**	1538	1571	24.3	1972	2011	29.1	2365	2410	35.1
1	**0**	**0**	**1**	1565	1601	26.4	2006	2048	31.6	2405	2455	38.3
1	**0**	**1**	**0**	1595	1635	28.7	2042	2088	34.5	2449	2502	41.7
1	**0**	**1**	**1**	1628	1671	31.4	2082	2132	38.1	2497	2555	45.9
1	**1**	**0**	**0**	1667	1714	34.7	2126	2183	43.4	2550	2617	52.9
1	**1**	**0**	**1**	1706	1758	38.0	2174	2238	48.9	2607	2682	59.1
1	**1**	**1**	**0**	1747	1804	41.6	2225	2296	55.1	2668	2752	66.5
1	**1**	**1**	**1**	1793	1855	46.1	2282	2364	63.2	2736	2830	75.4

Table 15 - Frequency Bands and VCO Gain

3.4.17 LO Sample Rate (LS2:0 Bits)

Bits LS2:0 (bit-2 to bit-0 respectively in byte-10) set the LO sample rate according to the following table:

LS2	LS1	LS0	Sample Rate	
0	0	0	$F_{comp}/4$	
0	0	1	$F_{comp}/8$	(reset state)
0	1	0	$F_{comp}/16$	
0	1	1	$F_{comp}/32$	
1	0	0	$F_{comp}/64$	
1	0	1	$F_{comp}/128$	
1	1	0	$F_{comp}/512$	
1	1	1	$F_{comp}/2048$	

Table 16 - LO Sample Rate Data

3.4.18 LO Window Level (WS, WH2:0 & WL2:0 Bits)

Byte-11 allows the user to change the lock and unlock window voltages that the tuning controller uses in comparison with the Vvar input. Setting the **WS** bit to ‘0’ allows the lock levels to be altered, or if set to ‘1’, the unlock levels are written. The **WH2:0** bits set the upper levels and the **WL2:0** bits set the lower levels in each case. Please see “Power-On Software Initialization” (sect. 4.1) on page 30 for recommended values.

			Lock		Unlock	
		WS	0		1	
WH2	WH1	WH0		Upper		Upper
WL2	WL1	WL0	Lower		Lower	
0	0	0	1.16	1.54	1.08	1.61
0	0	1	1.64	2.01	1.56	2.08
0	1	0	**2.11**	2.47	**2.03**	2.55
0	1	1	2.57	2.94	2.50	3.01
1	0	0	3.03	3.43	2.95	3.51
1	0	1	3.49	3.89	3.42	3.97
1	1	0	3.95	4.36	3.88	4.43
1	1	1	4.41	**4.82**	4.34	**4.89**

Key: **Reset Values**

Table 17 - LO Window Levels

3.4.19 LO Window Relaxation (WRE Bit)

In the event of the controller failing to lock due to the lock window being too narrow, the window is automatically widened when **WRE** (byte-11 bit-0) is ‘1’ in order to achieve lock. The **WRE** bit, when set to logic ‘0’, disables this facility.

3.4.20 LO Test (TL Bit)

For test purposes, the LO clock divided by the prescaler ratio can be output on the LOTEST pin by setting bit **TL** (byte-13 bit-0) to a logic ‘1’. By default this output is off, i.e., the **TL** bit is at logic ‘0’.

4.0 Software

In normal operation, only initialization, channel (frequency) changes and symbol rates require programming intervention. Note that the PLL comparison frequency is set by the crystal frequency divided by the PLL reference divide ratio. In the following examples of register settings, binary values are frequently used, indicated as e.g., 0110_2.

4.1 Power-On Software Initialization

a. **Bytes 2 + 3:** 2^{14} - 2^0 = desired channel frequency/PLL comparison frequency (VCO = 3, sub-band = 0, divider = 4 is default, means that the local oscillator frequency will be about 1.1 GHz).

b. **Byte 4:** BA1:0 = 01_2 for initial baseband filter input level.

c. **Byte 4:** BG1:0 = 01_2 for target baseband filter output level.

d. **Byte 4:** LEN = 1 if the RF loop through is to be disabled.

e. **Byte 5:** R4:0 = PLL reference divider for desired comparison frequency.

f. **Byte 8:** PS = 0 to give a pre-scaler ratio of 16/17. Bits ‘0’ & ‘1’ should be set to 00_2.

g. **Byte 11:** WL2:0 and WH2:0 may require different values from the defaults. Recommended settings are:

	WS	WH2	WH1	WH0	WL2	WL1	WL0	WRE	Lower V	Upper V
Lock	0	1	1	0	1	0	1	1	3.49	3.89
Unlock	1	1	1	1	1	0	0	1	2.95	4.89

Table 18 - LO Recommended Window Levels

h. **Byte 13:** BR4:0 = Crystal frequency in use (see also 4.3.3.1 on page 31).

4.2 Changing Channel

Bytes 2 + 3: 2^{14} - 2^0 = Channel frequency/PLL comparison frequency.

4.3 Symbol Rate and Filter Calculations

4.3.1 Determining the Filter Bandwidth from the Symbol Rate

$f_{bw} = (\alpha * \text{symbol rate})/(2.0 * 0.8) + f_{offs}$

where:

α = 1.35 for DVB or 1.20 for DSS, and is the roll-off of the raised-root cosine filter in the transmitter,

f_{offs} is the total offset of the received signal due to all causes (LNB drift, synthesizer step size, etc) and is read back from the demodulator,

and f_{bw} is the -3 dB roll-off of the filter for: 8 MHz $\le f_{bw} \le$ 35 MHz.

For low symbol rates, the energy content within the bandwidth of the filters reduces significantly so incrementing the baseband post-filter gain helps recover the signal level for the demodulator.

N.B. During channel acquisition or re-acquisition, the filter must be set to its maximum value.

4.3.2 Calculating the Filter Bandwidth

The -3 dB bandwidth of the filter (Hz) is given by the following expression:

Equation 1 - $$f_{bw} = \frac{f_{xtal}}{BR} \times (BF + 1) \times \frac{1}{K}$$

Where:

f_{bw} = Baseband filter –3 dB bandwidth (Hz) which should be within the range $8\mathrm{MHz} \le f_{bw} \le 35\mathrm{MHz}$.

f_{xtal} = Crystal oscillator reference frequency (Hz).

K = 1.257 (constant).

BF = Decimal value of the register bits BF6:BF1, range 0 - 62.

BR = Decimal value of the bits BR4:BR0 (baseband filter reference divider ratio), range 4 - 27.

where: 575 kHz $\le \frac{f_{xtal}}{BR} \le$ 2.5 MHz.

The digital nature of the control loop means that the filter bandwidth setting is quantized: the difference between the desired filter bandwidth and the actual filter bandwidth possible due to discrete settings causes a bandwidth error. In order to minimize this bandwidth error, the maximum filter bandwidth setting resolution is needed. From the limits given above, the best resolution possible is 575 kHz/1.257 = 457.4 kHz. However if this resolution is used, the maximum bandwidth with BF = 62 is only 28.82 MHz, below the maximum of 35 MHz. Therefore for filter bandwidths greater than 28.82 MHz the resolution must be decreased. For filter bandwidths around 35 MHz the resolution is typically reduced to 698 kHz/1.257 = 555.3 kHz.

4.3.3 Determining the Values of BF and BR

4.3.3.1 Calculating the Value of BR

The above description can be described mathematically as:

For $f_{bw} \le$ 28.82 MHz,

Equation 2 - $$BR = \frac{f_{xtal}}{575\mathrm{kHz}}.$$

For $f_{bw} >$ 28.82 MHz,

Equation 3 - $$BR = \frac{f_{xtal}}{f_{bw}} \times (62 + 1) \times \frac{1}{K}.$$

These equations can give non-integer results so rounding must be performed. The values for BR should be rounded DOWN to the nearest integer this ensures that $\frac{f_{xtal}}{BR}$ will not be below 575 kHz and that the maximum programmable bandwidth will not be below the desired bandwidth due to rounding.

4.3.3.2 Calculating the Value of BF

Equation 4 - $$BF = \left(\frac{f_{bw}}{f_{xtal}} \times BR \times K\right) - 1$$

For non-integer values of BF, the result should be simply rounded to the nearest integer to give the value for BF6:1.

4.3.4 Filter Bandwidth Programming Examples

Example 1, conditions: f_{xtal} = 10.111 MHz, f_{bw} = 9 MHz

Because f_{bw} is below 28.2 MHz, the value of BR can be evaluated with equation 2:

$$BR = \frac{f_{xtal}}{575kHz} = \frac{10.111MHz}{575kHz} = 17.583$$

This result should be rounded down to 17 to ensure that the result is not below the 575 kHz limit. Using this value for BR, equation 4 can be evaluated:

$$BF = \left(\frac{f_{bw}}{f_{xtal}} \times BR \times K\right) - 1 = \left(\frac{9MHz}{10.11MHz} \times 17 \times 1.257\right) - 1 = 18.02285$$

The result can be rounded to the nearest value, i.e. BF = 18.

Example 2, conditions: f_{xtal} = 10.111 MHz, f_{bw} = 34.6 MHz

In this case, f_{bw} is above 28.2 MHz so using equation 3 to solve for BR:

$$BR = \frac{f_{xtal}}{f_{bw}} \times (63) \times \frac{1}{K} = \frac{10.111MHz}{34.6MHz} \times (63) \times \frac{1}{1.257} = 14.647$$

Using equation 4, this time with the rounded-down value of 14 for BR:

$$BF = \left(\frac{f_{bw}}{f_{xtal}} \times BR \times K\right) - 1 = \left(\frac{34.6MHz}{10.11MHz} \times 14 \times 1.257\right) - 1 = 59.227$$

Rounding to the nearest integer thus gives a value of 59 for BF.

4.4 Programming Sequence for Filter Bandwidth Changes

a. **Byte 6:** Set RSD = 0 to re-enable baseband filter resistor switching.

b. **Byte 7:** Set BF6:1 to the value derived in 4.3.3.2, “Calculating the Value of BF“ on page 32.

c. **Byte 6:** Set RSD = 1 to disable baseband filter resistor switching. This must happen no sooner than a certain time after (b.). This minimum time equals BR/(32 * f_{xtal}) seconds, where BR is the decimal value of byte BR and f_{xtal} is the reference crystal frequency.

5.0 Application Notes

5.1 Thermal Considerations

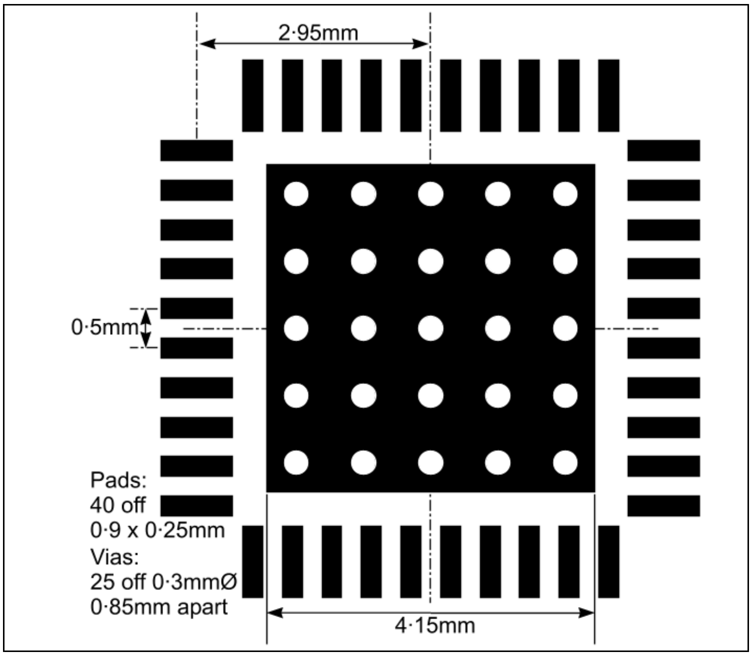


Figure 12 - Copper Dimensions for Optimum Heat Transfer

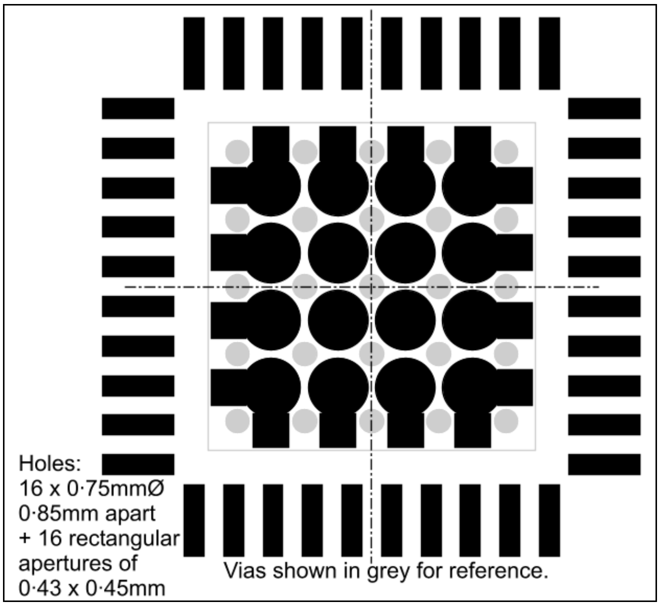


Figure 13 - Paste Mask for Reduced Paste Coverage

The ZL10038 uses the 40-pin QFN package with a thermal ‘paddle’ in the base, which has a very high thermal conductivity to the die, as well as low electrical resistance to the Vee connections. The ZL10038 has a fairly high power density, and if the excess heat is not efficiently removed, it will rapidly overheat beyond the 125°C limit, and affect the performance or could even cause permanent damage to the device.

The paddle is designed to be soldered to a size-matched pad on the PCB (see Figure 10) which is thermally connected to an efficient heat sink. The heat sink can be as simple as an area of copper ground plane on the underside of the board, thereby reducing the system cost. To transfer the heat from the paddle to the underside of the board, an array of 25 x 0·3 mmØ vias are used between the topside pad, which will be soldered to the paddle, and the ground plane on the underside of the board. It is also possible to use a smaller number of larger vias, e.g., 16 x 0·5 mmØ, but this arrangement is marginally less efficient.

The area of copper in the ground plane must be at least 2,000 mm² for 1 oz copper. If 2 oz copper board is used or if multiple ground planes are available, as with a four-layer board, the area could be reduced somewhat, but in general it is better to have the maximum cooling possible, as reliability will always be enhanced if lower temperatures are maintained.

While it is possible to use a paste mask that simply duplicates the aperture for the 4.15 mm sq. paddle, the quantity of solder paste under the device can cause problems and it is preferable to reduce the coverage to a level between 50% and 80% of the area. The pattern shown in Figure 11 reduces the coverage to approximately 60%, which should reduce out-gassing from under the device and improve the stand-off height of the package from the board.

A very useful publication giving further details is: “Application Notes for Surface Mount Assembly of Amkorþs MicroLeadFrame (MLF) Packages” which can be found on: www.amkor.com

5.2 Crystal Oscillator Notes

Component	4 MHz	10 MHz
C10	47 pF	100 pF
C11	47 pF	100 pF
Note: C12, a 10 pF (15 pF for 10 MHz) capacitor may be added between the crystal and Gnd if an oscillator output is required. Output is from the crystal/capacitor junction.		

Table 19 - Crystal Capacitor Values for 4 MHz and 10 MHz Operation
(component numbering refers to the example schematic, Figure 2)

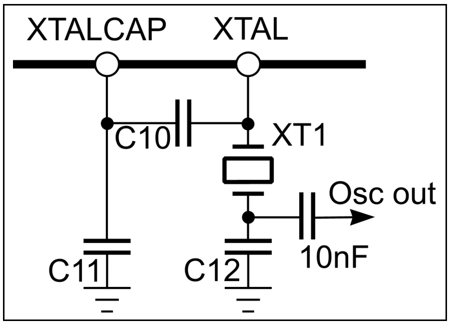


Figure 14 - Typical Oscillator Arrangement with Optional Output

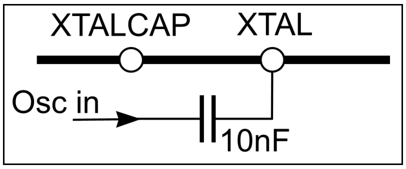


Figure 15 - Typical Arrangement for External Oscillator

6.0 Electrical Characteristics

6.1 Test Conditions

The following conditions apply to all figures in this chapter, except where notes indicate other settings.

Tamb = -10° to 85°C, Vee= 0 V, All Vcc supplies = 5 V±5%

RF gain adjust = +0 dB, prefilter = +4.2 dB and postfilter = 4.2 dB. RFG=0, BA1=0, BA0=1, BG1=0, BG0=1

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

6.2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Supply voltage	VccBB, VccDIG, VccLO, VccRF, VccTUNE	-0.3	5.5	V	w.r.t. Vee
Storage temperature	T_{STG}	-55	150	°C	
Junction temperature	T_j		125	°C	
Voltage on SDA & SCL		-0.3	6	V	Vcc = Vee to 5.25 V
Voltage on DRIVE		-0.3	VccTUNE+0.3	V	
Voltage on RFIN, RFBYPASS and inverted equivalents		-0.3	VccRF+0.3	V	
Voltage on RFAGC					
Voltage on Vvar		-0.3	VccLO+0.3	V	
Voltage on LOTEST					
Voltage on IOUT, QOUT, IDC, QDC and inverted equivalents		-0.3	VccBB+0.3	V	
Voltage on P1					
Voltage at DIGDEC		-0.3	3.6	V	
Voltage on PUMP		-0.3	VccDIG+0.3	V	
Voltage on SLEEP and P0					
Voltage on ADD, XTAL, XTALCAP and LOCK		-0.3	DIGDEC+0.3	V	
Sink current, P0 or P1			20	mA	Each output
ESD protection, pins 31 & 32[1]		0.5		kV	To Mil-std 883B method 3015 cat1
pins 1-30, 33-40		2.0		kV	

[1] ESD protection can be increased by adding a protection diode (D1) to the input circuit as shown in the application circuit (Figure 2).

6.3 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Notes
Supply voltage	VccBB, VccDIG, VccLO, VccRF, VccTUNE	4.75	5.25	V	w.r.t. Vee
Operating temperature	T_{OP}	-10	85	°C	

6.4 DC Characteristics

Pins	Characteristic	Min.	Typ.	Max.	Units	Conditions	
Normal operating conditions							
All Vcc pins: 5, 6, 18, 19, 26, 29, 36, 37	Supply current					RF bypass	filter b.w.
			210	259	mA	disabled	minimum
			228	281	mA		maximum
			243	300	mA	enabled	minimum
			261	322	mA		maximum
			82	107	mA	disabled	sleep mode
			115		mA	enabled	
QOUT, $\overline{QOUT}$, IOUT, $\overline{IOUT}$: 3, 4, 7, 8	Output impedance		25		Ω	Single-ended	
	Output load	1		15	kΩ pF	Maximum load, which can be applied to output, single-ended. If operated single ended unused output should be unloaded	
QDC, $\overline{QDC}$, $\overline{IDC}$, IDC: 1, 2, 9, 10	Bias voltage		3.8		V		
	Output impedance		11		kΩ		
SCL, SDA: 12, 13	Input high voltage	2.3		5.5	V		
	Input low voltage	0		1	V		
	Input current	-10		10	µA	Input voltage =Vee to VccDIG	
	Leakage current			10	µA	Input voltage = Vee to 5.5 V, VccDIG=Vee	
	Hysteresis		0.4		V		
SDA: 13	Output voltage			0.4	V	Isink = 3 mA	
				0.6	V	Isink = 6 mA	
PUMP: 21	Charge pump leakage		+-3	+-20	nA	Vpin = 1.8V	
	Charge pump current					Vpin = 1.8 V. See Table 13 on page 26	

Pins	Characteristic	Min.	Typ.	Max.	Units	Conditions	
DRIVE: 20	Max. voltage	VccTUNE-0.2			V	On-chip 3 kohm load resistor to VccTUNE	
	Min. voltage			0.3	V		
XTAL, XTALCAP: 14, 15	Recommended crystal E.S.R.	10		200	Ω	Parallel resonant crystal	
Vvar: 23	Input current	-1		1	mA	Vee <= Vvar <= 1.7 V (on-chip varactors forward biased)	
		-25		25	µA	1.7 V <= Vvar <= Vcc	
P0, P1: 24, 39	Sink current	10			mA	At Vport = 0.7 V	
	Leakage current			10	µA	Vport = Vcc	
LOCK: 25	Low output voltage			0.5	V	Out of lock	at 1 mA
	High output voltage	DigDec-0.5			V	In lock	
	Load current			1	mA		
ADD: 16	Input high current			1	mA	Vin=DIGDEC	
	Input low current			-0.5	mA	Vin=Vee	
SLEEP: 11	Input high voltage	2		3.6	V	Sleep enabled	
	Input low voltage	Vee		0.5	V	Normal mode	
	Input DC current			10	µA	Vin=Vee to DIGDEC	
RFAGC: 34	Leakage current	-150		150	µA	Vee <= Vagc<= Vcc	
LOTEST: 38	Output impedance		100		Ω		
	Bias voltage		3.3		V		

6.5 AC Characteristics

Characteristic	Min.	Typ.	Max.	Units	Conditions
System (See [1])					
Noise figure, DSB		9		dB	At -70 dBm operating level [2]
		12		dB	At -60 dBm operating level [2]
		10		dB	At -70 dBm operating level
		13		dB	At -60 dBm operating level
Variation in NF with RF gain adjust			-1	dB/dB	Above –60 dBm operating level [2] See Figure 8 on page 15
Conversion gain					
Maximum	72	78		dB	Vagc = 0.75 V
Minimum		6	10	dB	Vagc = 4.25 V
AGC control range	68	72		dB	AGC monotonic, Vagc from Vee to Vcc

Characteristic	Min.	Typ.	Max.	Units	Conditions
System IM2			-35 -40	dBc dBc	See [3] See [4]
System IM3			-15	dBc	See [5]
Variation in system second order intermodulation intercept			-1	dB/dB	See Figure 6 on page 14 and [6]
Variation in system third order intermodulation intercept			-1	dB/dB	See Figure 7 on page 14 and [7]
Input compression	-10	-6		dBm	See [8]
LO second harmonic interference level		-50	-35	dBc	See [9], all gain settings
LNA second harmonic interference level		-35	-20	dBc	See [10]
Quadrature gain match	-0.6		0.6	dB	Filter bandwidth settings 8-35 MHz, up to 0.8 x filter -3 dB bandwidth
Quadrature phase match	-3		3	deg	
I & Q channel in band ripple			1	dB	
I/Q Crosstalk			21	dB	
Synthesizer and other spurii on I & Q outputs			-30	dBc	All gain settings below 68 dB
			-25	dBc	At maximum gain. Linearly interpolated between max. and 68 dB gain, see [11]
LO reference sideband spur level on I & Q outputs			-40	dBc	Synthesizer phase detector comparison frequency 500-2000 kHz
In band LO leakage to RF input			-65	dBm	Within RF band 950-2150 MHz
			-55	dBm	Within RF band 30-950 MHz
RF bypass					
Gain	1.5		5.5	dB	
NF		10	13	dB	
OPIP3		9		dBm	See [12]
OPIP2	26			dBm	See [13]
Output return loss	9			dB	$Z_0 = 75\ \Omega$. See Figure 9 on page 16, with output matching as in Figure 2 on page 2. Bypass enabled or disabled.
Forward isolation		25		dB	950-2150 MHz Single-ended to single-ended, bypass disabled
Reverse isolation		25		dB	
In band LO leakage			-65	dBm	
Converter					
Converter Input return loss (pins RFIN & $\overline{\text{RFIN}}$)	8	10		dB	$Z_0 = 75\ \Omega$. See Figure 9 on page 16. With input matching as in Figure 2 on page 2. Bypass enabled or disabled

Characteristic	Min.	Typ.	Max.	Units	Conditions	
L.O. SSB phase noise		-84 -84 -108		dBc/Hz dBc/Hz dBc/Hz	@ 1 kHz offset @ 10 kHz offset @ 100 kHz offset	Measured either, at baseband output of 10 MHz, PLL loop bandwidth circa 15 kHz, or at LOTEST output[14].
		-120	-110 -132	dBc/Hz dBc/Hz	@ 1 MHz offset Noise floor.	Measured at LOTEST output.
L.O. integrated phase jitter			2	deg	See[15]	
LOTEST output amplitude		200		mVp-p	Test output enabled into 50 Ω	
Baseband Filters (specifications apply with both single-ended and differential load unless otherwise stated)						
Bandwidth	4		40	MHz	See 2.4, “Baseband Filter“ on page 16. Maximum load as specified	
Bandwidth absolute tolerance	-5		+5	%	Filter bandwidth setting, fset, 8-35 MHz. Slave oscillator enabled, see [16]	
Channel bandwidth match	-1		+1	%	Filter bandwidth settings 8-35 MHz	
Characteristic response					All bandwidth settings, see Figure on page 17	
Channel gain match					Included in system gain match	
Channel phase match						
Output total harmonic distortion			-26	dBc	At 0.8 V p-p, single-ended. Maximum load as specified	
Output limiting	1.0			Vp-p	Level at hard clipping, single-ended. Maximum load as specified	
Synthesizer						
Crystal frequency	4		20	MHz	See Table 19 on page 34.	
External reference input frequency	4		20	MHz	Sinewave coupled through 10 nF blocking capacitor to pin XTAL. XTALCAP is left open.	
External reference drive level	0.2		0.5	Vp-p		
Phase detector comparison frequency	31.25		2000	kHz		
Equivalent phase noise at phase detector		-148		dBc/Hz	SSB, within loop bandwidth. Phase detector comparison frequency = 1 MHz	
LO division ratio	240		32767			
Maximum SCL clock rate	100			kHz		

1. All power levels are referred to 75 Ω and assume an ideal impedance match: 0 dBm = 109 dBmV. System specifications refer to total cascaded system of converter/AGC stage and baseband amplifier/filter stage with maximum terminating load as specified in “Recommended Operating Conditions” on page 36, with output amplitude of 0.5 Vp-p differential.
2. See Figure 8, RF gain adjust = +4 dB, prefilter = +4.2 dB and postfilter = 0 dB, RFG = 1, BA1 = 0, BA0 = 1, BG1 = 0, BG0 = 0
3. ’Baseband defined IM2’. AGC set to deliver an output of 0.5 Vp-p with an input CW @ frequency fc of -25 dBm. Two undesired tones at fc+146 and fc+155 MHz @ -11 dBm generating output intermodulation spur at 9 MHz. Baseband filter at 22 MHz bandwidth setting.

4. ’Front end defined IM2’. LO set to 2145 MHz and AGC set to deliver a 5 MHz output of 0.5 Vp-p with a desired input CW @ frequency 2150 MHz of -45 dBm. Sum IM2 product from two undesired tones at 1.05 and 1.1 GHz at -25 dBm converted to 5 MHz baseband with desired input removed. Baseband filter at 22 MHz bandwidth setting.

5. ’IM3’. AGC set to deliver an output of 0.5 Vp-p with an input CW @ frequency fc of -30 dBm. Two undesired tones at fc+55 and fc+105 MHz at -11 dBm generating output intermodulation spur at 5 MHz. Baseband filter at 22 MHz bandwidth setting.

6. ’Front end defined’ variation in IP2 from two undesired tones at 1.05 and 1.1 GHz at 20 dBc relative to desired at 2.15 GHz converted to 5 MHz baseband with LO tuned to 2.145 GHz with AGC set to deliver 0.5 Vp-p differential on desired, as desired amplitude is varied from -45 dBm to -75 dBm.

7. Variation in IP3 product from two undesired tones at fc+55 and fc+105 MHz at 19 dBc relative to desired at fc converted to 5 MHz baseband with LO tuned to desired at fc GHz with AGC set to deliver 0.5 Vp-p differential on desired, as desired amplitude is varied from -30 dBm to -75 dBm.

8. AGC set to deliver an output of 0.5 Vp-p with an input CW @ frequency fc of -35 dBm. Input compression defined as the level of interferer at 100 MHz offset, which leads to a 1 dB compression in gain.

9. The level of 2.01 GHz downconverted to baseband relative to 1.01 GHz with the oscillator tuned to 1 GHz, measured with no input pre-filtering.

10. The level of second harmonic of 1.01 GHz input at -20 dBm downconverted to baseband relative to 2.01 GHz at -35 dBm with the oscillator tuned to 2 GHz, measured with no input pre-filtering gain set to deliver 0.5 Vp-p on 2.01 GHz CW signal. RF gain adjust = +4 dB, prefilter = +4.2 dB and postfilter = 0 dB RFG = 1, BA1 = 0, BA0 = 1, BG1 = 0, BG0 = 0

11. Within 0-100 MHz band, RF input set to deliver 0.5 Vp-p on output. RF gain adjust = +4 dB, prefilter = +4.2 dB and postfilter = 0 dB RFG = 1, BA1 = 0, BA0 = 1, BG1 = 0, BG0 = 0

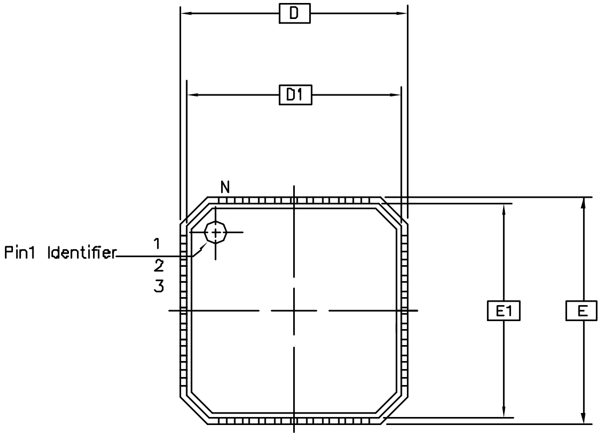
12. Two input tones at fc+50 and fc+100 MHz at -9 dBm generating output intermodulation spur at fc.

13. Sum IM2 product from two input tones at 1.05 and 1.1 GHz at -9 dBm converted to 2150 MHz.

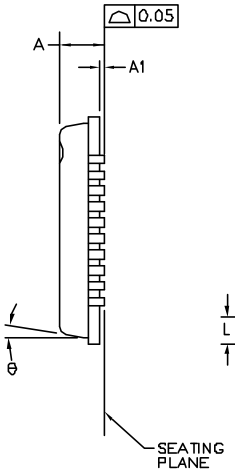
14. PLL loop bandwidth ~15 kHz, comparison frequency 1 - 2 MHz.

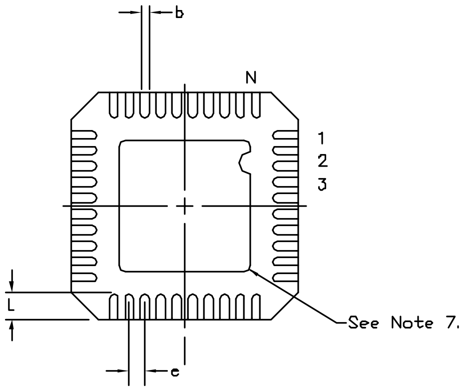
15. Integrated rms LO jitter measured from 1 kHz to 15 MHz, PLL loop bandwidth 15 kHz. Varactor voltage = 3.5 volts.

16. RSD = 0 for 8 MHz <= fset <= 20 MHz, RSD = 1 for 20 MHz <= fset <= 35 MHz.



TOP VIEW





BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS MIN.	MAX.
A	–	0.90
A1	0.00	0.05
b	0.18	0.30
D	6.00 BSC	
D1	5.75 BSC	
E	6.00 BSC	
E1	5.75 BSC	
N	40	
Nd	10	
Ne	10	
e	0.50 BSC	
L	0.30	0.50
θ	0°	12°

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS IN X & Y DIRECTION RESPECTIVELY.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. PACKAGE WARPAGE MAX 0.05mm.
6. NOT TO SCALE.
7. DIMENSION OF THE EXPOSED METAL PAD MAY BE UPTO 0.20MM SMALLER THAN THE NOMINAL DIE PAD DIMENSION
   – SEE LEADFRAME DRAWING FOR SPECIFIC PADDLE DIMENSION.

ISSUE	1	2		
ACN				
DATE	17Feb04	20Feb04		
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