

STK12C68 CMOS nvSRAM 8K x 8 High Performance AutoStore Monvolatile Static RAM

FEATURES

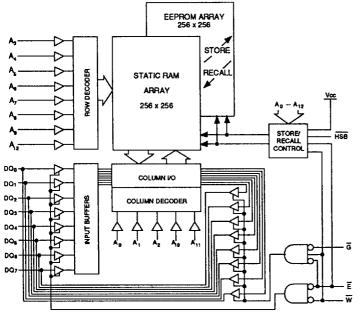
- 30, 35 and 45ns Access Times
- 15 mA I_{CC} at 200ns Access Speed
- Automatic STORE to EEPROM on Power Down
- Hardware or Software initiated STORE to EEPROM
- Automatic STORE Timing
- 100,000 STORE cycles to EEPROM
- 10 year data retention in EEPROM
- · Automatic RECALL on Power Up
- Software initiated RECALL from EEPROM
- Unlimited RECALL cycles from EEPROM
- Single 5V±10% Operation
- Commercial and Industrial Temperatures
- · Available in multiple standard packages

DESCRIPTION

The Simtek STK12C68 is a fast static RAM (30, 35 and 45ns), with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the STORE operation) take place automatically upon power down using charge stored in an external 100 μF capacitor. Transfers from the EEPROM to the SRAM (the RECALL operation) take place automatically on power up. Software sequences may also be used to initiate both STORE and RECALL operations. A STORE can also be initiated via a single pin.

The STK12C68 is available in the following packages: a 28-pin 300 mil plastic or ceramic DIP, a 28-pin 600 mil plastic DIP and a 28-pin SOIC. MIL-STD-883 and Standard Military Drawing (SMD 5962-94599) devices are also available.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS

_		ı	
VCAP C	\smile_{*}	⊒ v∞	×
A.a∐ 2	27	⊒ W	
A, 🛚 3	26) HSI	3
A s C 4	8	D 48	
A 5 🗆 5	24	D 4.	
A4C s	23	D 411	
A3[7	22	ם ב	
	21	A 1	
^, <u></u> ,	20	D E	
A 0 0 10	19	<u> </u>	7
ᅈᆲᆸᇷ	18	88	4
100, □ 12		b ∞	
DO 2 13		L	
V88 🗆 14		Б _ю	
` ** 'L''		Γ	•
28 - 600 PD	IP 28	- 350	SOIC
20 200 PC			CDIB

PIN NAMES

A ₀ - A ₁₂	Address Inputs
W	Write Enable
DQ ₀ - DQ ₇	Data in/Out
ш	Chip Enable
G	Output Enable
V _{CCX}	Power (+5V)
V _{SS}	Ground
V _{CAP}	Capacitor
HSB	Hardware Store/Busy

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to VSS	0.6V to 7.0V
Voltage on DQ ₀₋₇ and G	0.5V to (V _{CC} +0.5V)
Temperature under bias	55°C to 125°C
Storage temperature	65°C to 150°C
Power dissipation	
DC output current	

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

(One output at a time, one second duration)

DC CHARACTERISTICS

 $(V_{CC} = 5.0V \pm 10\%)^d$

		COMM	ERCIAL	INDUS	TRIAL			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES	
CC1 b	Average V _{CC} Current		85		95	mA	t _{AVAV} = 30ns	
001			80		85	mA	t _{AVAV} = 35ns	
			75		80	mA	t _{AVAV} = 45ns	
l _{CC2}	Average V _{CC} Current During STORE		6		7	mA	All inputs ≤ 0.2V or ≥ (V _{CC} - 0.2V)	
lcc3 ^b	Average V _{CC} Current		15		15	mA	E ≤ 0.2V, W ≥ (V _{CC} - 0.2V)	
	at t _{AVAV} = 200ns						others ≤ 0.2V or ≥ (V _{CC} - 0.2V)	
lcc4	Average V _{CC} current during AutoStore™ Cycle		4		4	mA	All inputs ≤ 0.2V or ≥ (V _{CC} - 0.2V)	
l _{SB₁} c	Average V _{CC} Current		35		39	mA	t _{AVAV} = 30ns	
•	(Standby, Cycling TTL Input Levels)		32		35	mA	t _{AVAV} = 35ns	
			28		32	mA	1 _{AVAV} = 45ns	
							E ≥ V _{iH} ; all others cycling	
lsB2°	Average V _{CC} Current		3		3	mA	E ≥ (V _{CC} - 0.2V)	
•	(Standby, Stable CMOS Input Levels)						all others $V_{IN} \le 0.2V$ or $\ge (V_{CC} - 0.2V)$	
I _{ILK3}	Input Leakage Current (Any Input)		±1		±1	μΑ	V _{CC} = max	
						ì	V _{IN} = V _{SS} to V _{CC}	
OLK	Off State Output Leakage Current		±5		±5	μА	V _{CC} = max	
							V _{OUT} = V _{SS} to V _{CC}	
V _{IH}	Input Logic "1" Voltage	2.2	V _{cc+.5}	2.2	V _{CC} +.5	٧	All Inputs	
V _{IL}	Input Logic "0" Voltage	V _{\$5} 5	0.8	V _{SS} 5	0.8	ν	All Inputs	
V _{OH}	Output Logic "1" Voltage	2.4		2.4		٧	I _{OUT} = -4mA except HSB	
V _{OL}	Output Logic "0" Voltage		0.4		0.4	٧	I _{OUT} = 8mA except HSB	
TA	Operating Temperature	0	70	-40	85	ా		

Note b: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing ₹ ≥ VIH will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d: VCC reference levels throughout this datasheet refer to VCCX if that is where the power supply connection is made, or VCAP if VCCX is connected to ground.

AC TEST CONDITIONS

Input Pulse Levels	. V _{ss} to 3V
Input Rise and Fall Times	
Input and Output Timing Reference Levels	1.5V
Output Load S	ee Figure 1

CAPACITANCE[®] (T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C _{IN}	Input Capacitance	8	рF	ΔV = 0 to 3V
C _{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

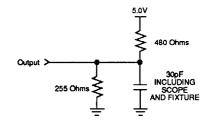


Figure 1: AC Output Loading

SRAM MEMORY OPERATION

READ CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)^d$

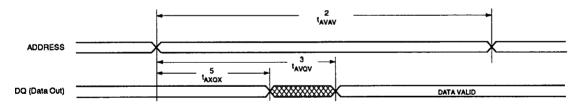
	SYMBOL	.s		STK12	C68-30	STK12	C68-35	STK12C68-45		
NO.	#1, #2	Alt,	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
1	t _{ELOV}	1 _{ACS}	Chip Enable Access Time		30		35		45	ns
2	† _{AVAV}	t _{RC}	Read Cycle Time	30		35		45		ns
3	1 _{AVQV} g	1 _{AA}	Address Access Time		30		35		45	ns
4	t _{GLOV}	t _{OE}	Output Enable to Data Valid		15		20		25	ns
5	taxox	tон	Output Hold After Address Change	5		5		5		ns
6	t _{ELOX}	t _{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t _{EHQZ} h	t _{HZ}	Chip Disable to Output Inactive		15		17		20	ns
8	t _{GLOX}	toLZ	Output Enable to Output Active	0		0		0		ns
9	t _{GHOZ} h	tonz	Output Disable to Output Inactive		15		17		20	ns
10	[†] ELICCH [®]	t _{PA}	Chip Enable to Power Active	0		0		0		ns
11	[†] EHICCL ^{0,●}	t _{PS}	Chip Disable to Power Standby		30		35		45	ns

Note c: Bringing E≥ V_{IH} will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

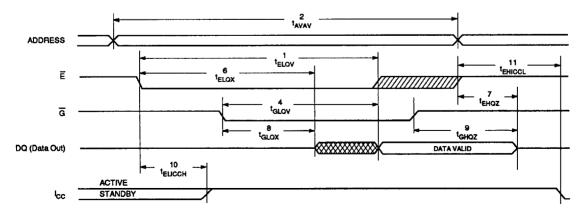
Note e: Parameter guaranteed but not tested.

Note 1: For READ CYCLE \$1 and \$2, \overline{W} is high for entire cycle. Note g: Device is continuously selected with \overline{E} low and \overline{G} low. Note h: Measured \pm 200mV from steady state output voltage.

READ CYCLE #1 f,g



READ CYCLE #2 f



WRITE CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)^d$

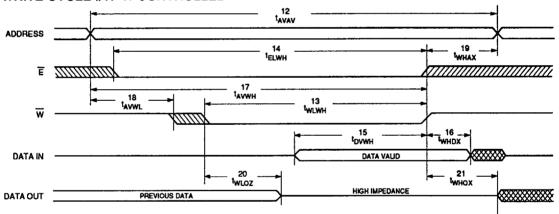
	S	YMBOLS			STK12	C68-30	STK12	C68-35	STK12C68-45		UNITS
NO.	#1	#2	Alt	PARAMETER	MIN	MAX	MEN	MAX	MIN	MAX	UNITS
12	t _{avav}	[†] AVAV	twc	Write Cycle Time	30		35		45		N8
13	^t wLWH	t _{wteh}	t _{wp}	Write Pulse Width	25		30		35		ns
14	t _{ELWH}	^t eleh	tcw	Chip Enable to End of Write	25		30		35		N\$
15	^t ovwH	† _{DVEH}	tow	Data Set-up to End of Write	15		18		20		กร
16	WHDX	t _{EHDX}	t _{DH}	Data Hold After End of Write	0		0		0		ns
17	t _{avwh}	t _{AVEH}	t _{AW}	Address Set-up to End of Write	25		30		35		ns
18	I _{AVWL}	tAVEL	t _{AS}	Address Set-up to Start of Write	0		0		0		ns.
19	WHAX	t _{EHAX}	t _{wr}	Address Hold After End of Write	0		0		0		ns
20	Mroz _{p1}		t _{wz}	Write Enable to Output Disable		15		17		20	ns
21	WHOX		tow	Output Active After End of Write	5		5	Ī	5		ns

Note h: Measured ±200mV from steady state output voltage.

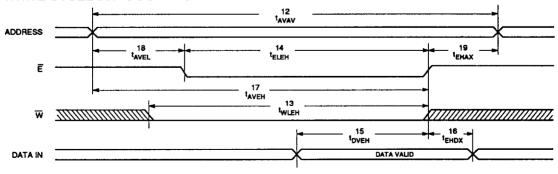
Note I: Ē or W̄ must be ≥VIH during address transitions.

Note]: If \overline{W} is low when \overline{E} goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: W CONTROLLED I



WRITE CYCLE #2: E CONTROLLED



DATA OUT HIGH IMPEDANCE

NONVOLATILE MEMORY OPERATION

MODE SELECTION

Ē	W	HSB	A ₁₂ - A ₀ (hex)	MODE	1/0	POWER	NOTES
Н	X	Н	X	Not Selected	Output High Z	Standby	
Ļ	Н	Н	Х	Read SRAM	Output Data	Active	I
L	L	Н	Х	Write SRAM	Input Data	Active	
L	Н	Н	0000	Read SRAM	Output Data	Active	k,l
			1555	Read SRAM	Output Data		k,i
			OAAA	Read SRAM	Output Data		k,l
			1FFF	Read SRAM	Output Data		k,l
			10F0	Read SRAM	Output Data		k,i
			0F0F	Nonvolatile STORE	Output High Z		k
L	н	Н	0000	Read SRAM	Output Data	Active	k,i
			1555	Read SRAM	Output Data		k,l
			OAAA	Read SRAM	Output Data		k,i
			1FFF	Read SRAM	Output Data	1	k,i
			10F0	Read SRAM	Output Data		k,i
			OFOE	Nonvolatile RECALL	Output High Z	1	k
X	Х	L	Х	STORE/Inhibit	Output High Z	l _{CC2} /Standby	m

Note k: The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. W must be high during all six consecutive cycles. See STORE cycle and RECALL cycle tables and diagrams for further details.

Note I: VO state assumes that $\overline{G} \le V_{IL}$. Activation of nonvolatile cycles does not depend on the state of \overline{G} .

Note m: HSB initiated STORE operation actually occurs only if a WRITE has been done since last STORE operation. After the STORE (if any) completes, the part will go into standby mode inhibiting all operation until HSB rises.

HARDWARE STORE / RECALL

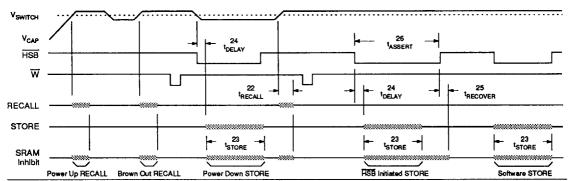
	SYMBO	LS					
NO.			PARAMETER	MIN	MAX	UNITS	NOTES
22	^t RECALL		RECALL Cycle Duration		20	μs	Note o
23	[†] STORE	tнцнн	STORE Cycle Duration		10	ms	V _{CC} ≥ 4.5V
24	^t DELAY	1 _{HLQZ}	HSB Low to Inhibit On	1		με	
25	[†] RECOVER	tHHQX	HSB High to Inhibit Off		300	ns	Note e
26	1 _{ASSERT}	t _{HLHX}	External STORE Pulse Width	250		ns	Note e
Ī	V _{switch}		Low Voltage Trigger Level	4.0	4.5	٧	
	HSB_OL		HSB Output Low Current	3	Ī	mA	HSB = V _{OL} , Note e, n
	IHSB_OH		HSB Output High Current	5	60	μΑ	HSB = V _{IL} , Note e, n

Note e: These parameters guaranteed but not tested.

Note n: HSB is an I/O that has a weak internal pullup; it is basically an open drain output. It is meant to allow up to 32 STK12C68s to be ganged together for simultaneous storing. Do not use HSB to pullup any external circuitry other than other STK12C68 HSB pins.

Note o: A RECALL cycle is initiated automatically at power up when V_{CC} exceeds V_{SWITCH}. 1_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

HARDWARE STORE / RECALL



SOFTWARE STORE/RECALL CYCLE

 $(V_{CC} = 5.0V \pm 10\%)^d$

	SYMBO	LS		:C68-30 STK12		2C68-35 STR		C68-45		
NO.	Std.	Alt	PARAMETER	MIN	MAX	MIN	MAX	MEN	MAX	UNITS
27	†AVAV	t _{RC}	Store/Recall Initiation Cycle Time	30		35		45		ns
28	t _{ELOZ} P		Chip Enable to Output Inactive		85		85		85	ns
29	t _{AVELN}	1 _{AE}	Address Set-up to Chip Enable	0		0]	0		ns
30	1ELEHNP,q	1 _{EP}	Chip Enable Pulse Width	20	ŀ	25		35		ns
31	t _{EHAXN}	1 _{EA}	Chip Disable to Address Change	0		0		0		ns

Note p: Once the software STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.

Note q: Noise on the E pin may trigger multiple read cycles from the same address and abort the address sequence.

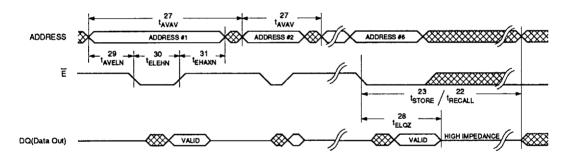
Note r: If the Chip Enable Pulse Width is less than telloy (see READ CYCLE #2) but greater than or equal to teleho, then the data may not be valid at the end of the low pulse, however the STORE or RECALL will still be initiated.

Note s: W must be HIGH when E is LOW during the address sequence in order to initiate a nonvolatile cycle. G may be either HIGH or LOW throughout.

Addresses #1 through #6 are found in the MODE SELECTION table. Address #6 determines whether the STK12C68 performs a STORE or RECALL.

Note t: E must be used to clock in the address sequence for the Software STORE and RECALL cycles.

SOFTWARE STORE/RECALL CYCLE q,r,t



DEVICE OPERATION

The STK12C68 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

STORE cycles may be initiated under user control via a software sequence or HSB assertion and are also automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH}. RECALL operations are automatically initiated upon power-up and whenever the power supply voltage level rises above V_{SWITCH}. RECALL cycles may also be initiated by a software sequence.

SRAM READ

The STK12C68 performs a READ cycle whenever \overline{E} and \overline{G} are LOW and \overline{HSB} and \overline{W} are HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} . If the READ is initiated by \overline{E} or \overline{G} , the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later. The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until \overline{E} or \overline{G} is brought HIGH or \overline{W} or \overline{HSB} is brought LOW.

SRAM WRITE

A write cycle is performed whenever \vec{E} and \vec{W} are LOW and $\vec{H} S \vec{B}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either \vec{E} or \vec{W} go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a \vec{W} controlled WRITE or t_{DVEH} before the end of an \vec{E} controlled WRITE.

It is recommended that \overline{G} be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If \overline{G} is left LOW, internal circuitry will turn off the output buffers t_{WLOZ} after \overline{W} goes LOW.

SOFTWARE STORE

The STK12C68 software STORE cycle is initiated by executing sequential READ cycles from six specific

address locations. By relying on READ cycles only, the STK12C68 implements nonvolatile operation while remaining compatible with standard 8Kx8 SRAMs. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into the nonvolatile elements. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of addresses is used for STORE initiation, it is critical that no other read or write accesses intervene in the sequence or the sequence will be aborted.

To initiate the STORE cycle the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	OAAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate STORE Cycle

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that \overline{G} be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE RECALL

A RECALL cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the STORE initiation. To initiate the RECALL cycle the following sequence of READ operations must be performed:

1.	Read address	0000(hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	OFOE (hex)	Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the

EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AUTOMATIC RECALL

During power up, or after any low power condition ($V_{CAP} < V_{SWITCH}$), when V_{CAP} exceeds the sense voltage of V_{SWITCH} , a *RECALL* cycle will automatically be initiated. After the initiation of this automatic *RECALL*, if V_{CAP} falls below V_{SWITCH} , then another *RECALL* operation will be performed whenever V_{CAP} again rises above V_{SWITCH} .

If the STK12C68 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between W and system V_{CC}.

HARDWARE PROTECT

The STK12C68 offers hardware protection against inadvertent *STORE* operation during low voltage conditions. When $V_{CAP} < V_{SWITCH}$, all externally initiated *STORE* operations will be inhibited.

HSB OPERATION

The Hardware Store Busy pin (HSB) is an open drain circuit acting as both input and output to perform two different functions. When driven low by the internal chip circuitry it indicates that a *STORE* operation (initiated via any means) is in progress within the chip. When driven low by external circuitry for longer than tassert, the chip will conditionally initiate a *STORE* operation after total and tasks.

READ and WRITE operations that are in progress when HSB is driven low (either by internal or external circuitry) will be allowed to complete before the STORE operation is performed, in the following manner. After HSB goes low, the part will continue normal SRAM operations for t_{DELAY}. During t_{DELAY}, a transition on any address or control signal will terminate SRAM operation and cause the STORE to commence. Note that if an SRAM write is attempted after HSB has been forced low, the write will not occur and the STORE operation will begin immediately.

HARDWARE-STORE-BUSY (HSB) is a high speed, low drive capability bi-directional control line. In order to allow a bank of STK12C68s to perform synchronized STORE functions, the HSB pin from a number of chips may be connected together. Each chip contains

a small internal current source to pull $\overline{\text{HSB}}$ HIGH when it is not being driven low. To decrease the sensitivity of this signal to noise generated on the PC board, it may optionally be pulled to V_{CCX} via an external resistor with a value such that the combined load of the resistor and all parallel chip connections does not exceed I_{HSB_OL} at V_{OL} . Do not connect this or any other pull-up to the V_{CAP} node.

If HSB is to be connected to external circuits other than other STK12C68s, an external pull-up resistor should be used.

During any STORE operation, regardless of how it was initiated, the STK12C68 will continue to drive the HSB pin low, releasing it only when the STORE is complete. Upon completion of a STORE operation, the part will be disabled until HSB actually goes HIGH.

AUTOMATIC STORE OPERATION

During normal operation, the STK12C68 will draw current from V_{CCX} to charge up a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH} , the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a STORE operation.

Figure 1 shows the proper connection of capacitors for automatic store operation. The charge storage capacitor should have a capacity of at least $100\mu F$ ($\pm 20\%$) at 6V. Each STK12C68 must have its own $100\mu F$ capacitor. Each STK12C68 must have a high quality, high frequency bypass capacitor of $0.1\mu F$ connected between V_{CAP} and V_{SS} , using leads and traces that are as short as possible.

If the AutoStore[™] function is not required, then V_{CAP} should be tied directly to the power supply and V_{CCX} should be tied to ground. In this mode, *STORE* operations may be triggered through software control or the HSB pin. In either event, V_{CAP} (Pin 1) *must* always have a proper bypass capacitor connected to it.

In order to prevent unneeded STORE operations, automatic STOREs as well as those initiated by externally driving HSB LOW will be ignored unless at least one WRITE operation has taken place since the most recent STORE cycle. Note that if HSB is driven low via external circuitry and no WRITEs have taken place, the part will

still be disabled until $\overline{\text{HSB}}$ is allowed to return HIGH. Software initiated STORE cycles are performed regardless of whether or not a WRITE operation has taken place.

PREVENTING AUTOMATIC STORES

The AutoStoreTM function can be disabled on the fly by holding HSB HIGH with a driver capable of sourcing 15mA at a VOH of at least 2.2V as it will have to overpower the internal pull-down device that drives HSB low for 50ns at the onset of an AutoStoreTM. When the STK12C68 is connected for AutoStoreTM operation (system V_{CC} connected to V_{CCX} and a 100uF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK12C68 will attempt to pull HSB low; if HSB doesn't actually get below V_{IL}, the part will stop trying to pull HSB LOW and abort the AutoStoreTM attempt.

LOW AVERAGE ACTIVE POWER

The STK12C68 has been designed to draw significantly less power when \overline{E} is LOW (chip enabled) but the access cycle time is longer than 55ns. Figure 2 below

shows the relationship between I_{CC} and access times for READ cycles. All remaining inputs are assumed to cycle, and current consumption is given for all inputs at CMOS or TTL levels, over the commercial temperature range. *Figure 3* shows the same relationship for WRITE cycles. When E is HIGH, the chip consumes only standby currents, and these plots do not apply.

The cycle time used in Figure 2 corresponds to the length of time from the later of the last address transition or \overline{E} going LOW to the earlier of \overline{E} going HIGH or the next address transition. \overline{W} is assumed to be HIGH, while the state of \overline{G} does not matter. Additional current is consumed when the address lines change state while \overline{E} is asserted. The cycle time used in Figure 3 corresponds to the length of time from the later of \overline{W} or \overline{E} going LOW to the earlier of \overline{W} or \overline{E} going HIGH.

The overall average current drawn by the part depends on the following items: 1) CMOS or TTL input levels; 2) the time during which the chip is disabled (\overline{E} HIGH); 3) the cycle time for accesses (\overline{E} LOW); 4) the ratio of reads to writes; 5) the operating temperature and; 6) the V_{CC} level.

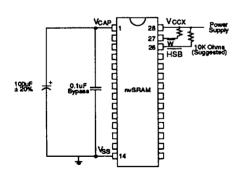


Figure 1. Schematic Diagram

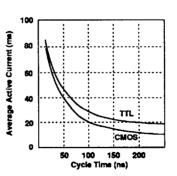


Figure 2. I_{CC} (Max) Reads

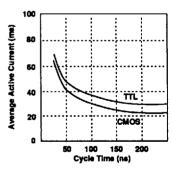


Figure 3. I_{CC} (Max) Writes

Note: Typical at 25° C

ORDERING INFORMATION

