

DATA SHEET

PMBFJ174 to 177 P-channel silicon field-effect transistors

Product specification
File under Discrete Semiconductors, SC07

April 1995

Philips
Semiconductors



PHILIPS

P-channel silicon field-effect transistors

PMBFJ174 to 177

DESCRIPTION

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT23 envelopes. They are intended for application with analogue switches, choppers, commutators etc. using SMD technology. A special feature is the interchangeability of the drain and source connections.

PINNING

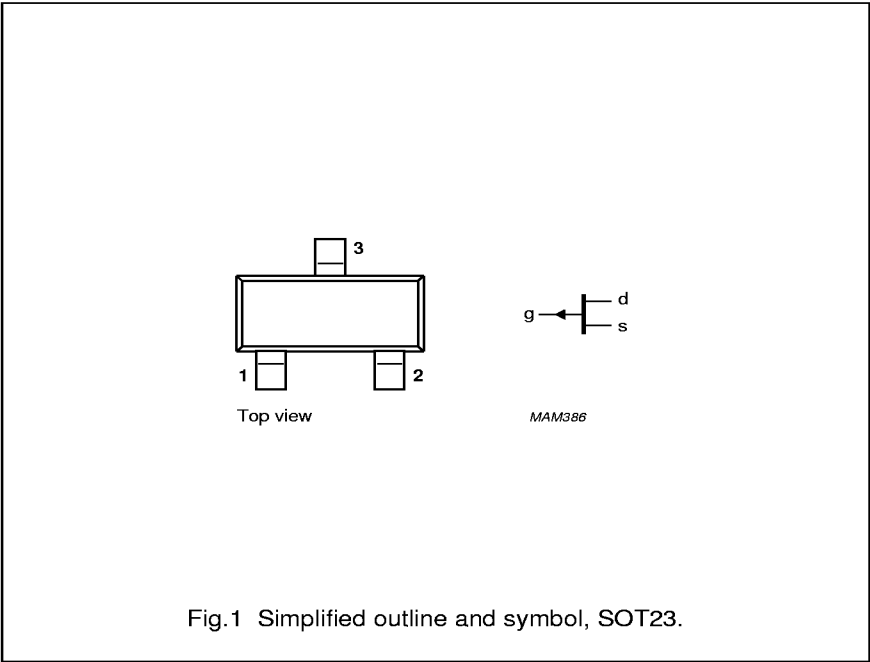
- 1 = drain
- 2 = source
- 3 = gate

Note

- 1. Drain and source are interchangeable.

Marking codes:

- 174 : p6X
- 175 : p6W
- 176 : p6S
- 177 : p6Y



QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate current	$-I_G$	max.	50	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300	mW
Drain current				
$-V_{DS} = 15\text{ V}; V_{GS} = 0$	$-I_{DSS}$	PMBFJ174 > 20 < 135	175 7 70	176 2 35 177 1,5 20 mA
Drain-source ON-resistance	$R_{DS\ on}$	<	85	125
$-V_{DS} = 0,1\text{ V}; V_{GS} = 0$			250	300 Ω

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^{(1)}$	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		-65 to + 150	$^{\circ}\text{C}$
Junction temperature	T_j	max.	150	$^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	430	K/W
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STATIC CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

			PMBFJ174	175	176	177
Gate cut-off current $V_{GS} = 20\text{ V}; V_{DS} = 0$	I_{GSS}	<	1	1	1	1 nA
Drain cut-off current $-V_{DS} = 15\text{ V}; V_{GS} = 10\text{ V}$	$-I_{DSX}$	<	1	1	1	1 nA
Drain current $-V_{DS} = 15\text{ V}; V_{GS} = 0$	$-I_{DSS}$	> <	20 135	7 70	2 35	1,5 20 mA
Gate-source breakdown voltage $I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$V_{(BR)GSS}$	>	30	30	30	30 V
Gate-source cut-off voltage $-I_D = 10\text{ nA}; V_{DS} = -15\text{ V}$	$V_{GS\ off}$	> <	5 10	3 6	1 4	0,8 2,25 V
Drain-source ON-resistance $-V_{DS} = 0,1\text{ V}; V_{GS} = 0$	$R_{DS\ on}$	<	85	125	250	300 Ω

Note

1. Mounted on a ceramic substrate of 8 mm × 10 mm × 0,7 mm.

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DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz

$V_{GS} = 10\text{ V}; V_{DS} = 0\text{ V}$

$V_{GS} = V_{DS} = 0$

Feedback capacitance, f = 1 MHz

$V_{GS} = 10\text{ V}; V_{DS} = 0\text{ V}$

Switching times (see Fig.2 + 3)

Delay time

Rise time

Turn-on time

Storage temperature

Fall time

Turn-off time

Test conditions:

C _{is}	typ.	8			pF
C _{is}	typ.	30			pF
C _{rs}	typ.	4			pF
	PMBFJ174	175	176	177	
t _d	typ.	2	5	15	20 ns
t _r	typ.	5	10	20	25 ns
t _{on}	typ.	7	15	35	45 ns
t _s	typ.	5	10	15	20 ns
t _f	typ.	10	20	20	25 ns
t _{off}	typ.	15	30	35	45 ns
-V _{DD}		10	6	6	6 V
V _{GS off}		12	8	6	3 V
R _L		560	1200	2000	2900 Ω
V _{GS on}		0	0	0	0 V

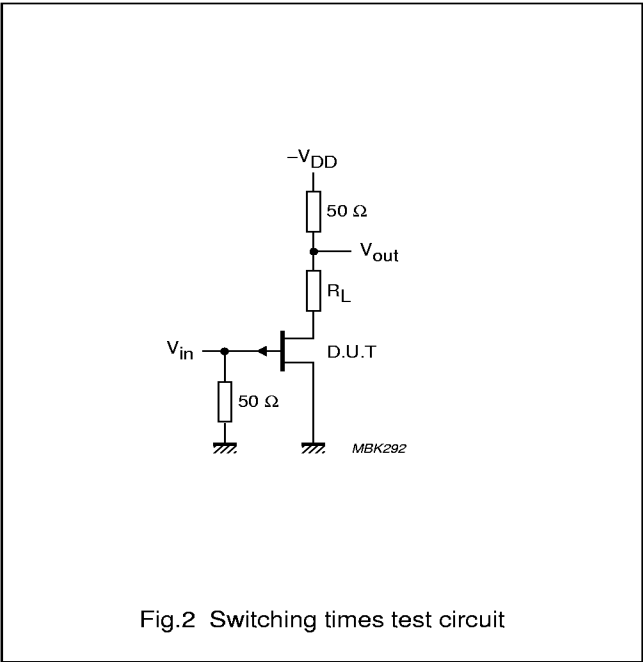
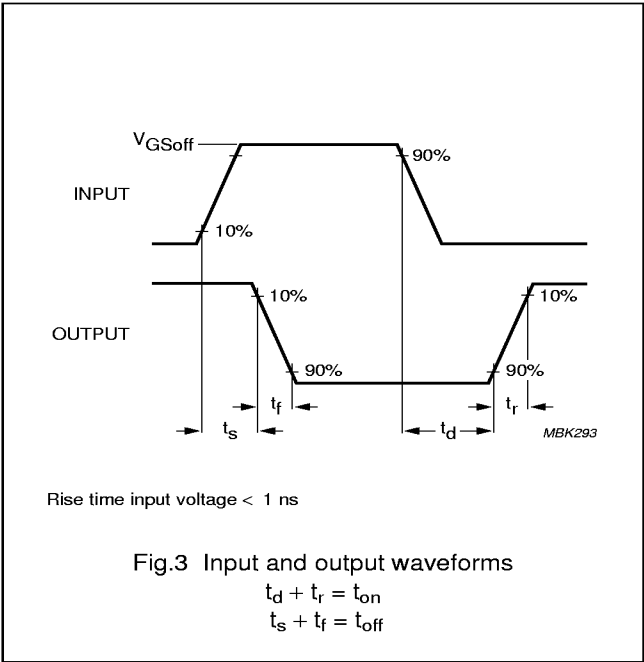


Fig.2 Switching times test circuit



Rise time input voltage < 1 ns

Fig.3 Input and output waveforms
 $t_d + t_r = t_{on}$
 $t_s + t_f = t_{off}$

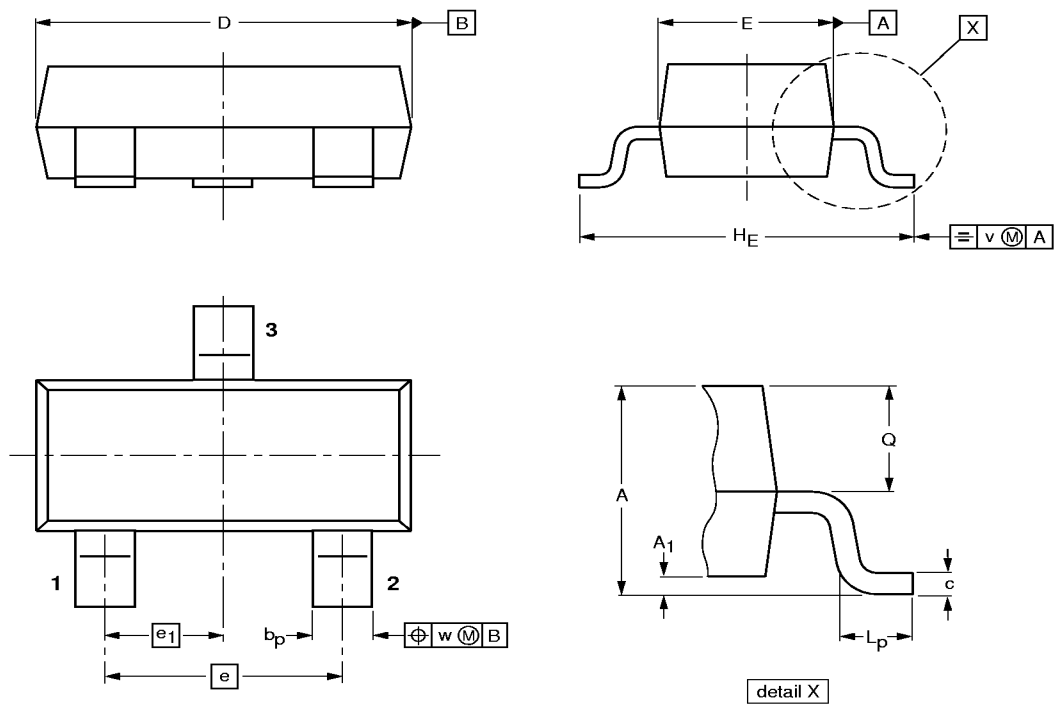
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PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28