IBM014400 IBM014400M
IBM014400B IBM014400P

1M x 4 10/10 DRAM

Features

- 1,048,576 word by 4 bit organization
- Power Supply: 3.3 ± 0.3V or 5.0 ± 0.5V
- Standard Power (SP) and Low Power (LP)
- 1024 Refresh Cycles
  - 16 ms Refresh Rate (SP version)
  - 128 ms Refresh Rate (LP version)
- High Performance:

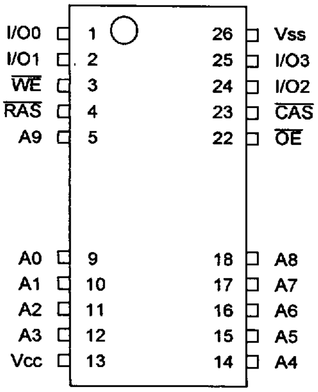
		-60	-70
t_{RAC}	$\overline{\text{RAS}}$ Access Time	60ns	70ns
t_{CAC}	$\overline{\text{CAS}}$ Access Time	15ns	18ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	40ns

- Power Dissipation
  - Active (max)
    - 85 mA / 70 mA (5.0V)
    - 95 mA / 80 mA (3.3V)
  - Standby Current: TTL Inputs (max)
    - 2.0 mA (SP version)
    - 1.0 mA (LP version)
  - Standby Current: CMOS Inputs (max)
    - 1.0 mA (SP version)
    - 0.15 mA (LP version)
- Fast Page Mode
- $\overline{\text{RAS}}$ Only, and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- Self-Refresh (LP version only)
- Packages: SOJ-26/20 (300mil)
  TSOP-26/20 (300mil)

Description

The IBM014400 is a fast-page dynamic RAM organized 1,048,576 words by 4 bits. The devices are fabricated in IBM's 4M-bit Shrink 2 CMOS silicon gate technology. The circuits and process have been designed to provide high performance, low power dissipation, and high reliability. The devices operate with either a 5.0V ± 0.5V or 3.3V ± 0.3V power supply and are offered in a plastic 26/20 pin SOJ (300mil) or TSOP (300mil) package. Refreshing may be accomplished by means of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{\text{RAS}}$ - only refresh cycles can also refresh all memory locations. Self-Refresh mode is entered by holding $\overline{\text{RAS}}$ low for $\geq 100\mu S$ during a CBR cycle. Detection of this long $\overline{\text{RAS}}$ time during a CBR cycle starts an internal oscillator that maintains data integrity without external clocking. Self-Refresh mode is included as a standard feature for Low Power devices (IBM014400M and IBM014400P). Self Refresh operating current is $\leq 170\mu A$ (max) and typically $\leq 100\mu A$. All low power devices support Extended Data Retention of 128ms, eight times (8x) the retention supported by IBM's standard power devices.

Pin Assignments



Pin Description

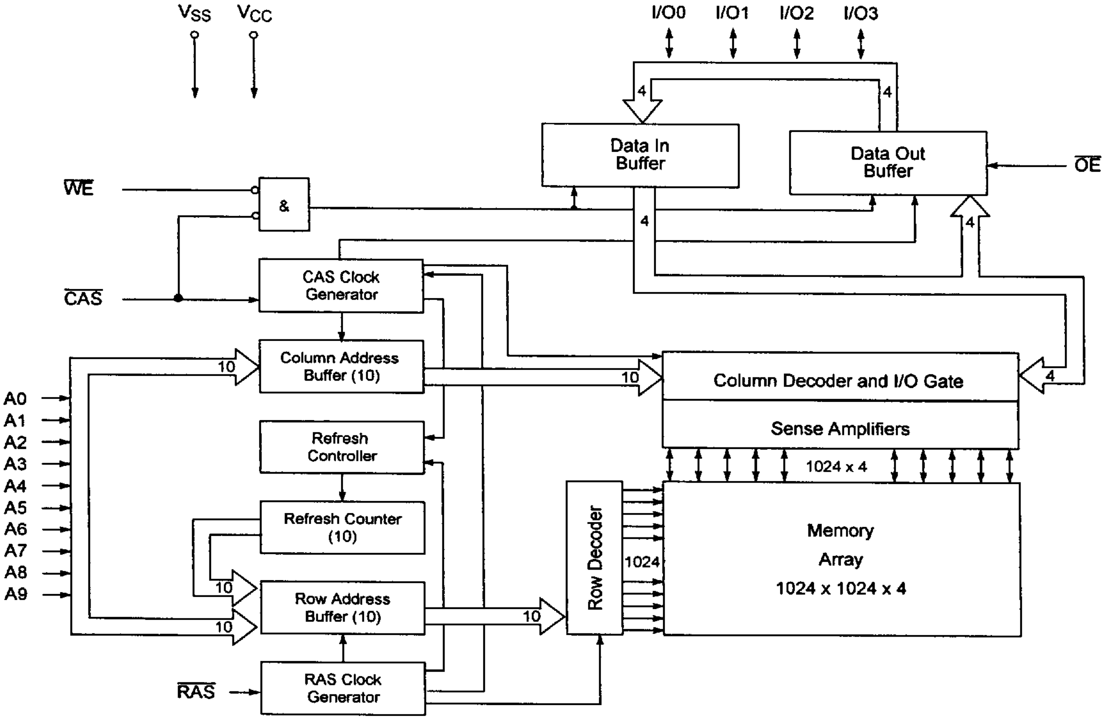
A0 - A9	Address Input
I/O0 - I/O3	Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
$\overline{\text{OE}}$	Output Enable
V_{CC}	Power (5.0V or 3.3V)
V_{SS}	Ground

Ordering Information

Part Number	SP / LP	Self Refresh	Power Supply	Speed	Package	Notes
IBM014400J1 -60	SP	No	5.0V	60ns	300mil SOJ 26/20	1
IBM014400J1 -70	SP	No	5.0V	70ns	300mil SOJ 26/20	1
IBM014400BJ1 -60	SP	No	3.3V	60ns	300mil SOJ 26/20	1
IBM014400BJ1 -70	SP	No	3.3V	70ns	300mil SOJ 26/20	1
IBM014400MJ1 -60	LP	Yes	5.0V	60ns	300mil SOJ 26/20	1
IBM014400MJ1 -70	LP	Yes	5.0V	70ns	300mil SOJ 26/20	1
IBM014400PJ1 -60	LP	Yes	3.3V	60ns	300mil SOJ 26/20	1
IBM014400PJ1 -70	LP	Yes	3.3V	70ns	300mil SOJ 26/20	1
IBM014400MT1 -60	LP	Yes	5.0V	60ns	300mil TSOP 26/20	1
IBM014400MT1 -70	LP	Yes	5.0V	70ns	300mil TSOP 26/20	1
IBM014400PT1 -60	LP	Yes	3.3V	60ns	300mil TSOP 26/20	1
IBM014400PT1 -70	LP	Yes	3.3V	70ns	300mil TSOP 26/20	1

1. SP = Standard Power version (IBM014400 and IBM014400B); LP = Low Power version (IBM014400M and IBM014400P)

Block Diagram



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Col. Address	I/O0 - I/O3
Standby		H	H→X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col.	Data Out
Early-Write		L	L	L	X	Row	Col.	Data In
Delayed-Write		L	L	H→L	H	Row	Col.	Data In
Read-Modify-Write		L	L	H→L	L→H	Row	Col.	Data Out, Data In
Fast Page Mode Read	1st Cycle	L	H→L	H	L	Row	Col.	Data Out
	2nd Cycle	L	H→L	H	L	N/A	Col.	Data Out
Fast Page Mode Write	1st Cycle	L	H→L	L	X	Row	Col.	Data In
	2nd Cycle	L	H→L	L	X	N/A	Col.	Data In
Fast Page Mode Read-Modify-Write	1st Cycle	L	H→L	H→L	L→H	Row	Col.	Data Out, Data In
	2nd Cycle	L	H→L	H→L	L→H	N/A	Col.	Data Out, Data In
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	N/A	High Impedance
Hidden Refresh Read		L→H→L	L	H	L	Row	Col.	Data Out
Self Refresh (LP version only)		H→L	L	L	H	X	X	X

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt Device	5.0 Volt Device		
V_{CC}	Power Supply Voltage	-0.5 to +4.1	-1.0 to +6.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC}+0.5, 4.1)	-0.5 to min (V_{CC}+0.5, 6.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC}+0.5, 4.1)	-0.5 to min (V_{CC}+0.5, 6.0)	V	1
T_A	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	1.0	1.0	W	1
I_{OUT}	Short Circuit Output Current	20	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Symbol	Parameter	5.0 Volt Devices			3.3 Volt Devices			Units	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	2.0	—	V_{CC} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS}=0V.

Capacitance (T_A=25°C, f=1MHz)

Symbol	Parameter	Min.	Max	Units	Notes
C_{I1}	Input Capacitance (Addresses)	—	5	pF	1
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	—	7	pF	1
C_o	Output Capacitance (I/O's)	—	7	pF	1

1. Input capacitance measurements made with rise time shift method with $\overline{CAS}$ = V_{IH} to disable output.

DC Electrical Characteristics (T_A= 0 to +70 C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter		3.3 Volt Device		5.0 Volt Device		Units	Notes
			Min.	Max.	Min.	Max.		
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling: t_{RC} = t_{RC} min.)	-60	—	95	—	85	mA	1,2,3,4
		-70	—	80	—	70		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ ≥ V_{IH} min)	SP version	—	2.0	—	2.0	mA	4
		LP version	—	1.0	—	1.0		
I_{CC3}	$\overline{\text{RAS}}$ Only Refresh Current Average Power Supply Current, $\overline{\text{RAS}}$ Only Mode ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}}$ ≥ V_{IH} min: t_{RC} = t_{RC} min)	-60	—	95	—	85	mA	1,3,4
		-70	—	80	—	70		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{\text{RAS}}$ ≤ V_{IL} min, $\overline{\text{CAS}}$ Cycling, t_{PC} = t_{PC} min)	-60	—	65	—	60	mA	1,2,3,4
		-70	—	65	—	60		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ ≥ V_{IH})	SP version	—	1	—	1	mA	7,8
		LP version	—	0.15	—	0.15		
I_{CC6}	$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Current Average Power Supply Current, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Mode (RAS Cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, t_{RC} = t_{RC} min)	-60	—	95	—	85	mA	1,3,4,5
		-70	—	80	—	70		
I_{CC7}	Self Refresh Current, LP version only Average Power Supply Current during Self Refresh (CBR cycle with $\overline{\text{RAS}}$ ≥ t_{RASS} (min))		—	170	—	170	µA	7,8
I_{CC8}	Battery Backup Refresh Current, LP version only Average Power Supply Current during Battery Backup refresh ($\overline{\text{CAS}}$ ≤V_{IL}, $\overline{\text{WE}}$ ≥V_{IH}, t_{RAS} ≤ 1µSec, t_{RC}=125µSec)		—	300	—	300	µA	7,8,9
I_{CC9}	Standby Current Standby current with Output's enabled ($\overline{\text{RAS}}$ ≥ V_{IH} (min) and $\overline{\text{CAS}}$ ≤ V_{IL} (max))		—	5	—	5	mA	4,6
$I_{I(L)}$	Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 1.0V)) for 5.0V, or (0.0 ≤ V_{IN} ≤ (V_{CC} + 0.3V)) for 3.3V. All Other Pins Not Under Test = 0V		-10	+10	-10	+10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC} max)		-10	+10	-10	+10	µA	
V_{OH}	Output Level (TTL) Output "H" Level Voltage (I_{OUT} = -5mA for 5.0V, or I_{OUT} = -2mA for 3.3V)		2.4	V_{CC}	2.4	V_{CC}	V	
V_{OL}	Output Level (TTL) Output "L" Level Voltage (I_{OUT} = +4.2mA for 5.0V, or I_{OUT} = +2mA for 3.3V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Column address can be changed once or less while $\overline{\text{RAS}}$ =V_{IL} and $\overline{\text{CAS}}$ =V_{IH}.
4. All I/O and other input pins must be ≤ V_{IL}(max) or ≥V_{IH}(min).
5. Enables on-chip refresh and address counters.
6. Assumes no resistive loads on I/O pins.
7. ((V_{CC}-0.2V ≤ V_{IH} ≤ V_{CC}+0.5V) and (0.0V ≤ V_{IL} ≤ 0.2V)) for 5.0V, or
   ((V_{CC}-0.2V ≤ V_{IH} ≤ V_{CC}+0.3V) and (0.0V ≤ V_{IL} ≤ 0.2V)) for 3.3V.
8. All other I/O and other inputs at V_{IH} or V_{IL}.
9. 1024 rows at 128µs = 128ms.

AC Characteristics (T_A=0 to +70°C)

1. An initial pause of 100μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles or 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. If $\overline{OE}$ is tied permanently low, Late-Write or Read-Modify-Write operations are not possible.
6. If $\overline{CAS}$ ≥ V_{IH}(min), data outputs are in high impedance.

Read, Write, Read-Modify-Write and Ref. Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	100K	18	100K	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	52	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	30	15	35	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	18	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	15	—	20	—	ns	5
t_{DZO}	$\overline{OE}$ Delay Time From D_{IN}	0	—	0	—	ns	6
t_{DZC}	$\overline{CAS}$ Delay Time From D_{IN}	0	—	0	—	ns	6
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	1,2,7

1. AC measurements assume t_T=5ns.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
3. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
4. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
5. Either t_{CDD} or t_{ODD} must be satisfied.
6. Either t_{DZC} or t_{DZO} must be satisfied.
7. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1,3,4
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	3
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	3
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	18	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	18	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	2
t_{DH}	D_{IN} Hold Time	12	—	15	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. t_{RWD}, t_{CWD}, and t_{AWD} apply to Read-Modify-Write cycles. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an Early Write cycle and the data I/O pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), and $t_{AWD} \geq t_{AWD}$(min), the cycle is a Read-Modify-Write cycle and the data I/O pins will contain read data from the selected cells. If neither of the above sets of conditions are satisfied, the condition of the data I/O pins (at access time) is indeterminate.
2. These parameters are referenced to the falling edge of $\overline{CAS}$ for Early-Write cycles and to the falling edge of $\overline{WE}$ for Delayed-Write or Read-Modify-Write cycles.
3. Parameter t_{WP} is applicable for a Delayed-Write cycle such as a Read-Write or Read-Modify-Write cycle. For Early-Write cycles, both t_{WCS} and t_{WCH} must be met.
4. The I/O pins go into high impedance during Read cycles once t_{OEZ} of t_{OFF} occurs. If $\overline{CAS}$ goes high first, $\overline{OE}$ becomes a "don't care". If $\overline{OE}$ goes high and $\overline{CAS}$ stays low, $\overline{OE}$ is not a "don't care", and the I/Os will provide the previously read data if $\overline{OE}$ is taken back low (while $\overline{CAS}$ remains low).

Read-Modify-Write-Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RWC}	Read-Modify-Write Cycle Time	145	—	175	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	—	90	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	—	40	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	—	55	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	15	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. t_{RWD}, t_{CWD}, and t_{AWD} apply to Read-Modify-Write cycles. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an Early Write cycle and the data I/O pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), and $t_{AWD} \geq t_{AWD}$(min), the cycle is a Read-Modify-Write cycle and the data I/O pins will contain read data from the selected cells. If neither of the above sets of conditions are satisfied, the condition of the data I/O pins (at access time) is indeterminate.
2. These parameters are referenced to the falling edge of $\overline{CAS}$ for Early-Write cycles and to the falling edge of $\overline{WE}$ for Late-Write and Read-Modify-Write cycles must have both t_{OEZ} and t_{OEH} satisfied ($\overline{OE}$ high during Write cycle) in order to insure that the output buffers will be in high impedance during the Write cycle. The data I/O pins will remain in high impedance until the next valid Read cycle.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RAC}	Access Time from $\overline{\text{RAS}}$	—	60	—	70	ns	1,4
t_{CAC}	Access Time from $\overline{\text{CAS}}$	—	15	—	18	ns	2,4,7
t_{AA}	Access Time from Address	—	30	—	35	ns	4,7,8
t_{OEA}	Access Time From $\overline{\text{OE}}$	—	15	—	18	ns	4,9
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	—	0	—	ns	5
t_{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	0	—	0	—	ns	5
t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z	0	—	0	—	ns	4
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{OHO}	Output Data Hold From $\overline{\text{OE}}$	0	—	0	—	ns	
t_{OFF}	Output Buffer Turn-Off Delay From $\overline{\text{CAS}}$	0	15	0	15	ns	6
t_{OEZ}	Output Buffer Turn-Off Delay From $\overline{\text{OE}}$	0	15	0	15	ns	6
t_{OES}	$\overline{\text{OE}}$ Setup Time prior to $\overline{\text{RAS}}$	0	—	0	—	ns	
t_{CDD}	$\overline{\text{CAS}}$ to D_{IN} Delay Time	15	—	20	—	ns	3

1. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, then t_{RAC} will exceed the value shown.
2. Assumes that $t_{RCD} \geq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max).
3. Either t_{CDD} or t_{ODD} must be satisfied.
4. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
5. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
6. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
7. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
8. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \geq t_{RAD}$(max).
9. If $\overline{\text{OE}}$ is tied permanently low, Late-Write or Read-Modify-Write operations are not possible.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	85	—	90	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{PC}	Fast Page Mode Cycle Time	40	—	40	—	ns	
t_{RASP}	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	60	100K	70	100K	ns	2
t_{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge	—	35	—	40	ns	1
t_{CPRH}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	35	—	40	—	ns	

1. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
2. t_{RASP} defines t_{RAS} in fast page mode cycles.

Refresh Cycle

Symbol	Parameter		-60		-70		Units	Notes
			Min.	Max.	Min.	Max.		
t_{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)		5	—	5	—	ns	1
t_{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)		10	—	10	—	ns	1
t_{WRP}	$\overline{\text{WE}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)		10	—	10	—	ns	
t_{WRH}	$\overline{\text{WE}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)		10	—	10	—	ns	
t_{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time		0	—	0	—	ns	
t_{REF}	Refresh period	SP version	—	16	—	16	ms	2
		LP version	—	128	—	128		

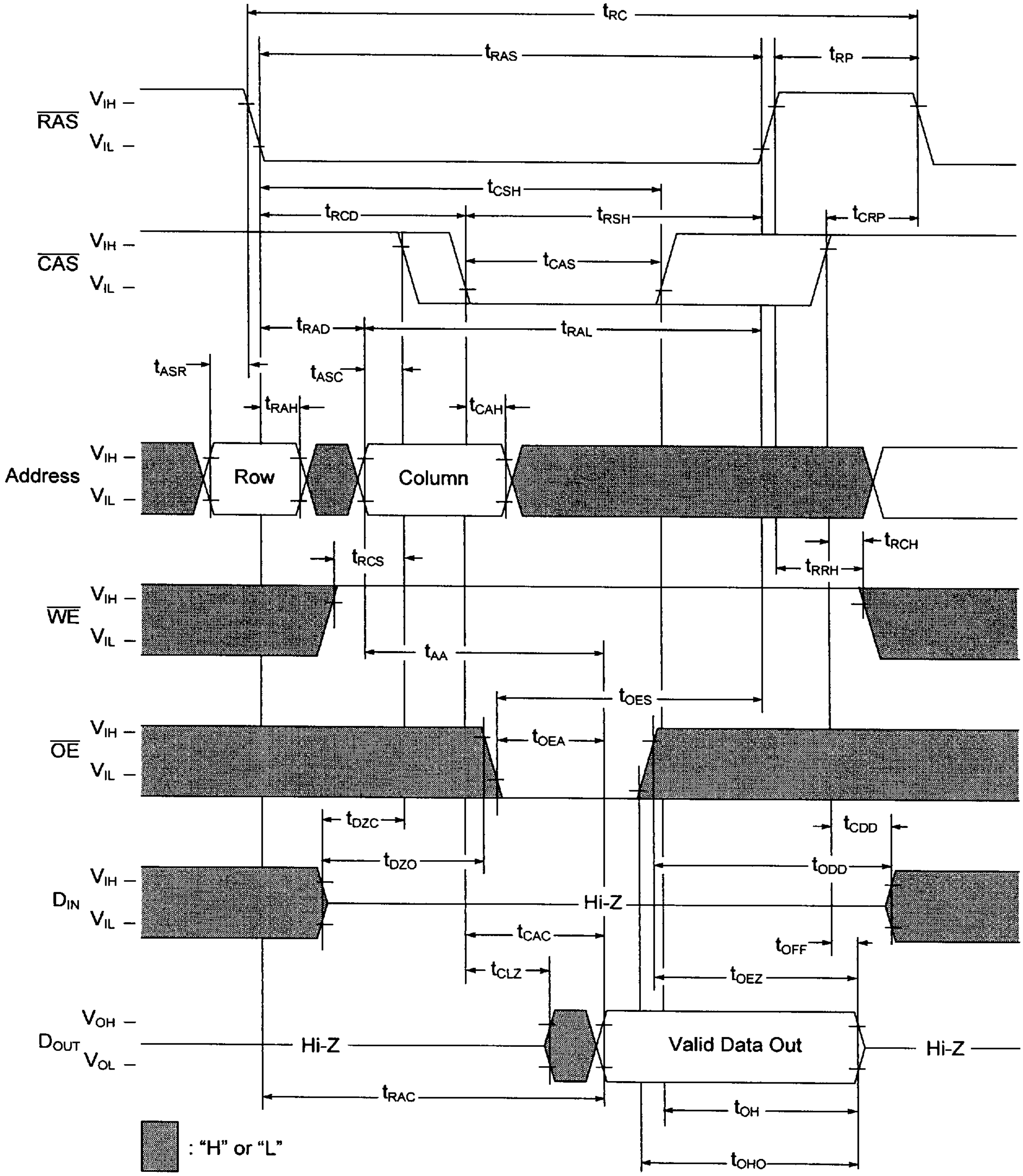
1. Enables on-chip refresh and address counters.
2. 1024 cycles.

Self Refresh Cycle - Low Power version only

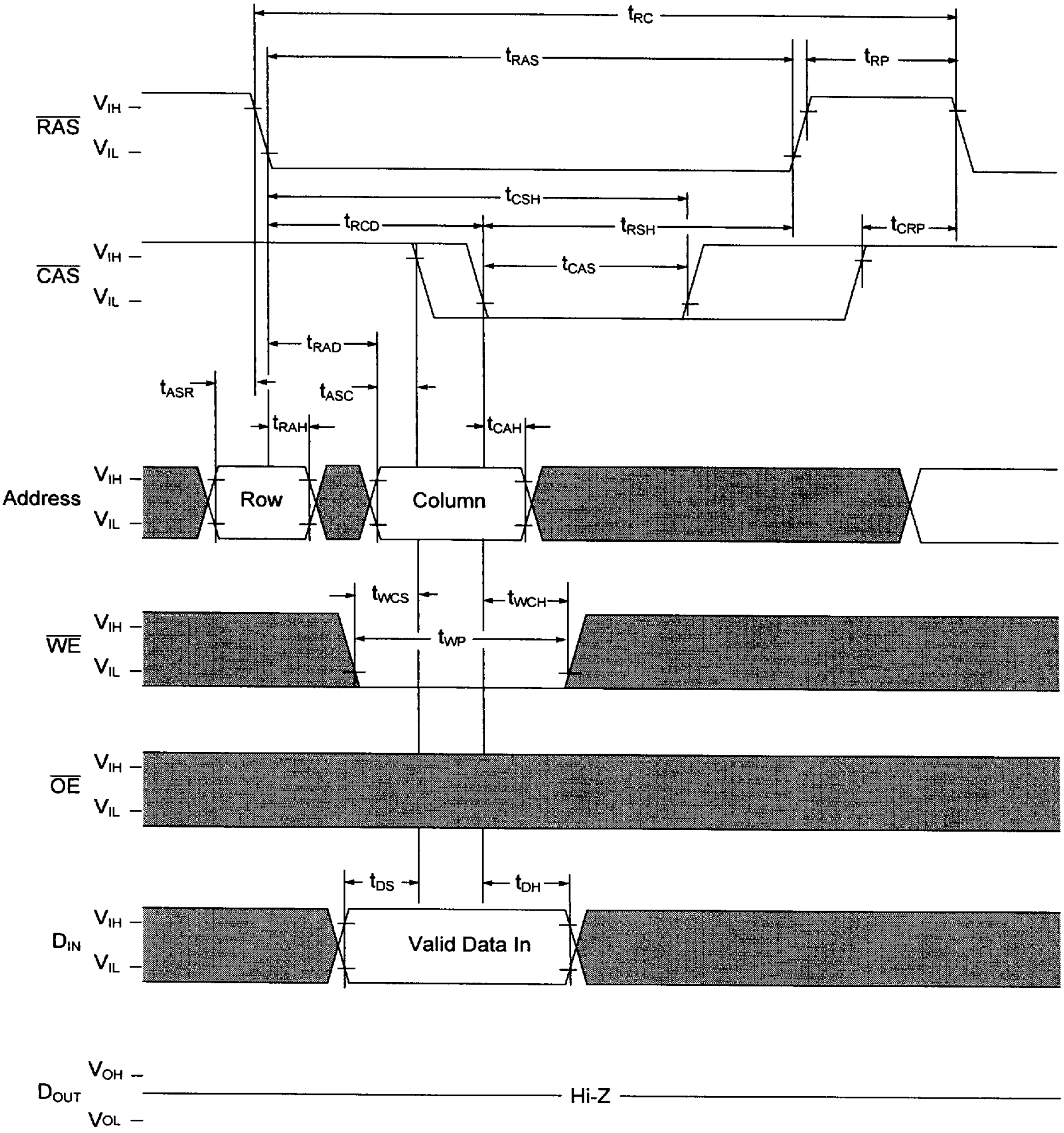
Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RASS}	$\overline{\text{RAS}}$ Pulse Width (Self Refresh)	100	—	100	—	µs	1,2
t_{RPS}	$\overline{\text{RAS}}$ Precharge Time During Self Refresh Cycle	110	—	130	—	ns	1
t_{CHD}	$\overline{\text{CAS}}$ Hold Time During Self Refresh Cycle	10	—	10	—	ns	1

1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in a EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in a ROR manner over the refresh interval, then a full burst of all row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh. If row addresses are being refreshed in a CBR-Burst manner over the refresh interval (i.e. burst of 8), then upon exiting from Self Refresh the user must conform to whatever refresh (i.e. burst of 8) method that was being used prior to entering Self Refresh.
2. I/O pins will go into high impedance after 100µs.

Read Cycle

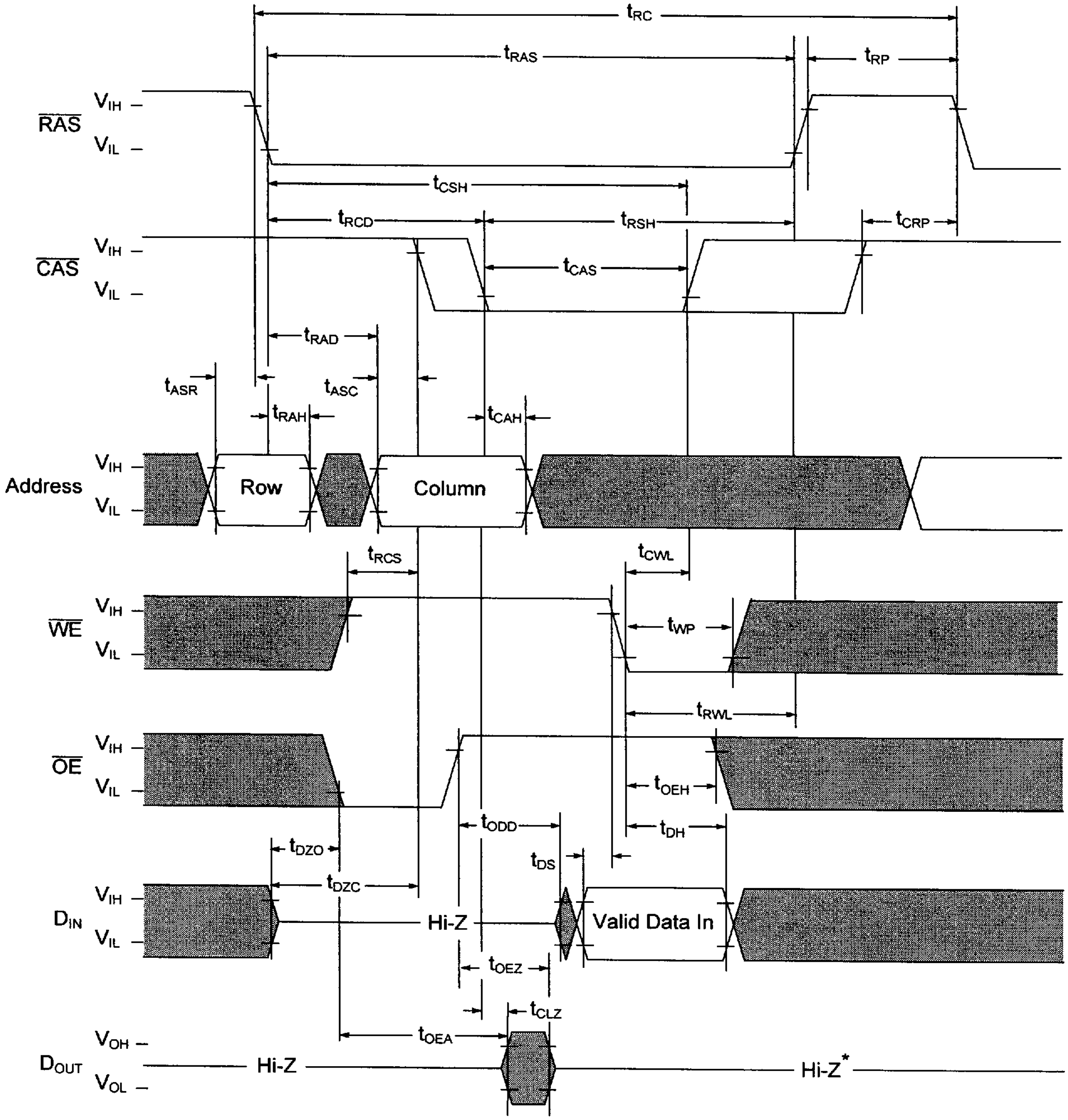

t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{RCD}
t_{RSH}
t_{CRP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{CAS}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
Address
V_{IH}
V_{IL}
Row
Column
t_{RCS}
t_{RCH}
t_{RRH}
$\overline{WE}$
V_{IH}
V_{IL}
t_{AA}
t_{OES}
$\overline{OE}$
V_{IH}
V_{IL}
t_{OEA}
t_{DZC}
t_{CDD}
t_{DZO}
t_{ODD}
D_{IN}
V_{IH}
V_{IL}
Hi-Z
t_{CAC}
t_{OFF}
t_{CLZ}
t_{OEZ}
D_{OUT}
V_{OH}
V_{OL}
Hi-Z
Valid Data Out
Hi-Z
t_{RAC}
t_{OH}
t_{OHO}
▨ : "H" or "L"

Write Cycle (Early Write)



▨ : "H" or "L"

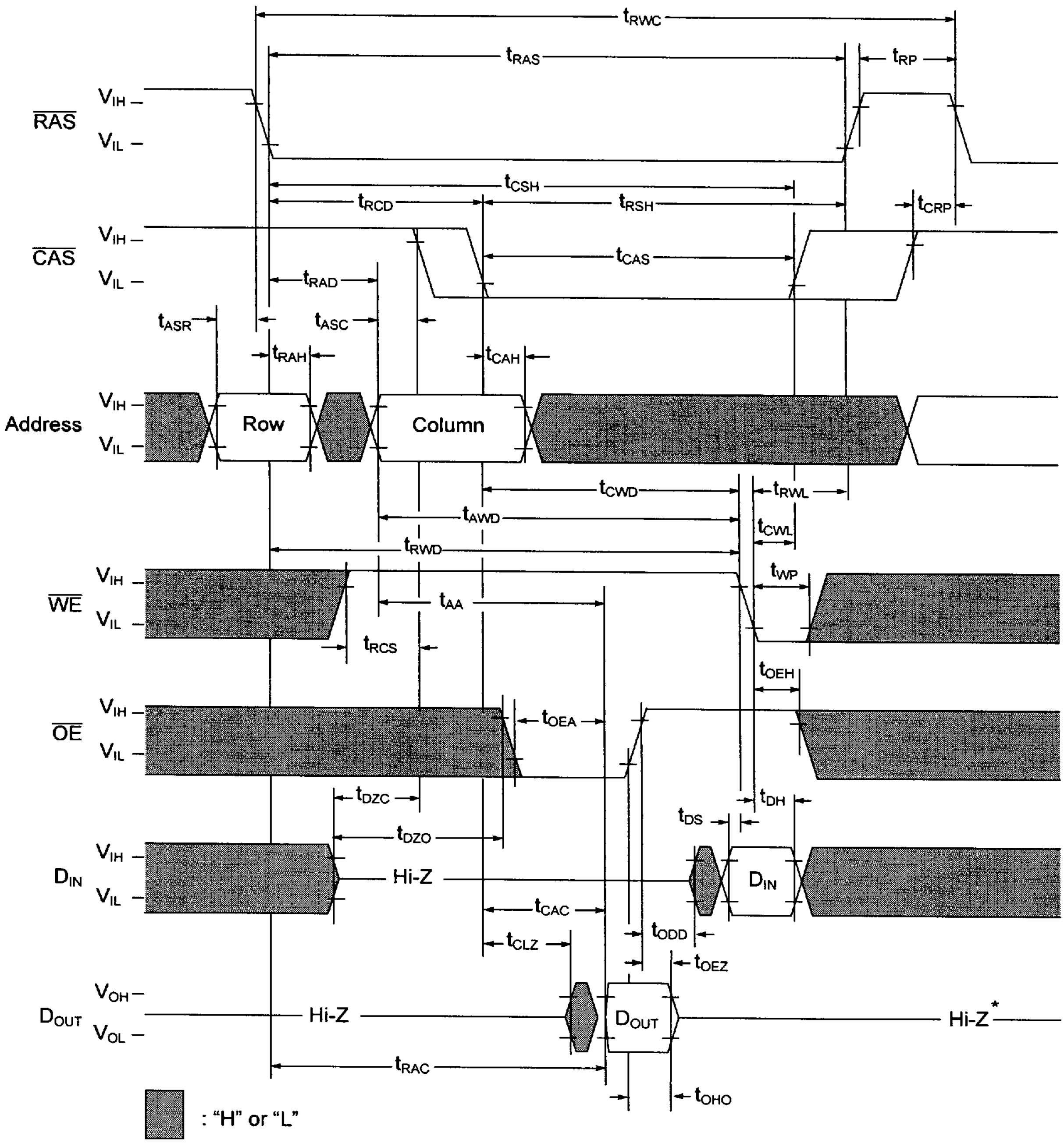
Write Cycle (Delayed Write)



▨ : "H" or "L"

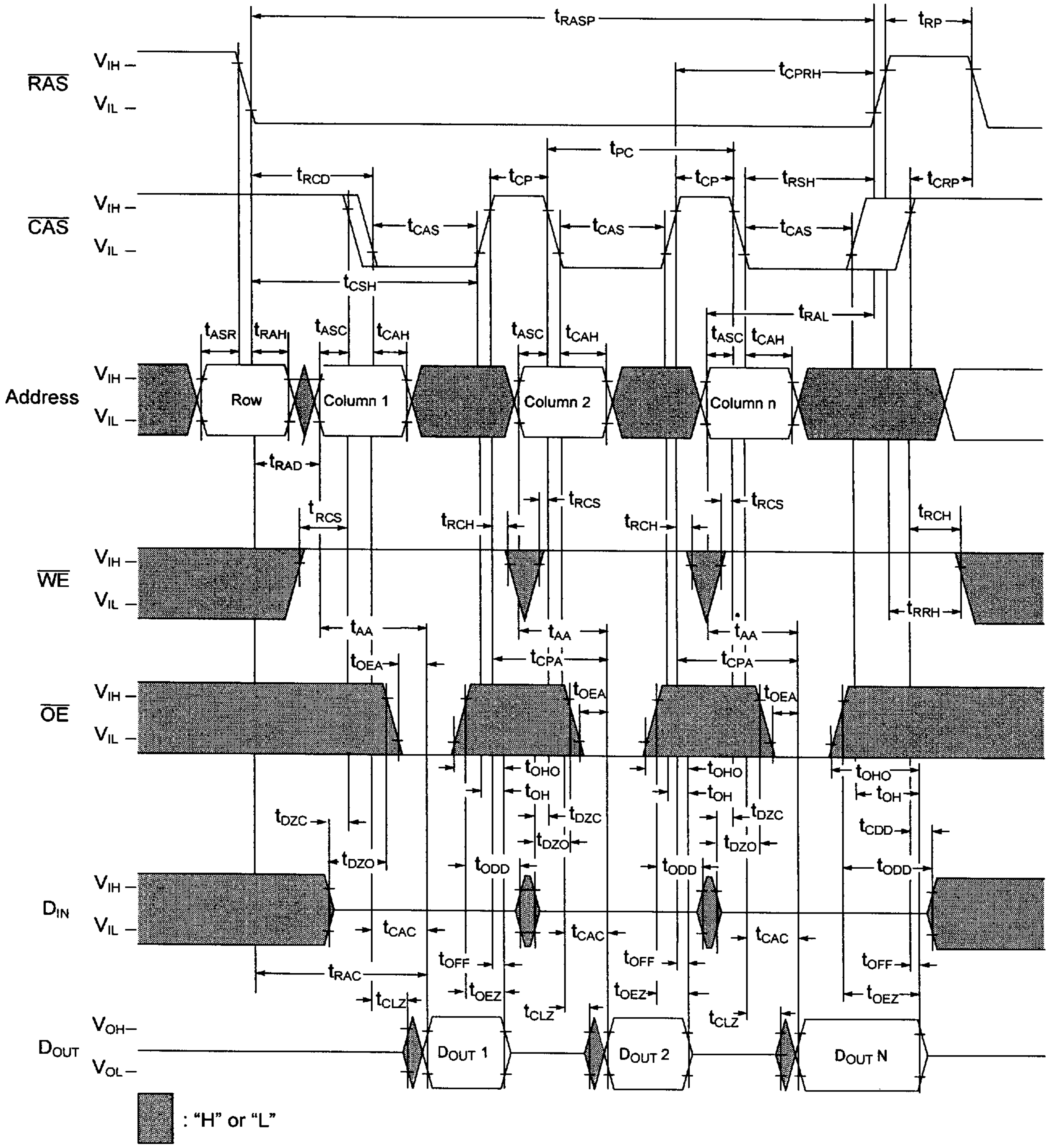
*Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

Read-Modify-Write Cycle

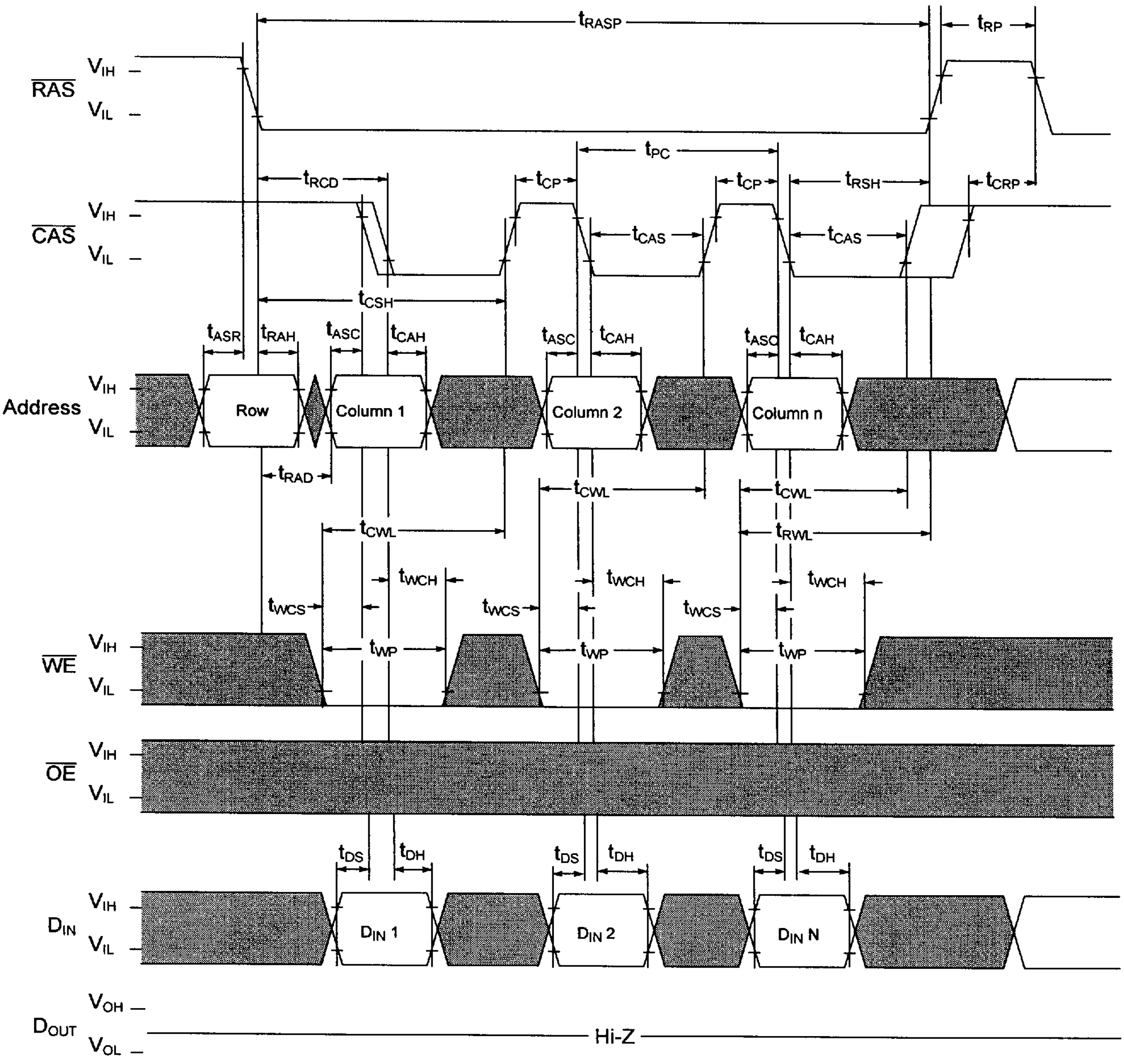


*Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

Fast Page Mode Read Cycle

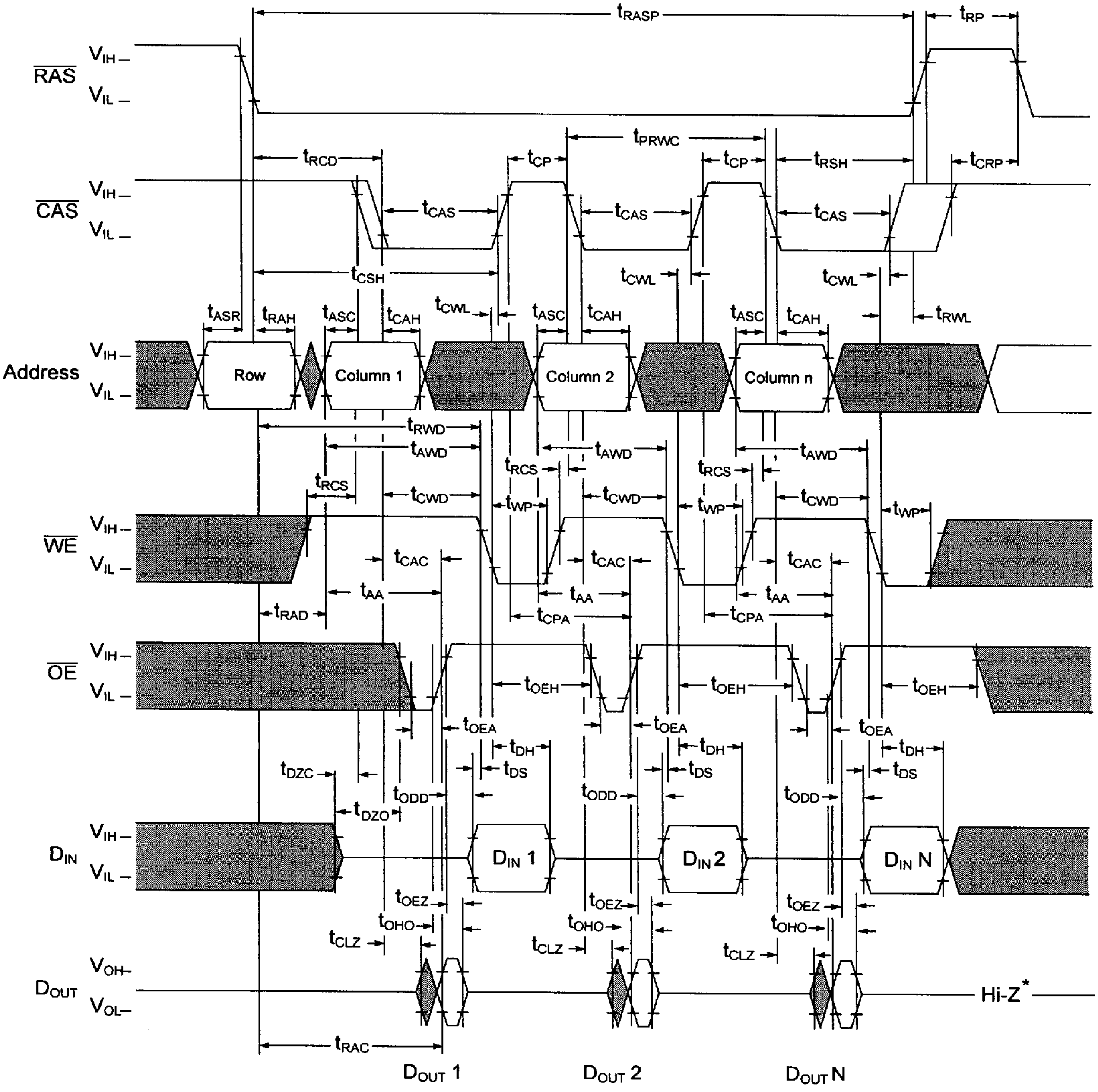


Fast Page Mode Write Cycle



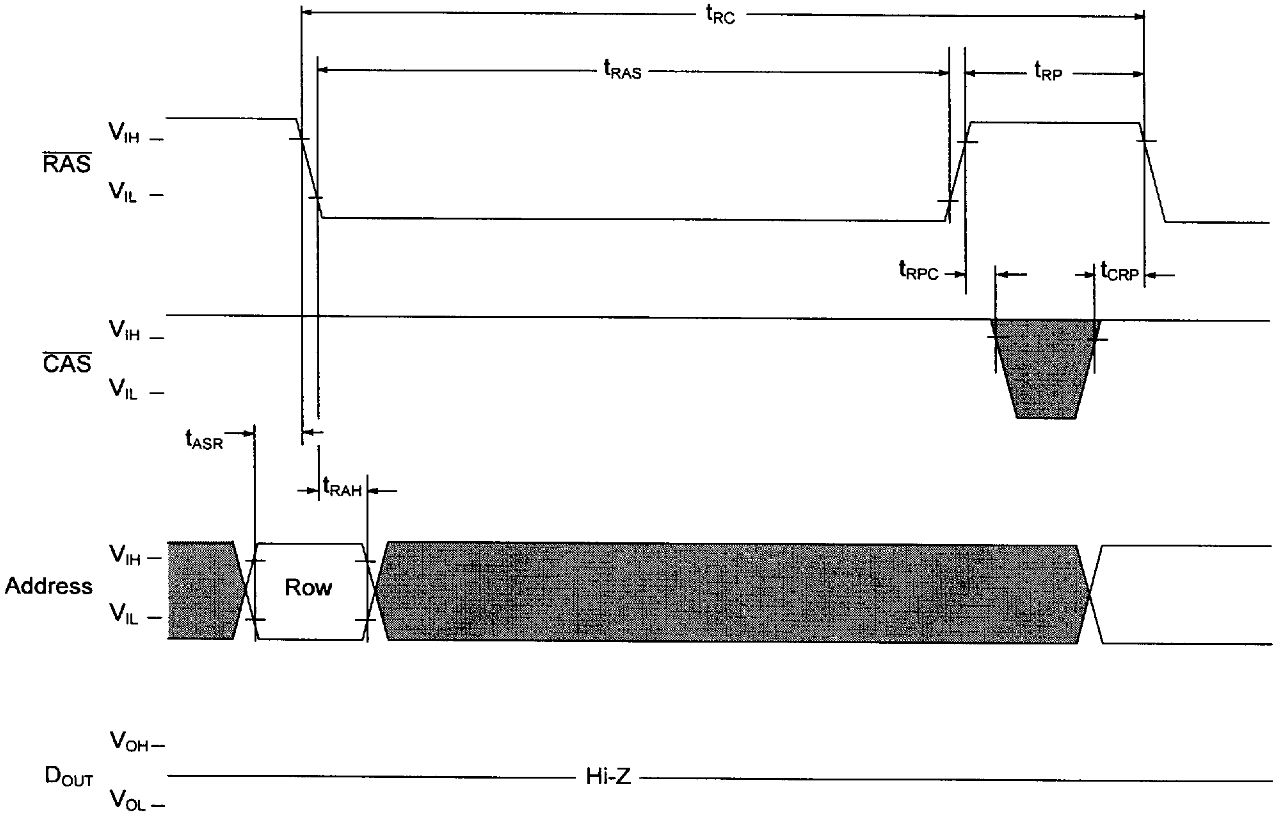
▨ : “H” or “L”

Fast Page Mode Read-Modify-Write Cycle



▨ : “H” or “L”

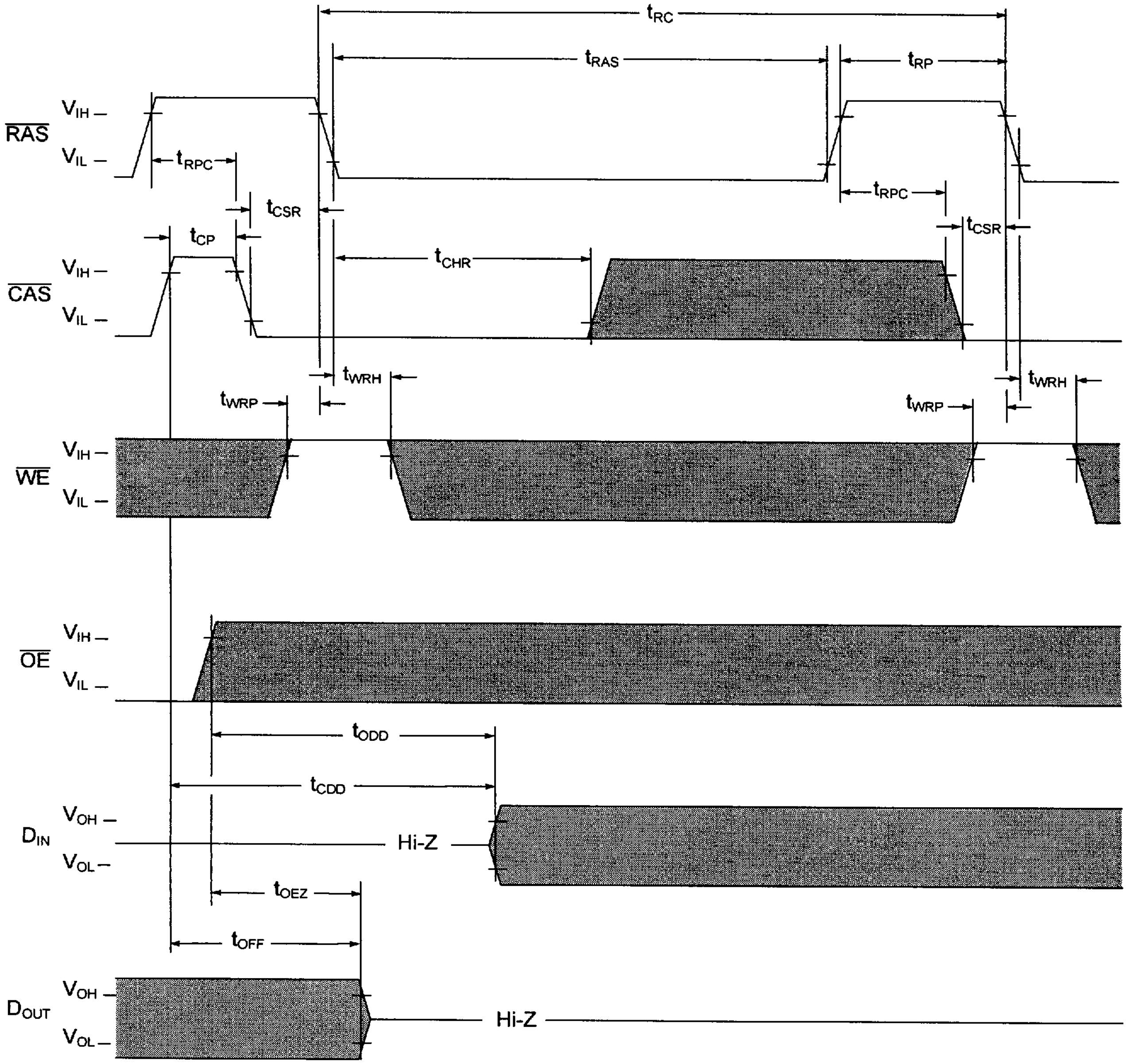
$\overline{\text{RAS}}$ Only Refresh Cycle



▨ : “H” or “L”

NOTE: $\overline{\text{WE}}$, $\overline{\text{OE}}$ and D_{IN} are “H” or “L”

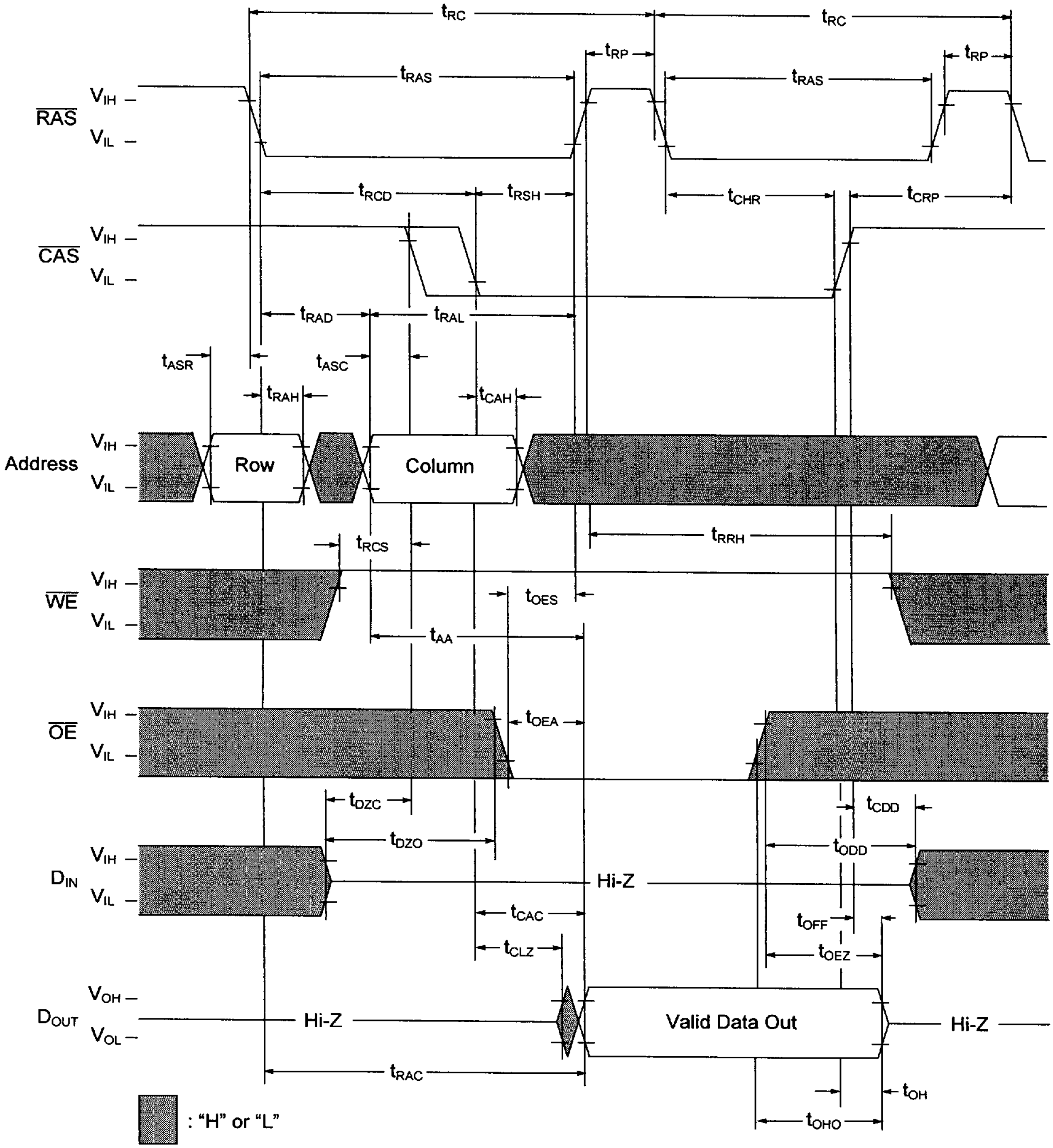
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



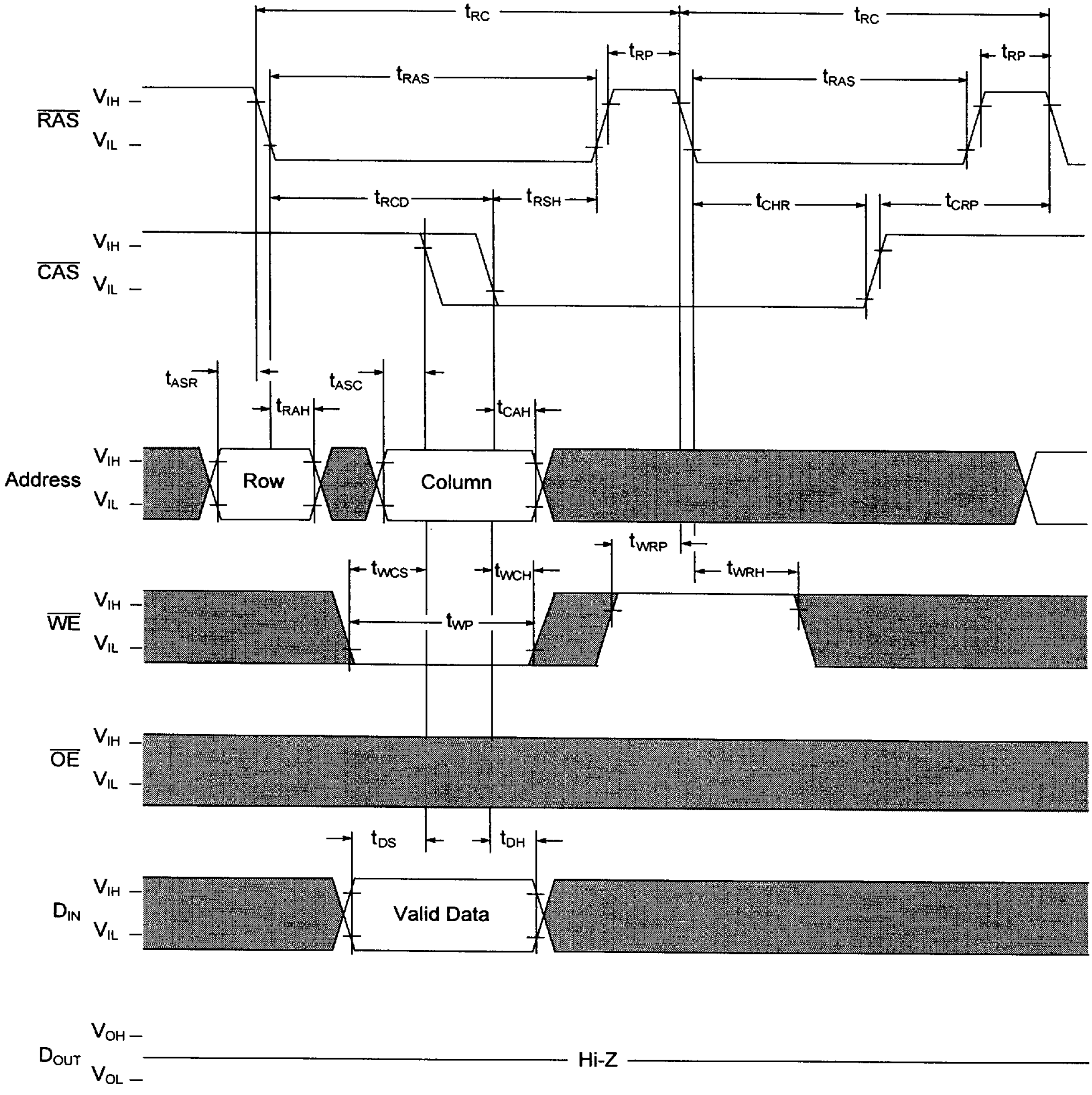
▨ : “H” or “L”

NOTE: Address is “H” or “L”

Hidden Refresh Cycle (Read)

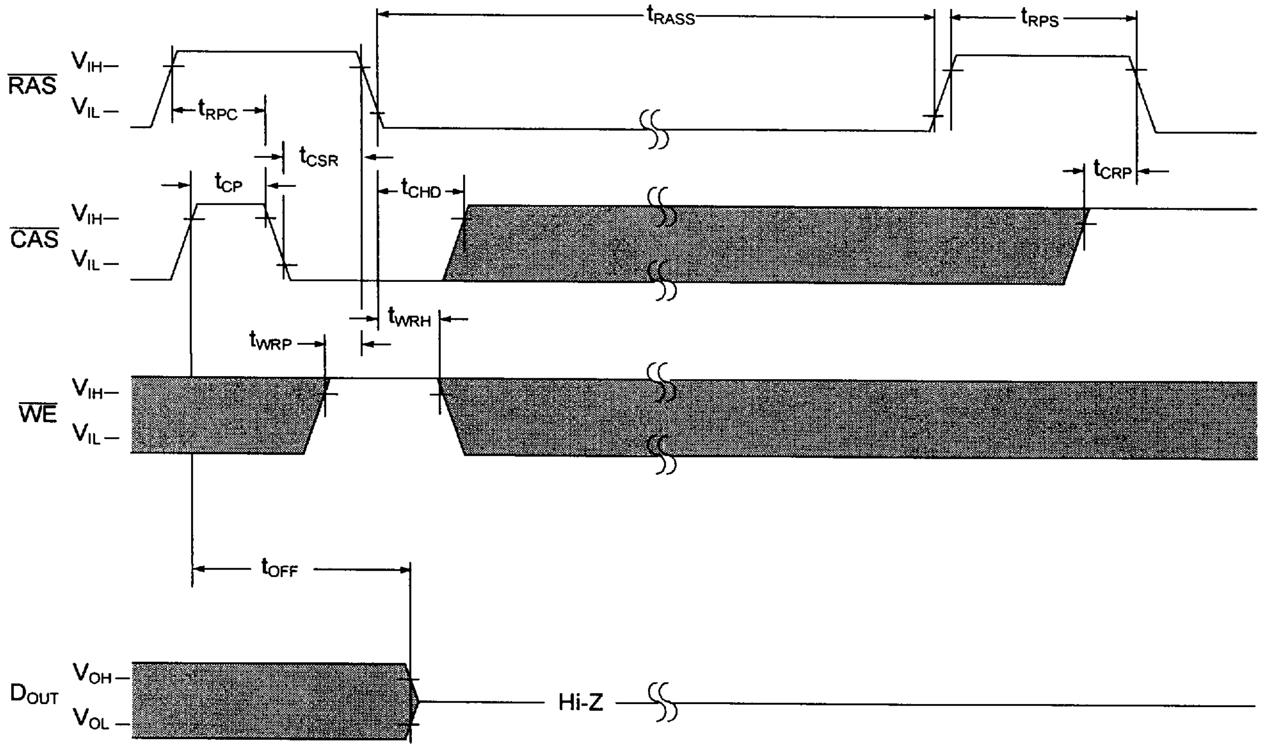


Hidden Refresh Cycle (Write)



▨ : “H” or “L”

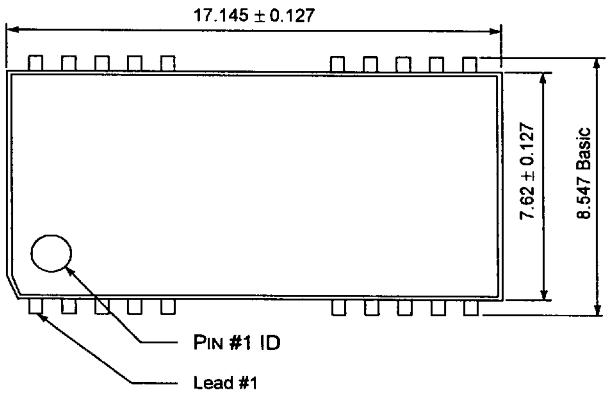
Self Refresh Cycle (Sleep Mode) - Low Power version only

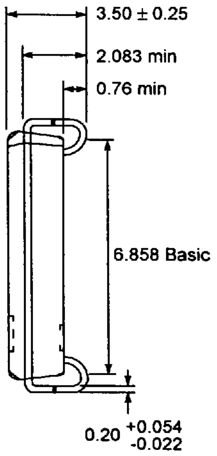


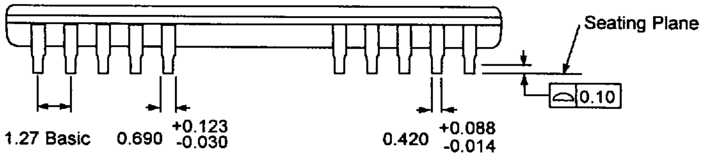
▨ : “H” or “L”

NOTE: Address and OE are “H” or “L”
Once $\overline{\text{RAS}}$ (min) is provided and $\overline{\text{RAS}}$ remains low, the DRAM will be in Self Refresh, commonly known as “Sleep Mode.”

Package Dimensions (300mil; 26/20 lead; Small Outline J-Lead)

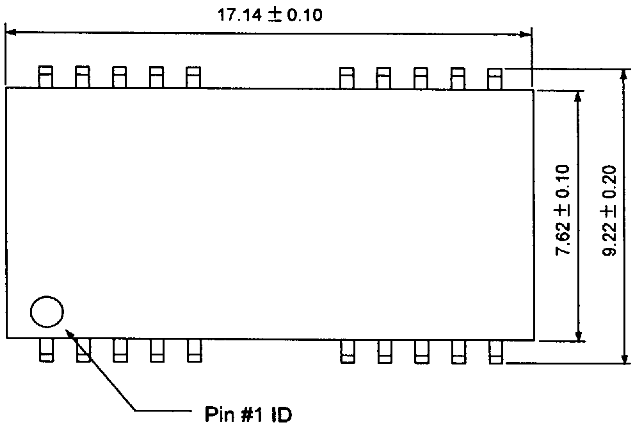


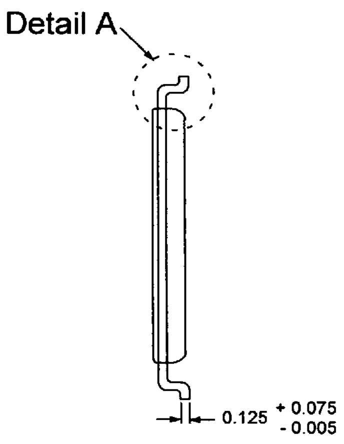


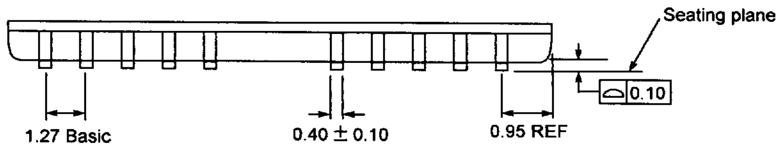


NOTE: All dimensions are in millimeters; Package diagrams are not drawn to scale.

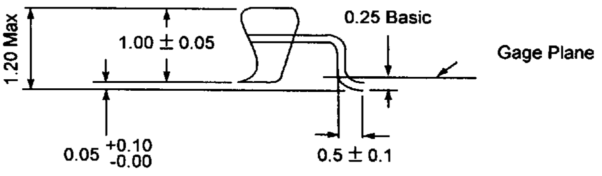
PACKAGE DIMENSIONS (300mil; 26/20 lead; Thin Small Outline Package)







Detail A



NOTE: All dimensions are in millimeters; Package diagrams are not drawn to scale.

Revision Log

Revision	Contents of Modification
12/13/94	Initial Release
01/17/95	1. t_{RPC} removed from $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle timing diagram (end of cycle only). $\overline{\text{CAS}}$ specified as "Don't Care" after t_{CHR}. 2. Corrected t_{RPC} value for -70; value changed from 10 to 0.
12/10/95	1. Packaging diagrams updated. 2. The Low Power and Standard Power Specifications were combined. ES# 27H4338 and ES# 27H4339 were combined into ES# 27H4339. 3. Truth Table added. 4. V_{IN} and V_{OUT} were added to the Absolute Maximum Ratings table. 5. t_{CAH} was changed from 15ns to 10ns for the -70 speed sort. 6. t_{DH} was reduced from 15ns to 12ns for the -60 speed sort. 7. t_{CHS} was removed from the Self Refresh Cycle. 8. t_{CHD} was added to the Self Refresh Cycle with a value of 10ns for all speed sorts. 9. The Self Refresh timing diagram was changed to allow $\overline{\text{CAS}}$ to go high t_{CHD} (10ns) after $\overline{\text{RAS}}$ falls entering a Self Refresh. 10. The CBR timing diagram was changed to allow $\overline{\text{CAS}}$ to remain low for back-to-back CBR cycles.
05/06/96	1. Die Revision G Part Numbers added. 2. Add Hidden Refresh (Write) timing diagram.