

# **F71863**

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## **Super Hardware Monitor + LPC I/O**

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**F71863 Datasheet Revision History**

| Version | Date       | Page  | Revision History  |
|---------|------------|-------|---|
| 0.10P   | 2006/04/21 | -     | Original Version  |
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| 0.21P   | 2006/06/20 | -     | Modify typo   |
| 0.22P   | 2006/07/06 | -     | Modify typo of register description                                       |
| 0.23P   | 2006/11/23 | -     | Remove GPIO17 function of pin66   |
|         |            | 62    | Modified the description of Wakeup Control Register 2Dh bit 7(SPI_CS1_EN) |
| 0.24P   | 2007/7/6   | -     | Company readdress   |
| 0.25P   | 2007/8/16  | 11-18 | Modify pin names of decription to matche pin configuration                |
| 0.26P   | 2008/1/30  | 99    | Modify operating temperature  |
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|         |            | -     | Modify power type of PWROK pin  |
| 0.28P   | 2008/5/26  | -     | Add register description of ACPI register F4h/F5h bit7                    |
| 0.29P   | 2008/7/21  | 52    | Add ST1/ST2 timing diagram  |
|         |            | 62    | Add register of new function( Index 29h bit 4-6)                          |
|         |            | 106   | Update application circuit  |

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## 1. General Description

The F71863 is the featured IO chip for PC system. Equipped with one IEEE 1284 Parallel Port, two UART Ports, Hardware Keyboard Controller, Serial Peripheral Interface (SPI), SIR and one FDC. The F71863 integrated with hardware monitor, 9 sets of voltage sensor, 3 sets of creative auto-controlling fans and 3 temperature sensor pins for the accurate dual current type temp. measurement for CPU thermal diode or external transistors 2N3906. Others, the F71863 supports newest AMDSI and Intel PECE interfaces for temperature sensing. For AMD platform, the F71863 provides the power sequence controller function.

The F71863 provides flexible features for multi-directional application. For instance, supports 4-In and 4-Out pins CPU VID controlling with offset implement., provides 25 GPIO pins (multi-pin), IRQ sharing function also designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature, provides 3 modes fan speed control mechanism included Manual Mode/Stage Auto Mode/Linear Auto Mode for users' selection.

The F71863 also integrated SPI interface. The SPI interface is for BIOS usage including bridge function and back up function. User can implement BIOS data in second flash to boot system when primary BIOS error. These features as above description will help you more and improve product value. Finally, the F71863 is powered by 3.3V voltage, with the LPC interface in the green package of 128-PQFP.

## 2. Feature List

### ● General Functions

- Comply with LPC Spec. 1.0
- Support DPM (Device Power Management), ACPI
- Support AMD power sequence controller
- 4-VIDIN and 4-VIDOUT for Vcore use
- Provides one FDC, two UARTs, Hardware KBC and Parallel Port
- H/W monitor functions
- SPI interface for BIOS usage
- Support AMD SID/SIC interface and Intel PECE interface
- 25 GPIO Pins for flexible application
- 24/48 MHz clock input
- Packaged in 128-PQFP and powered by 3.3VCC

**FDC**

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and under run conditions
- Built-in address mark detection circuit to simplify the read electronics
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate

**UART**

- Two high-speed 16C550 compatible UART with 16-byte FIFOs
- Fully programmable serial-interface characteristics
- Baud rate up to 115.2K
- Support IRQ sharing

**Infrared**

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

**Parallel Port**

- One PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

**Keyboard Controller**

- LPC interface support serial interrupt channel 1, 12.
- Two 16bit Programmable Address fully decoder, default 0x60 and 0x64.
- Support two PS/2 interface, one for PS/2 mouse and the other for keyboard.
- Keyboard's scan code support set1, set2.
- Programmable compatibility with the 8042.
- Support both interrupt and polling modes.
- Fast Gate A20 and Hardware Keyboard Reset.

- **Hardware Monitor Functions**

- 3 dual current type ( $\pm 3$  ) thermal inputs for CPU thermal diode and 2N3906 transistors
- Temperature range -40 ~127
- 9 sets voltage monitoring (6 external and 3 internal powers)
- High limit signal (PME#) for Vcore level
- 3 fan speed monitoring inputs
- 3 fan speed PWM/DC control outputs(support 3 wire and 4 wire fans)
- Stage auto mode ( 2-Limit and 3-Stage)/Linear auto mode/Manual mode
- Issue PME# and OVT# hardware signals output
- Case intrusion detection circuit
- WATCHDOG comparison of all monitored values

- **Serial Peripheral Interface Compatible**

- Support SPI Bridge Function for BIOS use
- Support Back Up BIOS function

- **Integrate AMD SI Interface**

- **Integrate Intel PECI Interface**

- **Support AMD Power Sequence Controller**

- **Package**

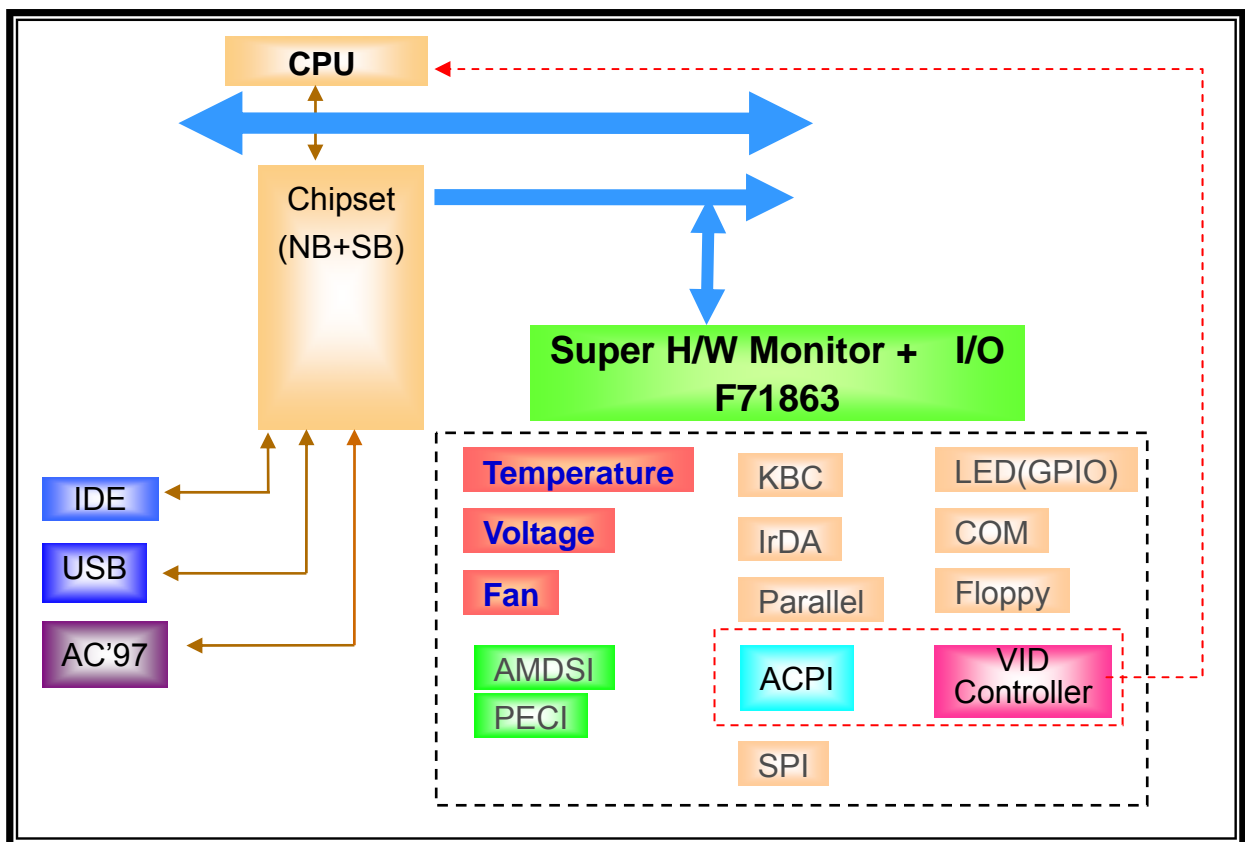
- 128-pin PQFP Green Package

Noted: Patented TW207103 TW207104 TW220442 US6788131 B1 TWI235231 TW237183 TW235553

### 3. Key Specification

|                            |              |
|----------------------------|--------------|
| ● Supply Voltage           | 3.0V to 3.6V |
| ● Operating Supply Current | 10 mA typ.   |

### 4. Block Diagram



### 5. Pin Configuration





## 6. Pin Description

- I/O<sub>12t</sub> - TTL level bi-directional pin with 12 mA source-sink cap ability.
- I/OOD<sub>12t</sub> - TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability.
- I/OD<sub>16t5v</sub> - TTL level bi-directional pin, Open-drain output with 16 mA source-sink capability, 5V tolerance.
- OD<sub>16-u10-5v</sub> - Open-drain output pin with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.
- I/OD<sub>12ts5v</sub> - TTL level bi-directional pin and schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.
- I<sub>Lv</sub>/OD<sub>D8-S1</sub> - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 8mA drive and 1mA sink capability.
- I<sub>Lv</sub>/OD<sub>12</sub> - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 12mA sink capability.
- O<sub>8-u47-5v</sub> - Open-drain pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.
- O<sub>8</sub> - Output pin with 8 mA source-sink capability.
- O<sub>12</sub> - Output pin with 12 mA source-sink capability.

|                     |   |
|---------------------|---|
| O <sub>30</sub>     | - Output pin with 30 mA source-sink capability.                   |
| AOUT                | - Output pin(Analog).   |
| OD <sub>12</sub>    | - Open-drain output pin with 12 mA sink capability.               |
| OD <sub>12-5v</sub> | - Open-drain output pin with 12 mA sink capability, 5V tolerance. |
| OD <sub>24</sub>    | - Open-drain output pin with 24 mA sink capability.               |
| IN <sub>ts5v</sub>  | - TTL level input pin,5V tolerance.                               |
| IN <sub>ts</sub>    | - TTL level input pin and schmitt trigger.                        |
| IN <sub>ts5v</sub>  | - TTL level input pin and schmitt trigger, 5V tolerance.          |
| AIN                 | - Input pin(Analog).  |
| P                   | - Power.  |

## 6.1 Power Pin

| Pin No.         | Pin Name | Type | Description                              |
|-----------------|----------|------|--|
| 4,37,99         | VCC      | P    | Power supply voltage input with 3.3V     |
| 68              | VSB      | P    | Stand-by power supply voltage input 3.3V |
| 86              | VBAT     | P    | Battery voltage input                    |
| 88              | AGND(D-) | P    | Analog GND                               |
| 20, 48, 73, 117 | GND      | P    | Digital GND                              |

## 6.2 LPC Interface

| Pin No. | Pin Name | Type               | PWR | Description   |
|---------|----------|--------------------|-----|---|
| 29      | LRESET#  | IN <sub>ts5v</sub> | VCC | Reset signal. It can connect to PCIRST# signal on the host.   |
| 30      | LDRQ#    | O <sub>12</sub>    | VCC | Encoded DMA Request signal.   |
| 31      | SERIRQ   | I/O <sub>12t</sub> | VCC | Serial IRQ input/Output.  |
| 32      | LFRAM#   | IN <sub>ts</sub>   | VCC | Indicates start of a new cycle or termination of a broken cycle.  |
| 36-33   | LAD[3:0] | I/O <sub>12t</sub> | VCC | These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral. |
| 38      | PCICLK   | IN <sub>ts</sub>   | VCC | 33MHz PCI clock input.  |
| 39      | CLKIN    | IN <sub>ts</sub>   | VCC | System clock input. According to the input frequency 24/48MHz.  |

## 6.3 FDC

| Pin No. | Pin Name | Type             | PWR | Description   |
|---------|----------|------------------|-----|---|
| 7       | DENSEL#  | OD <sub>24</sub> | VCC | Drive Density Select.<br>Set to 1 - High data rate.(500Kbps, 1Mbps)<br>Set to 0 – Low data rate. (250Kbps, 300Kbps) |
| 8       | MOA#     | OD <sub>24</sub> | VCC | Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.                             |
| 9       | DRVA#    | OD <sub>24</sub> | VCC | Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.                         |
| 10      | WDATA#   | OD <sub>24</sub> | VCC | Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An                   |

|    |         |                    |     |   |
|----|---------|--------------------|-----|---|
|    |         |                    |     | open drain output.  |
| 11 | DIR#    | OD <sub>24</sub>   | VCC | Direction of the head step motor. An open drain output.<br>Logic 1 = outward motion<br>Logic 0 = inward motion                                    |
| 12 | STEP#   | OD <sub>24</sub>   | VCC | Step output pulses. This active low open drain output produces a pulse to move the head to another track.   |
| 13 | HDSEL#  | OD <sub>24</sub>   | VCC | Head select. This open drain output determines which disk drive head is active.<br>Logic 1 = side 0<br>Logic 0 = side 1                           |
| 14 | WGATE#  | OD <sub>24</sub>   | VCC | Write enable. An open drain output.   |
| 15 | RDATA#  | IN <sub>ts5v</sub> | VCC | The read data input signal from the FDD.  |
| 16 | TRK0#   | IN <sub>ts5v</sub> | VCC | Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.                     |
| 17 | INDEX#  | IN <sub>ts5v</sub> | VCC | This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. |
| 18 | WPT#    | IN <sub>ts5v</sub> | VCC | Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.                                |
| 19 | DSKCHG# | IN <sub>ts5v</sub> | VCC | Diskette change. This signal is active low at power on and whenever the diskette is removed.  |

## 6.4 UART and SIR

| Pin No. | Pin Name  | Type                  | PWR | Description   |
|---------|-----------|-----------------------|-----|---|
| 27      | IRTX      | O <sub>12</sub>       | VCC | Infrared Transmitter Output.  |
|         | GPIO42    | I/OOD <sub>12t</sub>  |     | General Purpose IO  |
| 28      | IRRX      | IN <sub>ts</sub>      | VSB | Infrared Receiver input.  |
|         | GPIO43    | I/OOD <sub>12t</sub>  |     | General Purpose IO.   |
| 118     | DCD1#     | IN <sub>t5v</sub>     | VCC | Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.  |
| 119     | RI1#      | IN <sub>t5v</sub>     | VCC | Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.   |
| 120     | CTS1#     | IN <sub>t5v</sub>     | VCC | Clear To Send is the modem control input.   |
| 121     | DTR1#     | O <sub>8-u47,5v</sub> | VCC | UART 1 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping. |
|         | FAN60_100 | IN <sub>t5v</sub>     |     | Power on strapping pin:<br>1(Default): (Internal pull high)<br>Power on fan speed default duty is 60%.(PWM)<br>0: (External pull down)<br>Power on fan speed default duty is 100%.(PWM)     |
| 122     | RTS1#     | O <sub>8-u47,5v</sub> | VCC | UART 1 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable                             |

|     |             |                       |     |   |
|-----|-------------|-----------------------|-----|---|
|     |             |                       |     | after power on strapping.   |
| 123 | DSR1#       | IN <sub>t5v</sub>     | VCC | Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.  |
| 124 | SOUT1       | O <sub>8-u47,5v</sub> | VCC | UART 1 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.                                       |
|     | Config4E_2E | IN <sub>t5v</sub>     |     | Power on strapping: 1(Default)Configuration register:4E<br>0 Configuration register:2E  |
| 125 | SIN1        | IN <sub>t5v</sub>     | VCC | Serial Input. Used to receive serial data through the communication link.   |
| 126 | DCD2#       | IN <sub>t5v</sub>     | VCC | Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.  |
| 127 | RI2#        | IN <sub>t5v</sub>     | VCC | Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.   |
| 128 | CTS2#       | IN <sub>t5v</sub>     | VCC | Clear To Send is the modem control input.   |
| 1   | DTR2#       | O <sub>8-u47,5v</sub> | VCC | UART 2 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping. |
|     | FWH_TRAP    | IN <sub>t5v</sub>     |     | Power on strapping :<br>1(Default): SPI as a backup BIOS<br>0 : SPI as a primary BIOS   |
| 2   | RTS2#       | O <sub>8-u47,5v</sub> | VCC | UART 2 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.   |
|     | PWM_DC      | IN <sub>t5v</sub>     |     | Power on strapping :<br>1 (Default): Fan control method will be PWM Mode<br>0 Drive :Fan control method will be DAC Mode  |
| 3   | DSR2#       | IN <sub>t5v</sub>     | VCC | Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.  |
| 5   | SOUT2       | O <sub>8-u47,5v</sub> | VCC | UART 2 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.                                       |
|     | SPI_TRAP    | IN <sub>t5v</sub>     |     | Power on strapping:<br>1(Default) : SPI function disable<br>0 : SPI function enable   |
| 6   | SIN2        | IN <sub>t5v</sub>     | VCC | Serial Input. Used to receive serial data through the communication link.   |

|    |           |  |     |  |
|----|-----------|--|-----|--|
| 66 | CPU_PWRGD |  | VSB |  |
|----|-----------|--|-----|--|

## 6.5 Parallel Port

| Pin No. | Pin Name | Type                  | PWR | Description  |
|---------|----------|-----------------------|-----|--|
| 100     | SLCT     | IN <sub>ts5v</sub>    | VCC | An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.   |
| 101     | PE       | IN <sub>ts5v</sub>    | VCC | An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.                 |
| 102     | BUSY     | IN <sub>ts5v</sub>    | VCC | An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.                                      |
| 103     | ACK#     | IN <sub>ts5v</sub>    | VCC | An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| 104     | SLIN#    | OD <sub>12-5v</sub>   | VCC | Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.  |
| 105     | INIT#    | OD <sub>12-5v</sub>   | VCC | Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.  |
| 106     | ERR#     | IN <sub>ts5v</sub>    | VCC | An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.                 |
| 107     | AFD#     | OD <sub>12-5v</sub>   | VCC | An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.             |
| 108     | STB#     | OD <sub>12-5v</sub>   | VCC | An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.                                      |
| 109     | PD0      | I/O <sub>12ts5v</sub> | VCC | Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.  |
| 110     | PD1      | I/O <sub>12ts5v</sub> | VCC | Parallel port data bus bit 1.  |
| 111     | PD2      | I/O <sub>12ts5v</sub> | VCC | Parallel port data bus bit 2.  |
| 112     | PD3      | I/O <sub>12ts5v</sub> | VCC | Parallel port data bus bit 3.  |
| 113     | PD4      | I/O <sub>12ts5v</sub> | VCC | Parallel port data bus bit 4.  |
| 114     | PD5      | I/O <sub>12ts5v</sub> | VCC | Parallel port data bus bit 5.  |

|     |     |                       |     |                               |
|-----|-----|-----------------------|-----|-------------------------------|
| 115 | PD6 | I/O <sub>12ts5v</sub> | VCC | Parallel port data bus bit 6. |
| 116 | PD7 | I/O <sub>12ts5v</sub> | VCC | Parallel port data bus bit 7. |

## 6.6 Hardware Monitor

| Pin No. | Pin Name    | Type                        | PWR | Description   |
|---------|-------------|-----------------------------|-----|---|
| 93      | VIN6        | AIN                         | VCC | Voltage Input 6.  |
| 94      | VIN5        | AIN                         | VCC | Voltage Input 5.  |
| 95      | VDIMM(VIN4) | AIN                         | VCC | Voltage Input for VDIMM DUAL STR (2.5V/1.8V).   |
| 96      | VDDA(VIN3)  | AIN                         | VCC | Voltage Input for VDDA (2.5V).  |
| 97      | VLDT(VIN2)  | AIN                         | VCC | Voltage Input for VLDT (1.2V).  |
| 98      | Vcore(VIN1) | AIN                         | VCC | Voltage Input for Vcore.  |
| 21      | FANIN1      | IN <sub>ts5v</sub>          | VCC | Fan 1 tachometer input.   |
| 22      | FANCTL1     | OD <sub>12-5v</sub><br>AOUT | VCC | Fan 1 control output. This pin provides PWM duty-cycle output or a voltage output.  |
| 23      | FANIN2      | IN <sub>ts5v</sub>          | VCC | Fan 2 tachometer input.   |
| 24      | FANCTL2     | OD <sub>12-5v</sub><br>AOUT | VCC | Fan 2 control output. This pin provides PWM duty-cycle output or a voltage output.  |
| 25      | FANIN3      | IN <sub>ts5v</sub>          | VCC | Fan 3 speed input.  |
|         | GPIO40      | I/OOD <sub>12t</sub>        |     | General purpose IO.   |
| 26      | FANCTL3*    | OD <sub>12-5v</sub><br>AOUT | VCC | Fan 3 control output. This pin provides PWM duty-cycle output or a voltage output.<br>*This pin default function is FANCTL (PWM signal output), please take care the application if user want to implement GPIO function.   |
|         | GPIO41      | I/OOD <sub>12t</sub>        |     | General purpose IO.   |
| 89      | D3+(System) | AIN                         | VCC | Thermal diode/transistor temperature sensor input for system use.   |
| 90      | D2+         | AIN                         | VCC | Thermal diode/transistor temperature sensor input.  |
| 91      | D1+(CPU)    | AIN                         | VCC | CPU thermal diode/transistor temperature sensor input. This pin is for CPU use.   |
| 92      | VREF        | AOUT                        | VCC | Voltage sensor output.  |
| 79      | PME#        | OD <sub>12-5v</sub>         | VSB | Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the S3 state.  |
|         | GPIO25      | I/OOD <sub>12t</sub>        |     | General Purpose IO.   |
| 59      | GPIO10      | I/OOD <sub>12t</sub>        | VSB | General purpose IO.   |
|         | SPI_SLK     | O <sub>12</sub>             |     | Serial clock output pin for SPI device.   |
| 60      | GPIO11      | I/OOD <sub>12t</sub>        | VSB | General purpose IO.   |
|         | SPI_CS0#    | O <sub>12</sub>             |     | Function A: When using firmware hub BIOS for primary BIOS and SPI BIOS for second BIOS, please connect this pin to SPI BIOS chip select pin.<br>Function B: When using two SPI Flashes for primary and back up BIOS, please connect this pin to primary BIOS chip select pin. |
| 61      | GPIO12      | I/OOD <sub>12t</sub>        | VSB | General purpose IO.   |

|    |           |                      |     |   |
|----|-----------|----------------------|-----|---|
|    | SPI_MISO  | IN <sub>t5v</sub>    |     | SPI master in/slave out pin.  |
|    | FANCTL1_1 | OD <sub>12-5v</sub>  |     | Fan 1 control output. This pin provides PWM duty-cycle open drain output for Intel 4-pin Fan.                     |
| 62 | GPIO13    | I/OOD <sub>12t</sub> | VSB | General purpose IO.   |
|    | SPI_MOSI  | O <sub>12</sub>      |     | SPI master out/slave in pin.  |
|    | BEEP      | OD <sub>24</sub>     |     | Beep pin.   |
| 63 | GPIO14    | I/OOD <sub>12t</sub> | VSB | General purpose IO.   |
|    | FWH_DIS   | O <sub>12</sub>      |     | Firmware hub disable  |
|    | WDTRST#   | OD <sub>12-5v</sub>  |     | Watch dog timer signal output.  |
|    | SPI_CS1#  | O <sub>12</sub>      |     | When using two SPI Flashes for primary and back up BIOS, please connect this pin to back up BIOS chip select pin. |
| 67 | OVT#      | OD <sub>12-5v</sub>  | VSB | Over temperature signal output.   |

## 6.7 ACPI Function Pins

| Pin No. | Pin Name | Type                 | PWR  | Description  |
|---------|----------|----------------------|------|--|
| 64      | GPIO15   | I/OOD <sub>12t</sub> | VSB  | General purpose IO.  |
|         | LED_VSB  | OD <sub>12</sub>     |      | Power LED for VSB.   |
|         | ALERT#   | OD <sub>12</sub>     |      | Alert a signal when temperature over limit setting.  |
| 65      | GPIO16   | I/OOD <sub>12t</sub> | VSB  | General purpose IO.  |
|         | LED_VCC  | OD <sub>12</sub>     |      | Power LED for VCC.   |
| 74      | PCIRST1# | OD <sub>12</sub>     | VSB  | It is a output buffer of LRESET#.  |
|         | GPIO20   | I/OOD <sub>12</sub>  |      | General purpose IO.  |
| 75      | PCIRST2# | O <sub>12</sub>      | VSB  | It is a output buffer of LRESET#.  |
|         | GPIO21   | I/OOD <sub>12</sub>  |      | General purpose IO.  |
| 76      | PCIRST3# | O <sub>12</sub>      | VSB  | It is a output buffer of LRESET#.  |
|         | GPIO22   | I/OOD <sub>12</sub>  |      | General purpose IO.  |
| 77      | S5#      | IN <sub>ts5v</sub>   | VSB  | S5# signal input.  |
| 78      | ATXPG_IN | AIN                  | VSB  | ATX Power Good input.  |
|         | GPIO24   | I/OOD <sub>12t</sub> |      | General purpose IO.  |
| 84      | PWROK    | OD <sub>12</sub>     | VBAT | PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V. |
|         | GPIO32   | I/OOD <sub>12t</sub> |      | General purpose IO.  |
| 80      | PWSIN#   | IN <sub>ts5v</sub>   | VSB  | Main power switch button input.  |
|         | GPIO26   | I/OOD <sub>12t</sub> |      | General purpose IO.  |
| 81      | PWSOUT#  | OD <sub>12</sub>     | VSB  | Panel Switch Output. This pin is low active and pulse output. It is power on request output#.            |
|         | GPIO27   | I/OOD <sub>12t</sub> |      | General purpose IO.  |
| 82      | S3#      | IN <sub>ts5v</sub>   | VSB  | S3# Input is Main power on-off switch input.   |
|         | GPIO30   | I/OOD <sub>12t</sub> |      | General purpose IO.  |
| 83      | PS_ON#   | OD <sub>12-5v</sub>  | VSB  | Power supply on-off control output. Connect to ATX power supply PS_ON# signal.                           |

|    |         |                      |      |   |
|----|---------|----------------------|------|---|
|    | GPIO31  | I/OOD <sub>12t</sub> |      | General purpose IO.   |
| 85 | RSMRST# | OD <sub>12</sub>     | VBAT | Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 2.3V.   |
|    | GPIO33  | I/OOD <sub>12t</sub> |      | General purpose IO.   |
| 87 | COPEN#  | IN <sub>ts5v</sub>   | VBAT | Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power loss. |

## 6.8 VID Controller and Others

| Pin No. | Pin Name    | Type                                | PWR | Description  |
|---------|-------------|-------------------------------------|-----|--|
| 45-42   | VIDIN[D:A]  | IN <sub>ts5v</sub>                  | VCC | CPU VID input pins.<br>Special level input VIH → 0.9, VIL → 0.6  |
| 52-49   | VIDOUT[D:A] | OD <sub>12</sub>                    | VSB | CPU VID output pins.   |
| 46      | Vcore_EN    | OD <sub>12</sub>                    | VCC | Active high. The function of this pin is to enable the PWM for CPU Vcore. The external pull high resistor is required.   |
| 47      | VLDT_EN     | OD <sub>12</sub>                    | VCC | Active high. The function of this pin is to enable the VLDT voltage. The external pull high resistor is required.  |
| 53      | VDDA_EN     | OD <sub>12</sub>                    | VSB | Active high. The function of this pin is to enable the VDDA power for AMD K8 and after CPU. The external pull high resistor is required.   |
| 54      | VDIMM_EN    | OD <sub>12</sub>                    | VSB | Active high. The function of this pin is to enable the PWM for VDIMM_STR dual voltage. The external pull high resistor is required.  |
| 55      | ST2         | OD <sub>12</sub>                    | VSB | Status Pin2 for S0#/S3#/S5# states application.<br>In S0# → ST2 pin status is Tri-state.<br>In S3# → ST2 pin status is Low level.<br>In S5# → ST2 pin status is Low level, and can be programmed to Tri-state. |
|         | SLOT0CC#    | IN <sub>ts5v</sub>                  |     | CPU SLOT0CC# input.  |
|         | GPIO02      | I/OOD <sub>12t</sub>                |     | General purpose pin.   |
| 56      | ST1         | OD <sub>12</sub>                    | VSB | Status Pin1 for S0#/S3#/S5# states application.<br>In S0# → ST1 pin status is Tri-state.<br>In S3# → ST1 pin status is Low level.<br>In S5# → ST1 pin status is Tri-state.                                     |
|         | GPIO03      | I/OOD <sub>12t</sub>                |     | General purpose pin.   |
|         | WDTRST#     | OD <sub>12-5v</sub>                 |     | Watch dog timer signal output.   |
| 57      | AMDSI_CLK   | OD <sub>12</sub>                    | VSB | AMDSI interface clock output.  |
| 58      | PECI        | I <sub>Lv</sub> /O <sub>D8-S1</sub> | VSB | Intel Peci hardware monitor interface.   |
|         | AMDSI_DAT_1 | I <sub>Lv</sub> /OD <sub>12</sub>   |     | AMDSI interface data input.  |



## 6.9 KBC Function

| Pin No. | Pin Name | Type                    | PWR | Description  |
|---------|----------|-------------------------|-----|--|
| 40      | KBRST#   | OD <sub>16-u10,5V</sub> | VCC | Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P20)  |
| 41      | GA20     | OD <sub>16-u10,5V</sub> | VCC | Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21) |
| 69      | KDATA    | I/OD <sub>16t,5V</sub>  | VSB | Keyboard Data.   |
| 70      | KCLK     | I/OD <sub>16t,5V</sub>  | VSB | Keyboard Clock.  |
| 71      | MDATA    | I/OD <sub>16t,5V</sub>  | VSB | PS2 Mouse Data.  |
| 72      | MCLK     | I/OD <sub>16t,5V</sub>  | VSB | PS2 Mouse Clock.   |

## 7. Function Description

### 7.1 Power on Strapping Option

The F71863 provides four pins for power on hardware strapping to select functions. There is a form to describe how to set the functions you want.

| Pin No. | Symbol      | Value | Description  |
|---------|-------------|-------|--|
| 1       | FWH_TRAP    | 1     | SPI as a backup BIOS (Default)                       |
|         |             | 0     | SPI as a primary BIOS                                |
| 2       | PWM_DC      | 1     | Fan control mode: PWM mode. ( Default)               |
|         |             | 0     | Fan control mode: Linear mode.                       |
| 5       | SPI_TRAP    | 1     | SPI function disable (Default)                       |
|         |             | 0     | SPI function enable                                  |
| 121     | FAN60_100   | 1     | Power on Fan speed default duty is 60%(PWM)(Default) |
|         |             | 0     | Power on Fan speed default duty is 100%(PWM)         |
| 124     | Config4E_2E | 1     | Configuration Register I/O port is 4E/4F. (Default)  |
|         |             | 0     | Configuration Register I/O port is 2E/2F.            |

### 7.2 FDC

The Floppy Disk Controller provides the interface between a host processor and one floppy disk drives. It integrates a controller and a digital data separator with write pre-compensation, data rate selection logic, microprocessor interface, and a set of registers. The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in PC/AT mode and supports 3-mode type drives.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors in the data or operation of the FDC/FDD. The controller manages data transfers using a set of data transfer and control commands. These commands are handled in three phases: Command, Execution, and Result. Not all commands utilize all these three phases.

The below content is about the FDC device register descriptions. All the registers are for software porting reference.

**Status Register A (PS/2 mode) — Base + 0**

| Bit | Name    | R/W | Default | Description  |
|-----|---------|-----|---------|--|
| 7   | INTPEND | R   | 0       | This bit indicates the state of the interrupt output.  |
| 6   | DRV2_N  | R   | -       | 0: a second drive has been installed.<br>1: a second drive has not been installed.   |
| 5   | STEP    | R   | 0       | This bit indicates the complement of STEP# disk interface output.  |
| 4   | TRK0_N  | R   | -       | This bit indicates the state of TRK0# disk interface input.  |
| 3   | HDSEL   | R   | 0       | This bit indicates the complement of HDSEL# disk interface output.<br>0: side 0.<br>1: side 1.                               |
| 2   | INDEX_N | R   | -       | This bit indicates the state of INDEX# disk interface input.   |
| 1   | WPT_N   | R   | -       | This bit indicates the state of WPT# disk interface input.<br>0: disk is write-protected.<br>1: disk is not write-protected. |
| 0   | DIR     | R   | 0       | This bit indicates the complement of DIR# disk interface output.   |

**Status Register A (Model 30 mode) — Base + 0**

| Bit | Name    | R/W | Default | Description  |
|-----|---------|-----|---------|--|
| 7   | INTPEND | R   | 0       | This bit indicates the state of the interrupt output.  |
| 6   | DRQ     | R   | 0       | This bit indicates the state of the DRQ signal.  |
| 5   | STEP_FF | R   | 0       | This bit indicates the complement of latched STEP# disk interface output.  |
| 4   | TRK0    | R   | -       | This bit indicates the complement of TRK0# disk interface input.   |
| 3   | HDSEL_N | R   | 1       | This bit indicates the state of HDSEL# disk interface output.<br>0: side 0.<br>1: side 1.  |
| 2   | INDEX   | R   | -       | This bit indicates the complement of INDEX# disk interface input.  |
| 1   | WPT     | R   | -       | This bit indicates the complement of WPT# disk interface input.<br>0: disk is write-protected.<br>1: disk is not write-protected.        |
| 0   | DIR_N   | R   | 1       | This bit indicates the state of DIR# disk interface output.<br>0: head moves in inward direction.<br>1: head moves in outward direction. |

**Status Register B (PS/2 Mode) — Base + 1**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-6 | Reserved | R   | 11      | Reserved. Return 11b when read.  |
| 5   | DR0      | R   | 0       | Drive select 0. This bit reflects the bit 0 of Digital Output Register.                      |
| 4   | WDATA    | R   | 0       | This bit changes state at every rising edge of WDATA#.                                       |
| 3   | RDATA    | R   | 0       | This bit changes state at every rising edge of RDATA#.                                       |
| 2   | WGATE    | R   | 0       | This bit indicates the complement of WGATE# disk interface output.                           |
| 1   | MOTEN1   | R   | 0       | This bit indicates the complement of MOB# disk interface output. Not support in this design. |

|   |        |   |   |  |
|---|--------|---|---|--|
| 0 | MOTEN0 | R | 0 | This bit indicates the complement of MOA# disk interface output. |
|---|--------|---|---|--|

**Status Register B (Model 30 Mode) — Base + 1**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7   | DRV2_N   | R   | -       | 0: a second drive has been installed.<br>1: a second drive has not been installed.                          |
| 6   | DSB_N    | R   | 1       | This bit indicates the state of DRVB# disk interface output. Not support in this design.                    |
| 5   | DSA_N    | R   | 1       | This bit indicates the state of DRVA# disk interface output.  |
| 4   | WDATA_FF | R   | 0       | This bit is latched at the rising edge of WDATA# and is cleared by a read from the Digital Input Register.  |
| 3   | RDATA_FF | R   | 0       | This bit is latched at the rising edge of RDATA# and is cleared by a read from the Digital Input Register.  |
| 2   | WGATE_FF | R   | 0       | This bit is latched at the falling edge of WGATE# and is cleared by a read from the Digital Input Register. |
| 1   | DSD_N    | R   | 1       | This bit indicates the complement of DRVD# disk interface output. Not support in this design.               |
| 0   | DSC_N    | R   | 1       | This bit indicates the complement of DRVC# disk interface output. Not support in this design.               |

**Digital Output Register — Base + 2**

| Bit | Name   | R/W | Default | Description   |
|-----|--------|-----|---------|---|
| 7   | MOTEN3 | R   | 0       | Motor enable 3. Not support in this design.   |
| 6   | MOTEN2 | R   | 0       | Motor enable 2. Not support in this design.   |
| 5   | MOTEN1 | R/W | 0       | Motor enable 1. Used to control MOB#. MOB# is not support in this design.   |
| 4   | MOTEN0 | R/W | 0       | Motor enable 0. Used to control MOA#.   |
| 3   | DAMEN  | R/W | 0       | DMA enable. This bit has two mode of operation.<br>PC-AT and Model 30 mode: write 1 will enable DMA and IRQ, write 0 will disable DMA and IRQ.<br>PS/2 mode: This bit is reserved. DMA and IRQ are always enabled in PS/2 mode. |
| 2   | RESET  | R   | 0       | Write 0 to this bit will reset the controller. I will remain in reset condition until a 1 is written.   |
| 1   | DSD_N  | R   | 1       | This bit indicates the complement of DRVD# disk interface output. Not support in this design.   |
| 0   | DSC_N  | R   | 1       | This bit indicates the complement of DRVC# disk interface output. Not support in this design.   |

**Tape Drive Register — Base + 3**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-6 | Reserved | R   | 00      | Reserved. Return 00b when read.   |
| 5-4 | TYPEID   | R   | 11      | Reserved in normal function, return 11b when read.<br>If 3 mode FDD function is enabled. These bits indicate the drive type ID. |

|     |          |     |    |  |
|-----|----------|-----|----|--|
| 3-2 | Reserved | R   | 11 | Reserved. Return 11b when read in normal function.<br>Return 00b when read in 3 mode FDD function. |
| 1-0 | TAPESL   | R/W | 0  | These bits assign a logical drive number to be a tape drive.                                       |

**Main Status Register — Base + 4**

| Bit | Name      | R/W | Default | Description  |
|-----|-----------|-----|---------|--|
| 7   | RQM       | R   | 0       | Request for Master indicates that the controller is ready to send or receive data from the uP through the FIFO.  |
| 6   | DIO       | R   | 0       | Data I/O (direction):<br>0: the controller is expecting a byte to be written to the Data Register.<br>1: the controller is expecting a byte to be read from the Data Register. |
| 5   | NON_DMA   | R   | 0       | Non DMA Mode:<br>0: the controller is in DAM mode.<br>1: the controller is interrupt or software polling mode.   |
| 4   | FDC_BUSY  | R   | 0       | This bit indicate that a read or write command is in process.  |
| 3   | DRV3_BUSY | R   | 0       | FDD number 3 is in seek or calibration condition. FDD number 3 is not support in this design.  |
| 2   | DRV2_BUSY | R   | 0       | FDD number 2 is in seek or calibration condition. FDD number 2 is not support in this design.  |
| 1   | DRV1_BUSY | R   | 0       | FDD number 1 is in seek or calibration condition. FDD number 1 is not support in this design.  |
| 0   | DRV0_BUSY | R   | 0       | FDD number 0 is in seek or calibration condition.  |

**Data Rate Select Register — Base + 4**

| Bit                    | Name              | R/W | Default | Description   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
|------------------------|-------------------|-----|---------|---|------------|-------|---------------------|----------------|--------------|---------|--------------|---------|---------------|---------|---------------|--------|---------------|---------|---------------|----------|------------------------|-------------------|
| 7                      | SOFTST            | W   | 0       | A 1 written to this bit will software reset the controller. Auto clear after reset.   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 6                      | PWRDOWN           | W   | 0       | A 1 to this bit will put the controller into low power mode which will turn off the oscillator and data separator circuits.   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 5                      | Reserved          | -   | -       | Return 0 when read.   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 4-2                    | PRECOMP           | W   | 000     | Select the value of write precompensation:<br><table style="margin-left: 20px;"> <tr> <td>250K-1Mbps</td> <td>2Mbps</td> </tr> <tr> <td>000: default delays</td> <td>default delays</td> </tr> <tr> <td>001: 41.67ns</td> <td>20.8ns</td> </tr> <tr> <td>010: 83.34ns</td> <td>41.17ns</td> </tr> <tr> <td>011: 125.00ns</td> <td>62.5ns</td> </tr> <tr> <td>100: 166.67ns</td> <td>83.3ns</td> </tr> <tr> <td>101: 208.33ns</td> <td>104.2ns</td> </tr> <tr> <td>110: 250.00ns</td> <td>125.00ns</td> </tr> <tr> <td>111: 0.00ns (disabled)</td> <td>0.00ns (disabled)</td> </tr> </table><br>The default value of corresponding data rate:<br>250Kbps: 125ns<br>300Kbps: 125ns<br>500Kbps: 125ns<br>1Mbps: 41.67ns<br>2Mbps: 20.8ns | 250K-1Mbps | 2Mbps | 000: default delays | default delays | 001: 41.67ns | 20.8ns  | 010: 83.34ns | 41.17ns | 011: 125.00ns | 62.5ns  | 100: 166.67ns | 83.3ns | 101: 208.33ns | 104.2ns | 110: 250.00ns | 125.00ns | 111: 0.00ns (disabled) | 0.00ns (disabled) |
| 250K-1Mbps             | 2Mbps             |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 000: default delays    | default delays    |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 001: 41.67ns           | 20.8ns            |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 010: 83.34ns           | 41.17ns           |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 011: 125.00ns          | 62.5ns            |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 100: 166.67ns          | 83.3ns            |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 101: 208.33ns          | 104.2ns           |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 110: 250.00ns          | 125.00ns          |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 111: 0.00ns (disabled) | 0.00ns (disabled) |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 1-0                    | DRATE             | W   | 10      | Data rate select:<br><table style="margin-left: 20px;"> <tr> <td>MFM</td> <td>FM</td> </tr> <tr> <td>00: 500Kbps</td> <td>250Kbps</td> </tr> <tr> <td>01: 300Kbps</td> <td>150Kbps</td> </tr> <tr> <td>10: 250Kbps</td> <td>125Kbps</td> </tr> <tr> <td>11: 1Mbps</td> <td>illegal</td> </tr> </table>  | MFM        | FM    | 00: 500Kbps         | 250Kbps        | 01: 300Kbps  | 150Kbps | 10: 250Kbps  | 125Kbps | 11: 1Mbps     | illegal |               |        |               |         |               |          |                        |                   |
| MFM                    | FM                |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 00: 500Kbps            | 250Kbps           |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 01: 300Kbps            | 150Kbps           |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 10: 250Kbps            | 125Kbps           |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |
| 11: 1Mbps              | illegal           |     |         |   |            |       |                     |                |              |         |              |         |               |         |               |        |               |         |               |          |                        |                   |

**Data (FIFO) Register — Base + 5**

| Bit | Name | R/W | Default | Description   |
|-----|------|-----|---------|---|
| 7-0 | DATA | R/W | 00h     | The FIFO is used to transfer all commands, data and status between controller and the system. The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. The FIFO is default disabled and could be enabled via the CONFIGURE command. |

**Status Registers 0**

| Bit | Name | R/W | Default | Description  |
|-----|------|-----|---------|--|
| 7-6 | IC   | R   | -       | Interrupt code :<br>00: Normal termination of command.<br>01: Abnormal termination of command.<br>10: Invalid command.<br>11: Abnormal termination caused by poling. |
| 5   | SE   | R   | -       | Seek end.<br>Set when a SEEK or RECALIBRATE or a READ or WRITE with implied seek command is completed.   |
| 4   | EC   | R   | -       | Equipment check.<br>0: No error<br>1: When a fault signal is received form the FDD or the TRK0# signal fails to occur after 77 step pulses.                          |
| 3   | NR   | R   | -       | Not ready.<br>0: Drive is ready<br>1: Drive is not ready.  |
| 2   | HD   | R   | -       | Head address.<br>The current head address.   |
| 1-0 | DS   | R   | -       | Drive select.<br>00: Drive A selected.<br>01: Drive B selected.<br>10: Drive C selected.<br>11: Drive D selected.  |

**Status Registers 1**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7   | EN       | R   | -       | End of Track.<br>Set when the FDC tries to access a sector beyond the final sector of a cylinder.                             |
| 6   | DE       | R   | -       | Data Error.<br>The FDC detect a CRC error in either the ID field or the data field of a sector.                               |
| 4   | OR       | R   | -       | Overrun/Underrun.<br>Set when the FDC is not serviced by the host system within a certain time interval during data transfer. |
| 3   | Reserved | -   | -       | Unused. This bit is always "0"  |

|   |    |   |   |   |
|---|----|---|---|---|
| 2 | ND | R | - | No Data.<br>Set when the following conditions occurred:<br>1. The specified sector is not found during any read command.<br>2. The ID field cannot be read without errors during a READ ID command.<br>3. The proper sector sequence cannot be found during a READ TRACK command.               |
| 1 | NW | R | - | No Writable<br>Set when WPT# is active during execution of write commands.  |
| 0 | MA | R | - | Missing Address Mark.<br>Set when the following conditions occurred:<br>1. Cannot detect an ID address mark at the specified track after encountering the index pulse from the INDEX# pin twice.<br>2. Cannot detect a data address mark or a deleted data address mark on the specified track. |

**Status Registers 2**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7   | Reserved | -   | -       | Unused. This bit is always "0".  |
| 6   | CM       | R   | -       | Control Mark.<br>Set when following conditions occurred:<br>1. Encounters a deleted data address mark during a READ DATA command.<br>2. Encounters a data address mark during a READ DELETED DATA command. |
| 5   | DD       | R   | -       | Data Error in Data Field.<br>The FDC detects a CRC error in the data field.  |
| 4   | WC       | R   | -       | Wrong Cylinder.<br>Set when the track address from the sector ID field is different from the track address maintained inside the FDC.  |
| 3   | SE       | R   | -       | Scan Equal.<br>Set if the equal condition is satisfied during execution of the SCAN command.   |
| 2   | SN       | R   | -       | Scan Not Satisfied.<br>Set when the FDC cannot find a sector on the track which meets the desired condition during any scan command.   |
| 1   | BC       | R   | -       | Bad Cylinder.<br>The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FFh which indicates a bad track.                                 |
| 0   | MD       | R   | -       | Missing Data Address Mark.<br>Set when the FDC cannot detect a data address mark or a deleted data address mark.   |

**Status Registers 3**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7   | Reserved | -   | -       | Unused. This bit is always "0".                     |
| 6   | WP       | R   | -       | Write Protect.<br>Indicates the status of WPT# pin. |
| 5   | Reserved | R   | -       | Unused. This bit is always "1".                     |

|   |           |   |   |   |
|---|-----------|---|---|---|
| 4 | T0        | R | - | Track 0.<br>Indicates the status of the TRK0# pin.              |
| 3 | Reserved. | R | - | Unused. This bit is always "1".                                 |
| 2 | HD        | R | - | Head Address.<br>Indicates the status of the HDSEL# pin.        |
| 1 | DS1       | R | - | Drive Select.   |
| 0 | DS0       | R | - | These two bits indicate the DS1, DS0 bits in the command phase. |

**Digital Input Register (PC-AT Mode) — Base + 7**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7   | DSKCHG   | R   | -       | This bit indicates the complement of DSKCHG# disk interface input. |
| 6-0 | Reserved | R   | -       | Reserved.  |

**Digital Input Register (PS/2 Mode) — Base + 7**

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7   | DSKCHG    | R   | -       | This bit indicates the complement of DSKCHG# disk interface input.  |
| 6-3 | Reserved  | -   | -       | Reserved.   |
| 2-1 | DRATE     | R   | 10      | These bits indicate the status of the DRATE programmed through the Data Rate Select Register or Configuration Control Register. |
| 0   | HIGHDEN_N | R   | 1       | 0: 1Mbps or 500Kbps data rate is chosen.<br>1: 300Kbps or 250Kbps data rate is chosen.  |

**Digital Input Register (Model 30 Mode) — Base + 7**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7   | DSKCHG_N | R   | -       | This bit indicates the state of DSKCHG# disk interface input.   |
| 6-4 | Reserved | -   | -       | Reserved.   |
| 3   | DMAEN    | R   | 0       | This bit reflects the DMA bit in Digital Output Register.   |
| 2   | NOPRE    | R   | 0       | This bit reflects the NOPRE bit in Configuration Control Register.  |
| 1-0 | DRATE    | R   | 10      | These bits indicate the status of DRATE programmed through the Data Rate Select Register or Configuration Control Register. |

**Configuration Control Register (PC-AT and PS/2 Mode) — Base + 7**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-2 | Reserved | -   | -       | Reserved.  |
| 1-0 | DRATE    | W   | 10      | These bit determine the data rate of the floppy controller. See DRATE bits in Data Rate Select Register. |



**Configuration Control Register (Model 30 Mode) — Base + 7**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-3 | Reserved | -   | -       | Reserved.  |
| 2   | NOPRE    | W   | 0       | This bit could be programmed through Configuration Control Register and be read through the bit 2 in Digital Input Register in Model 30 Mode. But it has no functionality. |
| 1-0 | DRATE    | W   | 10      | These bit determine the data rate of the floppy controller. See DRATE bits in Data Rate Select Register.   |

**FDC Commands**

Terminology:

|         |  |
|---------|--|
| C       | Cylinder Number 0 -256   |
| D       | Data Pattern   |
| DIR     | Step Direction<br>0: step out<br>1: step in  |
| DS0     | Drive Select 0   |
| DS1     | Drive Select 1   |
| DTL     | Data Length  |
| EC      | Enable Count   |
| EOT     | End of Track   |
| EFIFO   | Enable FIFO<br>0: FIFO is enabled.<br>1: FIFO is disabled.   |
| EIS     | Enable Implied Seek  |
| FIFOTHR | FIFO Threshold   |
| GAP     | Alters Gap Length  |
| GPL     | Gap Length   |
| H/HDS   | Head Address   |
| HLT     | Head Load Time   |
| HUT     | Head Unload Time   |
| LOCK    | Lock EFIFO, FIFOTHR, PTRTRK bits.<br>Prevent these bits from being affected by software reset.                   |
| MFM     | MFM or FM mode<br>0: FM<br>1: MFM  |
| MT      | Multi-Track  |
| N       | Sector Size Code. All values up to 07h are allowable.<br>00: 128 bytes<br>01: 256 bytes<br>.. ..<br>07 16 Kbytes |
| NCN     | New Cylinder Number  |
| ND      | Non-DMA Mode   |
| OW      | Overwritten  |
| PCN     | Present Cylinder Number  |
| POLL    | Polling disable<br>0: polling is enabled.<br>1: polling is disabled.   |
| PRETRK  | Precompensation Start Track Number   |
| R       | Sector address   |
| RCN     | Relative Cylinder Number   |

SC Sector per Cylinder  
 SK Skip deleted data address mark  
 SRT Step Rate Time  
 ST0 Status Register 0  
 ST1 Status Register 1  
 ST2 Status Register 2  
 ST3 Status Register 3  
 WGate Write Gate alters timing of WE.

**Read Data**

| Phase     | R/W             | D7              | D6  | D5 | D4 | D3 | D2  | D1  | D0  | Remark   |  |
|-----------|-----------------|-----------------|-----|----|----|----|-----|-----|-----|--|--|
| Command   | W               | MT              | MFM | SK | 0  | 0  | 1   | 1   | 0   | Command code                                   |  |
|           | W               | 0               | 0   | 0  | 0  | 0  | HDS | DS1 | DS0 |  |  |
|           | W               | ----- C -----   |     |    |    |    |     |     |     |  | Sector ID information prior to command execution |
|           | W               | ----- H -----   |     |    |    |    |     |     |     |  |  |
|           | W               | ----- R -----   |     |    |    |    |     |     |     |  |  |
|           | W               | ----- N -----   |     |    |    |    |     |     |     |  |  |
|           | W               | ----- EOT ----- |     |    |    |    |     |     |     |  |  |
|           | W               | ----- GPL ----- |     |    |    |    |     |     |     |  |  |
| W         | ----- DTL ----- |                 |     |    |    |    |     |     |     |  |  |
| Execution |                 |                 |     |    |    |    |     |     |     | Data transfer between the FDD and system       |  |
| Result    | R               | ----- ST0 ----- |     |    |    |    |     |     |     | Status information after command execution.    |  |
|           | R               | ----- ST1 ----- |     |    |    |    |     |     |     |  |  |
|           | R               | ----- ST2 ----- |     |    |    |    |     |     |     |  |  |
|           | R               | ----- C -----   |     |    |    |    |     |     |     | Sector ID information after command execution. |  |
|           | R               | ----- H -----   |     |    |    |    |     |     |     |  |  |
|           | R               | ----- R -----   |     |    |    |    |     |     |     |  |  |
|           | R               | ----- N -----   |     |    |    |    |     |     |     |  |  |

**Read Deleted Data**

| Phase   | R/W | D7              | D6  | D5 | D4 | D3 | D2  | D1  | D0  | Remark       |  |
|---------|-----|-----------------|-----|----|----|----|-----|-----|-----|--------------|--|
| Command | W   | MT              | MFM | SK | 0  | 1  | 1   | 0   | 0   | Command code |  |
|         | W   | 0               | 0   | 0  | 0  | 0  | HDS | DS1 | DS0 |              |  |
|         | W   | ----- C -----   |     |    |    |    |     |     |     |              | Sector ID information prior to command execution |
|         | W   | ----- H -----   |     |    |    |    |     |     |     |              |  |
|         | W   | ----- R -----   |     |    |    |    |     |     |     |              |  |
|         | W   | ----- N -----   |     |    |    |    |     |     |     |              |  |
|         | W   | ----- EOT ----- |     |    |    |    |     |     |     |              |  |
|         | W   | ----- GPL ----- |     |    |    |    |     |     |     |              |  |
| W       |     |                 |     |    |    |    |     |     |     |              |  |

|           |   |                 |  |
|-----------|---|-----------------|--|
|           | W | ----- DTL ----- |  |
| Execution |   |                 | Data transfer between the FDD and system       |
| Result    | R | ----- ST0 ----- | Status information after command execution.    |
|           | R | ----- ST1 ----- |  |
|           | R | ----- ST2 ----- |  |
|           | R | ----- C -----   | Sector ID information after command execution. |
|           | R | ----- H -----   |  |
|           | R | ----- R -----   |  |
|           | R | ----- N -----   |  |

**Read A Track**

| Phase     | R/W | D7 | D6  | D5 | D4 | D3 | D2              | D1  | D0  | Remark  |  |
|-----------|-----|----|-----|----|----|----|-----------------|-----|-----|---|--|
| Command   | W   | 0  | MFM | 0  | 0  | 0  | 0               | 1   | 0   | Command code  |  |
|           | W   | 0  | 0   | 0  | 0  | 0  | HDS             | DS1 | DS0 |   |  |
|           | W   |    |     |    |    |    | ----- C -----   |     |     |   | Sector ID information prior to command execution |
|           | W   |    |     |    |    |    | ----- H -----   |     |     |   |  |
|           | W   |    |     |    |    |    | ----- R -----   |     |     |   |  |
|           | W   |    |     |    |    |    | ----- N -----   |     |     |   |  |
|           | W   |    |     |    |    |    | ----- EOT ----- |     |     |   |  |
|           | W   |    |     |    |    |    | ----- GPL ----- |     |     |   |  |
|           | W   |    |     |    |    |    | ----- DTL ----- |     |     |   |  |
| Execution |     |    |     |    |    |    |                 |     |     | Data transfer between the FDD and system. FDD reads contents of all cylinders from index hole to EOT. |  |
| Result    | R   |    |     |    |    |    |                 |     |     | Status information after command execution.   |  |
|           | R   |    |     |    |    |    |                 |     |     |   |  |
|           | R   |    |     |    |    |    |                 |     |     |   |  |
|           | R   |    |     |    |    |    |                 |     |     | Sector ID information after command execution.  |  |
|           | R   |    |     |    |    |    |                 |     |     |   |  |
|           | R   |    |     |    |    |    |                 |     |     |   |  |
|           | R   |    |     |    |    |    |                 |     |     |   |  |

**Read ID**

| Phase   | R/W | D7 | D6  | D5 | D4 | D3 | D2  | D1  | D0  | Remark       |
|---------|-----|----|-----|----|----|----|-----|-----|-----|--------------|
| Command | W   | 0  | MFM | 0  | 0  | 1  | 0   | 1   | 0   | Command code |
|         | W   | 0  | 0   | 0  | 0  | 0  | HDS | DS1 | DS0 |              |

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|           |   |                 |  |
|-----------|---|-----------------|--|
| Execution |   |                 | The first correct ID information on the cylinder is stored in Data Register.                         |
| Result    | R | ----- ST0 ----- | Status information after command execution.<br><br>Disk status after the command has been completed. |
|           | R | ----- ST1 ----- |  |
|           | R | ----- ST2 ----- |  |
|           | R | ----- C -----   |  |
|           | R | ----- H -----   |  |
|           | R | ----- R -----   |  |
|           | R | ----- N -----   |  |

### Verify

| Phase     | R/W | D7 | D6  | D5 | D4 | D3 | D2  | D1  | D0  | Remark  |  |
|-----------|-----|----|-----|----|----|----|-----|-----|-----|---|--|
| Command   | W   | MT | MFM | SK | 1  | 0  | 1   | 1   | 0   | Command code  |  |
|           | W   | EC | 0   | 0  | 0  | 0  | HDS | DS1 | DS0 |   |  |
|           | W   |    |     |    |    |    |     |     |     |   | Sector ID information prior to command execution |
|           | W   |    |     |    |    |    |     |     |     |   |  |
|           | W   |    |     |    |    |    |     |     |     |   |  |
|           | W   |    |     |    |    |    |     |     |     |   |  |
|           | W   |    |     |    |    |    |     |     |     |   |  |
|           | W   |    |     |    |    |    |     |     |     |   |  |
|           | W   |    |     |    |    |    |     |     |     |   |  |
| Execution |     |    |     |    |    |    |     |     |     | No data transfer  |  |
| Result    | R   |    |     |    |    |    |     |     |     | Status information after command execution.<br><br>Sector ID information after command execution. |  |
|           | R   |    |     |    |    |    |     |     |     |   |  |
|           | R   |    |     |    |    |    |     |     |     |   |  |
|           | R   |    |     |    |    |    |     |     |     |   |  |
|           | R   |    |     |    |    |    |     |     |     |   |  |
|           | R   |    |     |    |    |    |     |     |     |   |  |
|           | R   |    |     |    |    |    |     |     |     |   |  |

### Version

| Phase   | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Remark              |
|---------|-----|----|----|----|----|----|----|----|----|---------------------|
| Command | W   | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | Command code        |
| Result  | R   | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | Enhanced controller |

**Write Data**

| Phase     | R/W | D7 | D6  | D5 | D4 | D3              | D2  | D1  | D0  | Remark  |   |
|-----------|-----|----|-----|----|----|-----------------|-----|-----|-----|---|---|
| Command   | W   | MT | MFM | 0  | 0  | 0               | 1   | 0   | 1   | Command code  |   |
|           | W   | 0  | 0   | 0  | 0  | 0               | HDS | DS1 | DS0 |   |   |
|           | W   |    |     |    |    | ----- C -----   |     |     |     |   | Sector ID<br>information prior to<br>command<br>execution |
|           | W   |    |     |    |    | ----- H -----   |     |     |     |   |   |
|           | W   |    |     |    |    | ----- R -----   |     |     |     |   |   |
|           | W   |    |     |    |    | ----- N -----   |     |     |     |   |   |
|           | W   |    |     |    |    | ----- EOT ----- |     |     |     |   |   |
|           | W   |    |     |    |    | ----- GPL ----- |     |     |     |   |   |
|           | W   |    |     |    |    | ----- DTL ----- |     |     |     |   |   |
| Execution |     |    |     |    |    |                 |     |     |     | Data transfer<br>between the FDD<br>and system.         |   |
| Result    | R   |    |     |    |    | ----- ST0 ----- |     |     |     | Status information<br>after command<br>execution.       |   |
|           | R   |    |     |    |    | ----- ST1 ----- |     |     |     |   |   |
|           | R   |    |     |    |    | ----- ST2 ----- |     |     |     |   |   |
|           | R   |    |     |    |    | ----- C -----   |     |     |     | Sector ID<br>information after<br>command<br>execution. |   |
|           | R   |    |     |    |    | ----- H -----   |     |     |     |   |   |
|           | R   |    |     |    |    | ----- R -----   |     |     |     |   |   |
|           | R   |    |     |    |    | ----- N -----   |     |     |     |   |   |

**Write Deleted Data**

| Phase     | R/W | D7 | D6  | D5 | D4 | D3              | D2  | D1  | D0  | Remark  |   |
|-----------|-----|----|-----|----|----|-----------------|-----|-----|-----|---|---|
| Command   | W   | MT | MFM | 0  | 0  | 1               | 0   | 0   | 1   | Command code                                    |   |
|           | W   | 0  | 0   | 0  | 0  | 0               | HDS | DS1 | DS0 |   |   |
|           | W   |    |     |    |    | ----- C -----   |     |     |     |   | Sector ID<br>information prior to<br>command<br>execution |
|           | W   |    |     |    |    | ----- H -----   |     |     |     |   |   |
|           | W   |    |     |    |    | ----- R -----   |     |     |     |   |   |
|           | W   |    |     |    |    | ----- N -----   |     |     |     |   |   |
|           | W   |    |     |    |    | ----- EOT ----- |     |     |     |   |   |
|           | W   |    |     |    |    | ----- GPL ----- |     |     |     |   |   |
|           | W   |    |     |    |    | ----- DTL ----- |     |     |     |   |   |
| Execution |     |    |     |    |    |                 |     |     |     | Data transfer<br>between the FDD<br>and system. |   |
| Result    | R   |    |     |    |    | ----- ST0 ----- |     |     |     | Status information<br>after command             |   |
|           | R   |    |     |    |    | ----- ST1 ----- |     |     |     |   |   |

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|   |                 |  |
|---|-----------------|--|
| R | ----- ST2 ----- | execution.<br><br>Sector ID information after command execution. |
| R | ----- C -----   |  |
| R | ----- H -----   |  |
| R | ----- R -----   |  |
| R | ----- N -----   |  |

**Format A Track**

| Phase                              | R/W | D7 | D6  | D5 | D4 | D3 | D2  | D1  | D0  | Remark                                      |
|------------------------------------|-----|----|-----|----|----|----|-----|-----|-----|---|
| Command                            | W   | 0  | MFM | 0  | 0  | 1  | 1   | 0   | 1   | Command code                                |
|                                    | W   | 0  | 0   | 0  | 0  | 0  | HDS | DS1 | DS0 |   |
|                                    | W   |    |     |    |    |    |     |     |     | Bytes/Sector                                |
|                                    | W   |    |     |    |    |    |     |     |     | Sectors/Cylinder                            |
|                                    | W   |    |     |    |    |    |     |     |     | Gap 3 Length                                |
|                                    | W   |    |     |    |    |    |     |     |     |   |
| Execution for each sector (repeat) |     |    |     |    |    |    |     |     |     | Input sector parameter.                     |
|                                    | W   |    |     |    |    |    |     |     |     |   |
|                                    | W   |    |     |    |    |    |     |     |     |   |
|                                    | W   |    |     |    |    |    |     |     |     |   |
| Result                             | R   |    |     |    |    |    |     |     |     | Status information after command execution. |
|                                    | R   |    |     |    |    |    |     |     |     |   |
|                                    | R   |    |     |    |    |    |     |     |     |   |
|                                    | R   |    |     |    |    |    |     |     |     |   |
|                                    | R   |    |     |    |    |    |     |     |     |   |
|                                    | R   |    |     |    |    |    |     |     |     |   |

**Recalibrate**

| Phase     | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1  | D0  | Remark                    |
|-----------|-----|----|----|----|----|----|----|-----|-----|---------------------------|
| Command   | W   | 0  | 0  | 0  | 0  | 0  | 1  | 1   | 1   | Command code              |
|           | W   | 0  | 0  | 0  | 0  | 0  | 0  | DS1 | DS0 |                           |
| Execution |     |    |    |    |    |    |    |     |     | Head retracted to track 0 |

**Sense Interrupt Status**

| Phase   | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Remark       |
|---------|-----|----|----|----|----|----|----|----|----|--------------|
| Command | W   | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | Command code |
| Result  | R   |    |    |    |    |    |    |    |    |              |
|         | R   |    |    |    |    |    |    |    |    |              |

**Specify**

| Phase   | R/W | D7              | D6 | D5 | D4 | D3              | D2 | D1 | D0 | Remark       |
|---------|-----|-----------------|----|----|----|-----------------|----|----|----|--------------|
| Command | W   | 0               | 0  | 0  | 0  | 0               | 0  | 1  | 1  | Command code |
|         | W   | ----- SRT ----- |    |    |    | ----- HUT ----- |    |    |    |              |
|         | W   | ----- SRT ----- |    |    |    |                 |    |    | ND |              |

**Seek**

| Phase     | R/W | D7              | D6 | D5 | D4 | D3 | D2  | D1  | D0  | Remark   |
|-----------|-----|-----------------|----|----|----|----|-----|-----|-----|--|
| Command   | W   | 0               | 0  | 0  | 0  | 1  | 1   | 1   | 1   | Command code                                     |
|           | W   | 0               | 0  | 0  | 0  | 0  | HDS | DS1 | DS0 |  |
|           | W   | ----- NCN ----- |    |    |    |    |     |     |     |  |
| Execution |     |                 |    |    |    |    |     |     |     | Head positioned over proper cylinder on diskette |

**Configure**

| Phase     | R/W | D7                 | D6  | D5    | D4   | D3                  | D2  | D1  | D0  | Remark                     |
|-----------|-----|--------------------|-----|-------|------|---------------------|-----|-----|-----|----------------------------|
| Command   | W   | 0                  | 0   | 0     | 1    | 0                   | 0   | 1   | 1   | Command code               |
|           | W   | 0                  | 0   | 0     | 0    | 0                   | HDS | DS1 | DS0 |                            |
|           | W   | 0                  | EIS | EFIFO | POLL | ----- FIFOTHR ----- |     |     |     |                            |
|           | W   | ----- PRETRK ----- |     |       |      |                     |     |     |     |                            |
| Execution |     |                    |     |       |      |                     |     |     |     | Internal registers written |

**Relative Seek**

| Phase   | R/W | D7              | D6  | D5 | D4 | D3 | D2  | D1  | D0  | Remark       |
|---------|-----|-----------------|-----|----|----|----|-----|-----|-----|--------------|
| Command | W   | 1               | DIR | 0  | 0  | 1  | 1   | 1   | 1   | Command code |
|         | W   | 0               | 0   | 0  | 0  | 0  | HDS | DS1 | DS0 |              |
|         | W   | ----- RCN ----- |     |    |    |    |     |     |     |              |

**Perpendicular Mode**

| Phase   | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1  | D0    | Remark       |
|---------|-----|----|----|----|----|----|----|-----|-------|--------------|
| Command | W   | 0  | 0  | 0  | 1  | 0  | 0  | 1   | 0     | Command code |
|         | W   | OW | 0  | D3 | D2 | D1 | D0 | GAP | WGATE |              |

**Lock**

| Phase   | R/W | D7   | D6 | D5 | D4   | D3 | D2 | D1 | D0 | Remark       |
|---------|-----|------|----|----|------|----|----|----|----|--------------|
| Command | W   | LOCK | 0  | 0  | 1    | 0  | 1  | 0  | 0  | Command code |
| Result  | R   | 0    | 0  | 0  | LOCK | 0  | 0  | 0  | 0  |              |

**Dumpreg**

| Phase   | R/W                | D7                          | D6  | D5    | D4   | D3                  | D2 | D1  | D0    | Remark       |
|---------|--------------------|-----------------------------|-----|-------|------|---------------------|----|-----|-------|--------------|
| Command | W                  | 0                           | 0   | 0     | 0    | 1                   | 1  | 1   | 0     | Command code |
| Result  | R                  | ----- PCN ( Drive 0 ) ----- |     |       |      |                     |    |     |       |              |
|         | R                  | ----- PCN ( Drive 0 ) ----- |     |       |      |                     |    |     |       |              |
|         | R                  | ----- PCN ( Drive 0 ) ----- |     |       |      |                     |    |     |       |              |
|         | R                  | ----- PCN ( Drive 0 ) ----- |     |       |      |                     |    |     |       |              |
|         | R                  | ----- SRT -----             |     |       |      | ----- HUT -----     |    |     |       |              |
|         | R                  | ----- SRT -----  ND         |     |       |      |                     |    |     |       |              |
|         | R                  | ----- SC/EOT -----          |     |       |      |                     |    |     |       |              |
|         | R                  | LOCK                        | 0   | D3    | D2   | D1                  | D0 | GAP | WGATE |              |
|         | R                  | 0                           | EIS | EFIFO | POLL | ----- FIFOTHR ----- |    |     |       |              |
| R       | ----- PRETRK ----- |                             |     |       |      |                     |    |     |       |              |

**Sense Drive Status**

| Phase   | R/W | D7              | D6 | D5 | D4 | D3 | D2  | D1  | D0  | Remark                              |
|---------|-----|-----------------|----|----|----|----|-----|-----|-----|-------------------------------------|
| Command | W   | 0               | 0  | 0  | 0  | 0  | 1   | 0   | 0   | Command code                        |
|         | W   | 0               | 0  | 0  | 0  | 0  | HDS | DS1 | DS0 |                                     |
| Result  | R   | ----- ST3 ----- |    |    |    |    |     |     |     | Status information about disk drive |

**Invalid**

| Phase   | R/W | D7                        | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Remark                     |
|---------|-----|---------------------------|----|----|----|----|----|----|----|----------------------------|
| Command | W   | ----- Invalid Codes ----- |    |    |    |    |    |    |    | FDC goes to standby state. |
| Result  | R   | ----- ST0 -----           |    |    |    |    |    |    |    | ST0 = 80h                  |

## 7.3 UART

The F71863 provides two UART ports and supports IRQ sharing for system application. The UARTs are used to convert data between parallel format and serial format. They convert parallel data into serial format on transmission and serial format into parallel data on receiver side. The serial format is formed by one start bit, followed by five to eight data bits, a parity bit if programmed and one ( 1.5 or 2 ) stop bits. The UARTs include complete modem control capability and an interrupt system that may be software trailed to the computing time required to handle the communication link. They have FIFO mode to reduce the number of interrupts presented to the host. Both receiver and transmitter have a



16-byte FIFO.

The below content is about the UART1 and UART2 device register descriptions. All the registers are for software porting reference.

**Receiver Buffer Register — Base + 0**

| Bit | Name | R/W | Default | Description                                      |
|-----|------|-----|---------|--|
| 7-0 | RBR  | R   | 00h     | The data received.<br>Read only when LCR[7] is 0 |

**Transmitter Holding Register — Base + 0**

| Bit | Name | R/W | Default | Description  |
|-----|------|-----|---------|--|
| 7-0 | THR  | W   | 00h     | Data to be transmitted.<br>Write only when LCR[7] is 0 |

**Divisor Latch (LSB) — Base + 0**

| Bit | Name | R/W | Default | Description   |
|-----|------|-----|---------|---|
| 7-0 | DLL  | R/W | 01h     | Baud generator divisor low byte.<br>Access only when LCR[7] is 1. |

**Divisor Latch (MSB) — Base + 1**

| Bit | Name | R/W | Default | Description  |
|-----|------|-----|---------|--|
| 7-0 | DLM  | R/W | 00h     | Baud generator divisor high byte.<br>Access only when LCR[7] is 1. |

**Interrupt Enable Register — Base + 1**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-4 | Reserved | -   | -       | Reserved.  |
| 3   | EDSSI    | R/W | 0       | Enable Modem Status Interrupt. Access only when LCR[7] is 0.                       |
| 2   | ELSI     | R/W | 0       | Enable Line Status Error Interrupt. Access only when LCR[7] is 0.                  |
| 1   | ETBFI    | R/W | 0       | Enable Transmitter Holding Register Empty Interrupt. Access only when LCR[7] is 0. |
| 0   | ERBFI    | R/W | 0       | Enable Received Data Available Interrupt. Access only when LCR[7] is 0.            |

**Interrupt Identification Register — Base + 2**

| Bit | Name     | R/W | Default | Description                                |
|-----|----------|-----|---------|--|
| 7   | FIFO_EN  | R   | 0       | 0: FIFO is disabled<br>1: FIFO is enabled. |
| 6   | FIFO_EN  | R   | 0       | 0: FIFO is disabled<br>1: FIFO is enabled. |
| 5-4 | Reserved | -   | -       | Reserved.                                  |

|     |           |   |     |   |
|-----|-----------|---|-----|---|
| 3-1 | IRQ_ID    | R | 000 | 000: Interrupt is caused by Modem Status<br>001: Interrupt is caused by Transmitter Holding Register Empty<br>010: Interrupt is caused by Received Data Available.<br>110: Interrupt is caused by Character Timeout<br>011: Interrupt is caused by Line Status. |
| 0   | IRQ_PENDN | R | 1   | 1: Interrupt is not pending.<br>0: Interrupt is pending.  |

**FIFO Control Register — Base + 2**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-6 | RCV_TRIG | W   | 00      | 00: Receiver FIFO trigger level is 1.<br>01: Receiver FIFO trigger level is 4.<br>10: Receiver FIFO trigger level is 8.<br>11: Receiver FIFO trigger level is 14. |
| 5-3 | Reserved | -   | -       | Reserved.   |
| 2   | CLRTX    | R   | 0       | Reset the transmitter FIFO.   |
| 1   | CLRRX    | R   | 0       | Reset the receiver FIFO.  |
| 0   | FIFO_EN  | R   | 0       | 0: Disable FIFO.<br>1: Enable FIFO.   |

**Line Control Register — Base + 3**

| Bit | Name   | R/W | Default | Description  |
|-----|--------|-----|---------|--|
| 7   | DLAB   | R/W | 0       | 0: Divisor Latch can't be accessed.<br>1: Divisor Latch can be accessed via Base and Base+1.                 |
| 6   | SETBRK | R/W | 0       | 0: Transmitter is in normal condition.<br>1: Transmit a break condition.                                     |
| 5   | STKPAR | R/W | 0       | XX0: Parity Bit is disable   |
| 4   | EPS    | R/W | 0       | 001: Parity Bit is odd.  |
| 3   | PEN    | R/W | 0       | 011: Parity Bit is even<br>101: Parity Bit is logic 1<br>111: Parity Bit is logic 0                          |
| 2   | STB    | R/W | 0       | 0: Stop bit is one bit<br>1: When word length is 5 bit stop bit is 1.5 bit<br>else stop bit is 2 bit         |
| 1-0 | WLS    | R/W | 00      | 00: Word length is 5 bit<br>01: Word length is 6 bit<br>10: Word length is 7 bit<br>11: Word length is 8 bit |

**MODEM Control Register — Base + 4**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-5 | Reserved | -   | -       | Reserved.   |
| 4   | LOOP     | R/W | 0       | 0: UART in normal condition.<br>1: UART is internal loop back               |
| 3   | OUT2     | R/W | 0       | 0: All interrupt is disabled.<br>1: Interrupt is enabled (disabled) by IER. |
| 2   | OUT1     | R/W | 0       | Read from MSR[6] is loop back mode  |
| 1   | RTS      | R/W | 0       | 0: RTS# is forced to logic 1<br>1: RTS# is forced to logic 0                |

|   |     |     |   |  |
|---|-----|-----|---|--|
| 0 | DTR | R/W | 0 | 0: DTR# is forced to logic 1<br>1: DTR# is forced to logic 0 |
|---|-----|-----|---|--|

**Line Status Register — Base + 5**

| Bit | Name    | R/W | Default | Description  |
|-----|---------|-----|---------|--|
| 7   | RCR_ERR | R   | 0       | 0: No error in the FIFO when FIFO is enabled<br>1: Error in the FIFO when FIFO is enabled. |
| 6   | TEMT    | R   | 1       | 0: Transmitter is in transmitting.<br>1: Transmitter is empty.                             |
| 5   | THRE    | R   | 1       | 0: Transmitter Holding Register is not empty.<br>1: Transmitter Holding Register is empty. |
| 4   | BI      | R   | 0       | 0: No break condition detected.<br>1: A break condition is detected.                       |
| 3   | FE      | R   | 0       | 0: Data received has no frame error.<br>1: Data received has frame error.                  |
| 2   | PE      | R   | 0       | 0: Data received has no parity error.<br>1: Data received has parity error.                |
| 1   | OE      | R   | 0       | 0: No overrun condition occurred.<br>1: An overrun condition occurred.                     |
| 0   | DR      | R   | 0       | 0: No data is ready for read.<br>1: Data is received.                                      |

**MODEM Status Register — Base + 6**

| Bit | Name | R/W | Default | Description   |
|-----|------|-----|---------|---|
| 7   | DCD  | R   | -       | Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR. |
| 6   | RI   | R   | -       | Complement of RI# input. In loop back mode, this bit is equivalent to OUT1 in MCR   |
| 5   | DSR  | R   | -       | Complement of DSR# input. In loop back mode, this bit is equivalent to DTR in MCR   |
| 4   | CTS  | R   | -       | Complement of CTS# input. In loop back mode, this bit is equivalent to RTS in MCR   |
| 3   | DDCD | R   | 0       | 0: No state changed at DCD#.<br>1: State changed at DCD#.                           |
| 2   | TERI | R   | 0       | 0: No Trailing edge at RI#.<br>1: A low to high transition at RI#.                  |
| 1   | DDSR | R   | 0       | 0: No state changed at DSR#.<br>1: State changed at DSR#.                           |
| 0   | DCTS | R   | 0       | 0: No state changed at CTS#.<br>1: State changed at CTS#.                           |

**Scratch Register — Base + 7**

| Bit | Name | R/W | Default | Description       |
|-----|------|-----|---------|-------------------|
| 7-0 | SCR  | R/W | 00h     | Scratch register. |

## 7.4 Parallel Port

The parallel port in F71863 supports an IBM XT/AT compatible parallel port ( SPP ), bi-directional parallel port ( BPP ), Enhanced Parallel Port ( EPP ), Extended Capabilities Parallel Port ( ECP ) mode. Refer to the configuration registers for more information on selecting the mode of operation.

The below content is about the Parallel Port device register descriptions. All the registers are for software porting reference.

### Parallel Port Data Register — Base + 0

| Bit | Name | R/W | Default | Description  |
|-----|------|-----|---------|--|
| 7-0 | DATA | R/W | 00h     | The output data to drive the parallel port data lines. |

### ECP Address FIFO Register — Base + 0

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-0 | ECP_AFIFO | R/W | 00h     | Access only in ECP Parallel Port Mode and the ECP_MODE programmed in the Extended Control Register is 011.<br>The data written to this register is placed in the FIFO and tagged as an Address/RLE. It is auto transmitted by the hardware. The operation is only defined for forward direction. It divide into two parts :<br>Bit 7 :<br>0: bits 6-0 are run length, indicating how many times the next byte to appear (0 = 1time, 1 = 2times, 2 = 3times and so on).<br>1: bits 6-0 are a ECP address.<br>Bit 6-0 :<br>Address or RLE depends on bit 7. |

### Device Status Register — Base + 1

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7   | BUSY_N   | R   | -       | Inverted version of parallel port signal BUSY.  |
| 6   | ACK_N    | R   | -       | Version of parallel port signal ACK#.   |
| 5   | PERROR   | R   | -       | Version of parallel port signal PE.   |
| 4   | SELECT   | R   | -       | Version of parallel port signal SLCT.   |
| 3   | ERR_N    | R   | -       | Version of parallel port signal ERR#.   |
| 2-1 | Reserved | R   | 11      | Reserved. Return 11b when read.   |
| 0   | TMOUT    | R   | -       | This bit is valid only in EPP mode. Return 1 when in other modes.<br>It indicates that a 10uS time out has occurred on the EPP bus.<br>0: no time out error.<br>1: time out error occurred, write 1 to clear. |

**Device Control Register — Base + 2**

| Bit | Name      | R/W | Default | Description  |
|-----|-----------|-----|---------|--|
| 7-6 | Reserved  | -   | 11      | Reserved. Return 11b when read.  |
| 5   | DIR       | R/W | 0       | 0: the parallel port is in output mode.<br>1: the parallel port is in input mode.<br>It is auto reset to 0 when in SPP mode. |
| 4   | ACKIRQ_EN | R/W | 0       | Enable an interrupt at the rising edge of ACK#.  |
| 3   | SLIN      | R/W | 0       | Inverted and then drives the parallel port signal SLIN#.<br>When read, the status of inverted SLIN# is return.               |
| 2   | INIT_N    | R/W | 0       | Drives the parallel port signal INIT#.<br>When read, the status of INIT# is return.  |
| 1   | AFD       | R/W | 0       | Inverted and then drives the parallel port signal AFD#.<br>When read, the status of inverted AFD# is return.                 |
| 0   | STB       | R/W | 0       | Inverted and then drives the parallel port signal STB#.<br>When read, the status of inverted STB# is return.                 |

**EPP Address Register — Base + 3**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-0 | EPP_ADDR | R/W | 00h     | Write this register will cause the hardware to auto transmit the written data to the device with the EPP Address Write protocol.<br>Read this register will cause the hardware to auto receive data from the device by with the EPP Address Read protocol. |

**EPP Data Register — Base + 4 – Base + 7**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-0 | EPP_DATA | R/W | 00h     | Write this register will cause the hardware to auto transmit the written data to the device with the EPP Data Write protocol.<br>Read this register will cause the hardware to auto receive data from the device by with the EPP Data Read protocol. |

**Parallel Port Data FIFO — Base + 400h**

| Bit | Name   | R/W | Default | Description   |
|-----|--------|-----|---------|---|
| 7-0 | C_FIFO | R/W | 00h     | Data written to this FIFO is auto transmitted by the hardware to the device by using standard parallel port protocol.<br>It is only valid in ECP and the ECP_MODE is 010b. The operation is only for forward direction. |

**ECP Data FIFO — Base + 400h**

| Bit | Name | R/W | Default | Description |
|-----|------|-----|---------|-------------|
|-----|------|-----|---------|-------------|

|     |           |     |     |   |
|-----|-----------|-----|-----|---|
| 7-0 | ECP_DFIFO | R/W | 00h | <p>Data written to this FIFO when DIR is 0 is auto transmitted by the hardware to the device by using ECP parallel port protocol.</p> <p>Data is auto read from device into the FIFO when DIR is 1 by the hardware by using ECP parallel port protocol. Read the FIFO will return the content to the system.</p> <p>It is only valid in ECP and the ECP_MODE is 011b.</p> |
|-----|-----------|-----|-----|---|

**ECP Test FIFO — Base + 400h**

| Bit | Name   | R/W | Default | Description  |
|-----|--------|-----|---------|--|
| 7-0 | T_FIFO | R/W | 00h     | <p>Data may be read, written from system to the FIFO in any Direction. But no hardware handshake occurred on the parallel port lines. It could be used to test the empty, full and threshold of the FIFO.</p> <p>It is only valid in ECP and the ECP_MODE is 110b.</p> |

**ECP Configuration Register A — Base + 400h**

| Bit | Name       | R/W | Default | Description  |
|-----|------------|-----|---------|--|
| 7   | IRQ_MODE   | R   | 0       | <p>0: interrupt is ISA pulse.</p> <p>1: interrupt is ISA level.</p> <p>Only valid in ECP and ECP_MODE is 111b.</p>   |
| 6-4 | IMPID      | R   | 001     | <p>000: the design is 16-bit implementation.</p> <p>001: the design is 8-bit implementation (default).</p> <p>010: the design is 32-bit implementation.</p> <p>011-111: Reserved.</p> <p>Only valid in ECP and ECP_MODE is 111b.</p>                           |
| 3   | Reserved   | -   | -       | Reserved.  |
| 2   | BYTETRAN_N | R   | 1       | <p>0: when transmitting there is 1 byte waiting in the transceiver that does not affect the FIFO full condition.</p> <p>1: when transmitting the state of the full bit includes the byte being transmitted.</p> <p>Only valid in ECP and ECP_MODE is 111b.</p> |
| 1-0 | Reserved   | R   | 00      | <p>Return 00 when read.</p> <p>Only valid in ECP and ECP_MODE is 111b.</p>   |

**ECP Configuration Register B — Base + 401h**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7   | COMP     | R   | 0       | <p>0: only send uncompressed data.</p> <p>1: compress data before sending.</p> <p>Only valid in ECP and ECP_MODE is 111b.</p> |
| 6   | Reserved | R   | 1       | <p>Reserved. Return 1 when read.</p> <p>Only valid in ECP and ECP_MODE is 111b.</p>   |

|     |            |   |     |   |
|-----|------------|---|-----|---|
| 5-3 | ECP_IRQ_CH | R | 001 | 000: the interrupt selected with jumper.<br>001: select IRQ 7 (default).<br>010: select IRQ 9.<br>011: select IRQ 10.<br>100: select IRQ 11.<br>101: select IRQ 14.<br>110: select IRQ 15.<br>111: select IRQ 5.<br>Only valid in ECP and ECP_MODE is 111b. |
| 2-0 | ECP_DMA_CH | R | 011 | Return the DMA channel of ECP parallel port.<br>Only valid in ECP and ECP_MODE is 111b.   |

**Extended Control Register — Base + 402h**

| Bit | Name        | R/W | Default | Description   |
|-----|-------------|-----|---------|---|
| 7-5 | ECP_MODE    | R/W | 000     | 000: SPP Mode.<br>001: PS/2 Parallel Port Mode.<br>010: Parallel Port Data FIFO Mode.<br>011: ECP Parallel Port Mode.<br>100: EPP Mode.<br>101: Reserved.<br>110: Test Mode.<br>111: Configuration Mode.<br>Only valid in ECP.  |
| 4   | ERRINTR_EN  | R/W | 0       | 0: disable the interrupt generated on the falling edge of ERR#.<br>1: enable the interrupt generated on the falling edge of ERR#.   |
| 3   | DAMEN       | R/W | 0       | 0: disable DMA.<br>1: enable DMA. DMA starts when SERVICEINTR is 0.   |
| 2   | SERVICEINTR | R/W | 1       | 0: enable the following case of interrupt.<br>DMAEN = 1: DMA mode.<br>DMAEN = 0, DIR = 0: set to 1 whenever there are writeIntrThreshold or more bytes are free in the FIFO.<br>DMAEN = 0, DIR = 0: set to 1 whenever there are readIntrThreshold or more bytes are valid to be read in the FIFO. |
| 1   | FIFOFULL    | R   | 0       | 0: The FIFO has at least 1 free byte.<br>1: The FIFO is completely full.  |
| 0   | FIFOEMPTY   | R   | 0       | 0: The FIFO contains at least 1 byte.<br>1: The FIFO is completely empty.   |

## 7.5 Keyboard Controller

The KBC circuit provides the functions included a keyboard and/or a PS/2 mouse, and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

## Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60H. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system.

## Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60H or 64H. Writing to address 60H sets a flag to indicate a data write; writing to address 64H sets a flag to indicate a command write. Data written to I/O address 60H is sent to keyboard through the controller's input buffer only if the input buffer full bit in the status register is "0".

## Status Register

The status register is an 8-bit read-only register at I/O address 64H, that holds information about the status of the keyboard controller and interface. It may be read at any time.

| BIT | BIT FUNCTION             | DESCRIPTION   |
|-----|--------------------------|---|
| 0   | Output Buffer Full       | 0: Output buffer empty<br>1: Output buffer full   |
| 1   | Input Buffer Full        | 0: Input buffer empty<br>1: Input buffer full   |
| 2   | System Flag              | This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller (KCCB). It defaults to 0 after a power-on reset. |
| 3   | Command/Data             | 0: Data byte<br>1: Command byte   |
| 4   | Inhibit Switch           | 0: Keyboard is inhibited<br>1: Keyboard is not inhibited  |
| 5   | Mouse Output Buffer      | 0: Mouse output buffer empty<br>1: Mouse output buffer full   |
| 6   | General Purpose Time-out | 0: No time-out error<br>1: Time-out error   |
| 7   | Parity Error             | 0: Odd parity<br>1: Even parity (error)   |

## Commands

| COMMAND | FUNCTION          |
|---------|-------------------|
| 20h     | Read Command Byte |



| 60h | Write Command Byte   |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
|-----|--|----------------------------|-------------|---|---------------------------|---|------------------------|---|-------------|---|---------|---|----------------------------|---|-------------------------|---|-----------------------------|---|---------|
|     | <table border="1"> <thead> <tr> <th>BIT</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Enable Keyboard Interrupt</td> </tr> <tr> <td>1</td> <td>Enable Mouse Interrupt</td> </tr> <tr> <td>2</td> <td>System flag</td> </tr> <tr> <td>3</td> <td>Reserve</td> </tr> <tr> <td>4</td> <td>Disable Keyboard Interface</td> </tr> <tr> <td>5</td> <td>Disable Mouse interface</td> </tr> <tr> <td>6</td> <td>IBM keyboard Translate Mode</td> </tr> <tr> <td>7</td> <td>Reserve</td> </tr> </tbody> </table> | BIT                        | DESCRIPTION | 0 | Enable Keyboard Interrupt | 1 | Enable Mouse Interrupt | 2 | System flag | 3 | Reserve | 4 | Disable Keyboard Interface | 5 | Disable Mouse interface | 6 | IBM keyboard Translate Mode | 7 | Reserve |
|     | BIT  | DESCRIPTION                |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
|     | 0  | Enable Keyboard Interrupt  |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
|     | 1  | Enable Mouse Interrupt     |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
|     | 2  | System flag                |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
|     | 3  | Reserve                    |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
|     | 4  | Disable Keyboard Interface |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
|     | 5  | Disable Mouse interface    |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| 6   | IBM keyboard Translate Mode  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| 7   | Reserve  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| A7h | Disable Auxiliary Device Interface   |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| A8h | Enable Auxiliary Device Interface  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| A9h | Auxiliary Interface Test<br>8'h00: indicate Auxiliary interface is ok.<br>8'h01: indicate Auxiliary clock is low.<br>8'h02: indicate Auxiliary clock is high<br>8'h03: indicate Auxiliary data is low<br>8'h04: indicate Auxiliary data is high  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| AAh | Self-test<br>Returns 055h if self test succeeds  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| ABh | keyboard Interface Test<br>8'h00: indicate keyboard interface is ok.<br>8'h01: indicate keyboard clock is low.<br>8'h02: indicate keyboard clock is high<br>8'h03: indicate keyboard data is low<br>8'h04: indicate keyboard data is high  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| ADh | Disable Keyboard Interface   |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| AEh | Enable Keyboard Interface  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| C0h | Read Input Port(P1) and send data to the system  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| C1h | Continuously puts the lower four bits of Port1 into STATUS register  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| C2h | Continuously puts the upper four bits of Port1 into STATUS register  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| D0h | Send Port2 value to the system   |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| D1h | Only set/reset GateA20 line based on the system data bit 1   |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| D2h | Send data back to the system as if it came from Keyboard   |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| D3h | Send data back to the system as if it came from Muse   |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| D4h | Output next received byte of data from system to Mouse   |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |
| FEh | Pulse only RC(the reset line) low for 6 $\mu$ S if Command byte is even  |                            |             |   |                           |   |                        |   |             |   |         |   |                            |   |                         |   |                             |   |         |

**KBC Command Description**

## PS2 wakeup function

The KBC supports keyboard and mouse wakeup function, keyboard wakeup function has 4 kinds of conditions, when key is pressed combinational key (1) CTRL +ESC (2) CTRL+F1 (3) CTRL+SPACE (4) ANY KEY (5) windows 98 wakeup up key, KBC will assert PME signal. Mouse wakeup function has 2 kinds of conditions, when mouse (1) BUTTON CLICK or (2) BUTTON CLICK AND MOVEMENT, KBC will assert PME signal. Those wakeup conditions are controlled by configuration register.

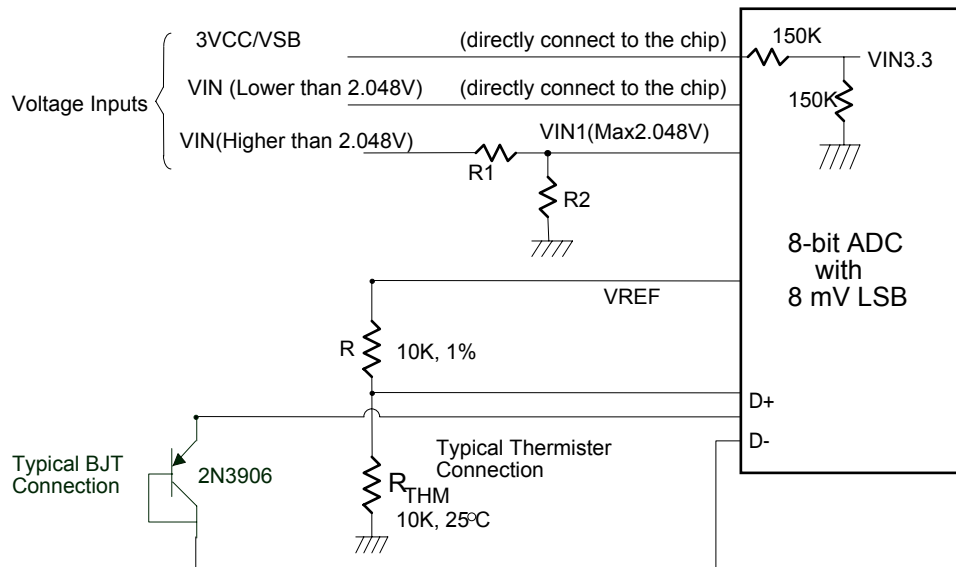
## 7.6 Hardware Monitor

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.048V. Therefore the voltage under 2.048V (ex:1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3VCC/VSB/VBAT is an exception for it is main power of the F71863. Therefore 3VCC/VSB/VBAT can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F71863 and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V.

There are four voltage inputs in the F71863 and the voltage divided formula is shown as follows:

$$V_{IN} = V_{+12V} \times \frac{R_2}{R_1 + R_2} \quad \text{where } V_{+12V} \text{ is the analog input voltage, for example.}$$

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.


**Fig 7-1**

The F71863 monitors three remote temperature sensors. These sensors can be measured from  $-40^{\circ}\text{C}$  to  $127^{\circ}\text{C}$ . More detail please refer register description.

#### Remote-sensor transistor manufacturers

| Manufacturer | Model Number   |
|--------------|----------------|
| Panasonic    | 2SB0709 2N3906 |
| Philips      | PMBT3906       |

#### Monitor Temperature from “thermistor”

The F71863 can connect three thermistor to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1)  $\beta$  value is 3435K (2) resistor value is 10K ohm at  $25^{\circ}\text{C}$ . In the Figure 7-1, the thermistor is connected by a serial resistor with 10K ohm, then connected to VREF.

#### Monitor Temperature from “thermal diode”

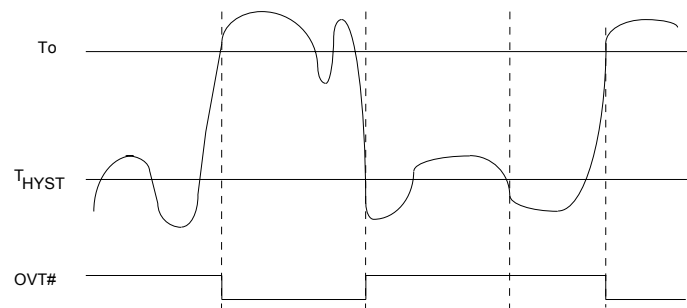
Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F71863 is capable to these situations. The build-in reference table is for PNP 2N3906 transistor. In the Figure 7-1, the transistor is directly connected into temperature pins.

## ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

## Over Temperature Signal (OVT#)

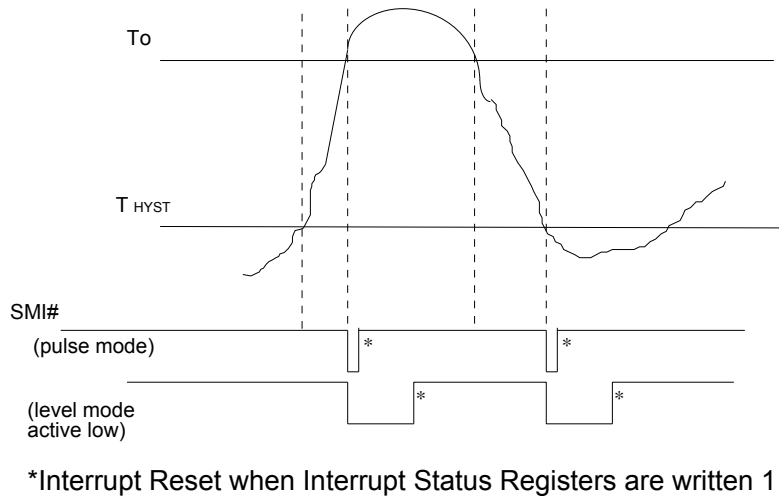
OVT# alert for temperature is shown as figure 7-2. When monitored temperature exceeds the over-temperature threshold value, OVT# will be asserted until the temperature goes below the hysteresis temperature.



**Fig 7-2**

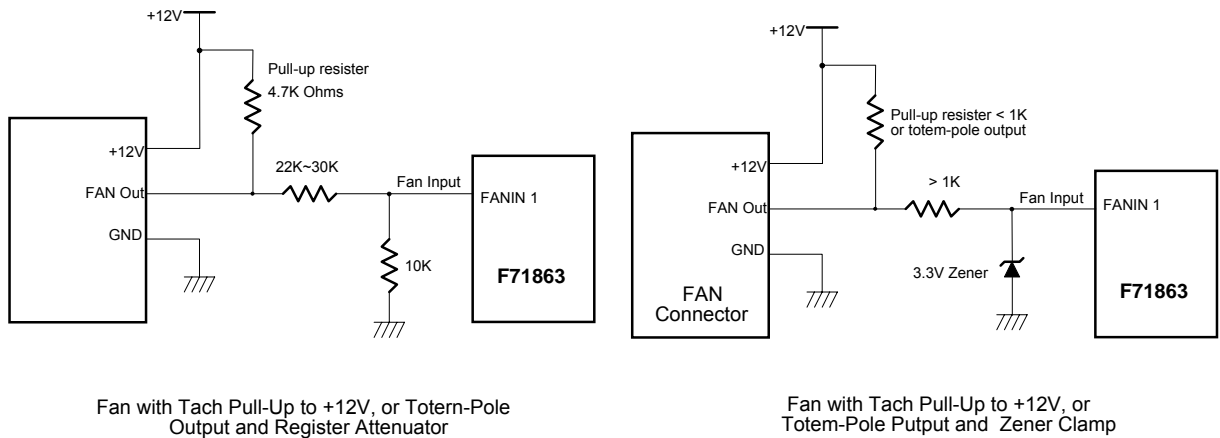
## Temperature PME#

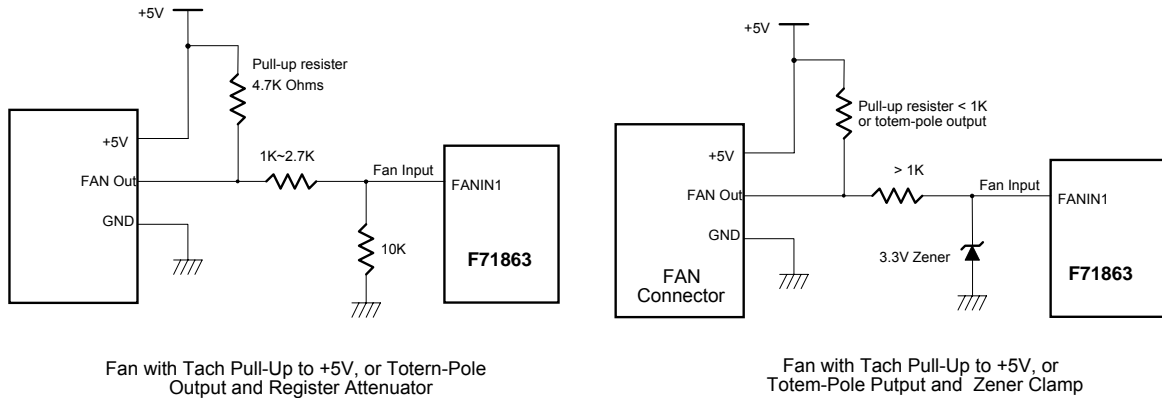
PME# interrupt for temperature is shown as figure 7-3. Temperature exceeding high limit or going below hysteresis will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.


**Fig 7-3**

### Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as follows:


**Fig 7-4 / 7-5**


**Fig 7-6 / 7-7**

Determine the fan counter according to:

$$Count = \frac{1.5 \times 10^6}{RPM}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by the following equation. As for fan, it would be best to use 2 pulses tachometer output per round.

$$RPM = \frac{1.5 \times 10^6}{Count}$$

### Fan speed control

The F71863 provides 2 fan speed control methods:

1. DAC FAN CONTROL
2. PWM DUTY CYCLE

### DAC Fan Control

The range of DC output is 0~3.3V, controlled by 8-bit register. 1 LSB is about 0.013V. The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$Output\_voltage (V) = 3.3 \times \frac{\text{Programmed 8bit Register Value}}{255}$$

And the suggested application circuit for linear fan control would be:

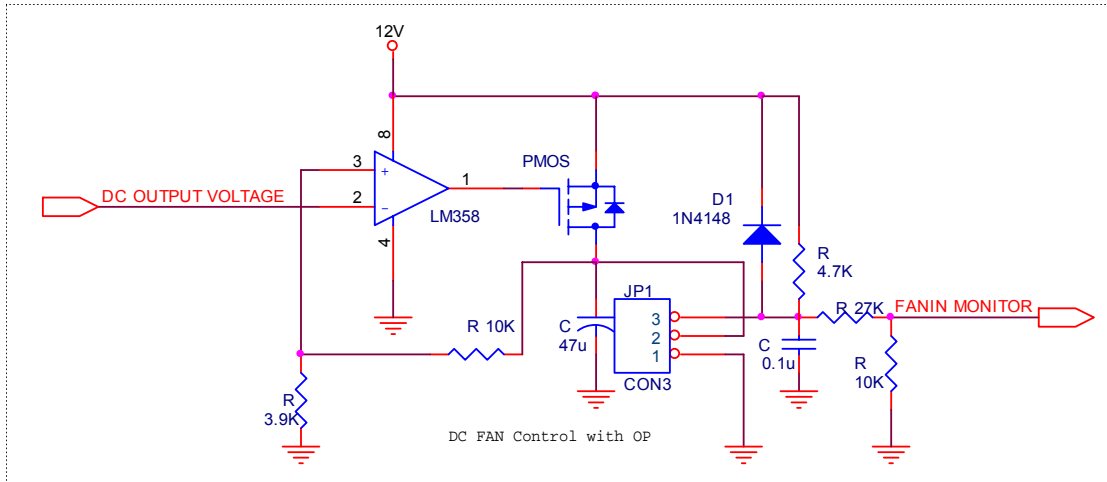


Fig 7-8

**PWM duty Fan Control**

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty\_cycle(\%)} = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

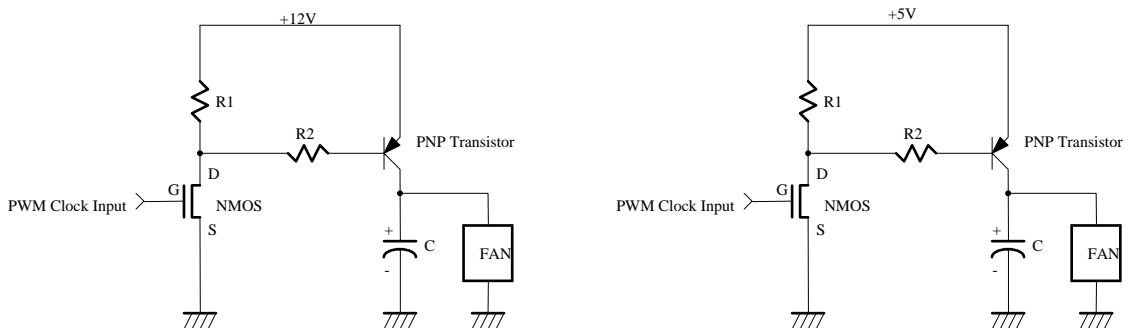


Fig 7-9

**Fan speed control mechanism**

There are some modes to control fan speed and they are 1. Manual mode, 2. Stage auto mode, 3. Linear auto mode. More detail, please refer the description of registers.

**Manual mode**

For manual mode, it generally acts as software fan speed control.

**Stage auto mode**

At this mode, the F71863 provides automatic fan speed control related to temperature

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variation of CPU/GPU or the system. The F71863 can provide two temperature boundaries and three intervals, and each interval has its related fan speed PWM duty. All these values should be set by BIOS first. Take figure 7-10 as example. When temperature boundaries are set as 45 and 75°C and there are three intervals. The related desired fan speed for each interval are 40%, 80% and 100% (fixed). When the temperature is within 45~75°C, the fan speed will follow 80% PWM duty and that define in registers. It can be said that the fan will be turned on with a specific speed set by BIOS and automatically controlled with the temperature variation. The F71863 will take charge of all the fan speed control and need no software support.

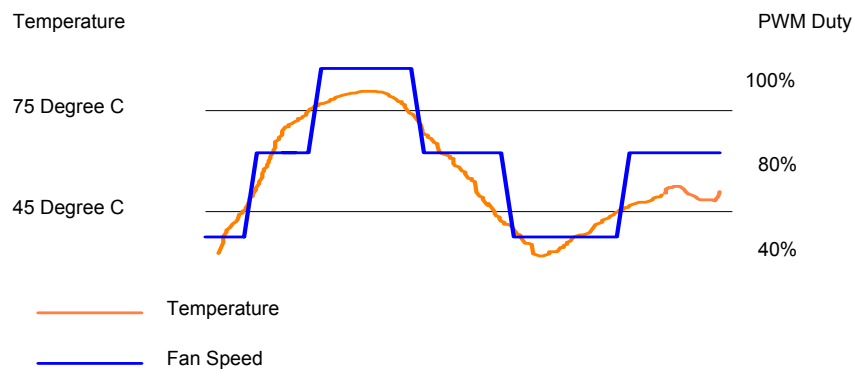
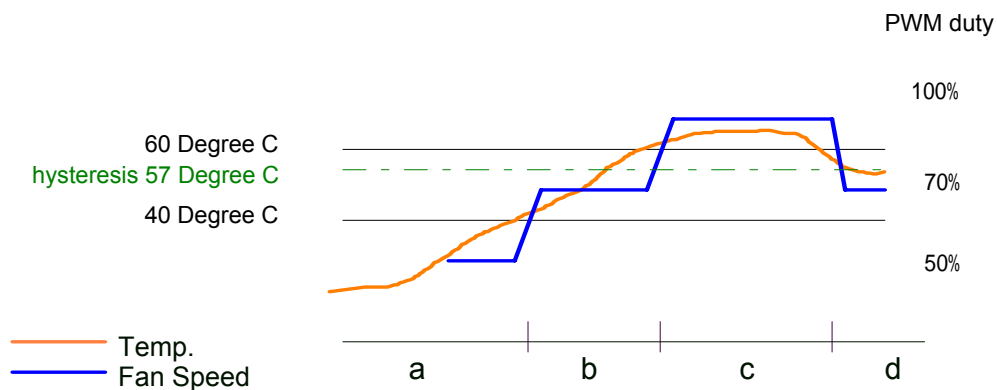


Figure 7-10

Below is a sample for Stage auto mode:

Set temperature as 60°C, 40°C and Duty as 100%, 70%, 50%



- Once temp. is under 40°C, the lowest fan speed keeps 50% PWM duty
- Once temp. is over 40°C, 60°C, the fan speed will vary from 70% to 100% PWM duty and increase with temp. level.
- Once temp. keeps in 55°C, fan speed keeps in 70% PWM duty
- If set the hysteresis as 3°C (default 4°C), once temp reduces under 57°C, fan speed reduces to 70% PWM duty and stays there.

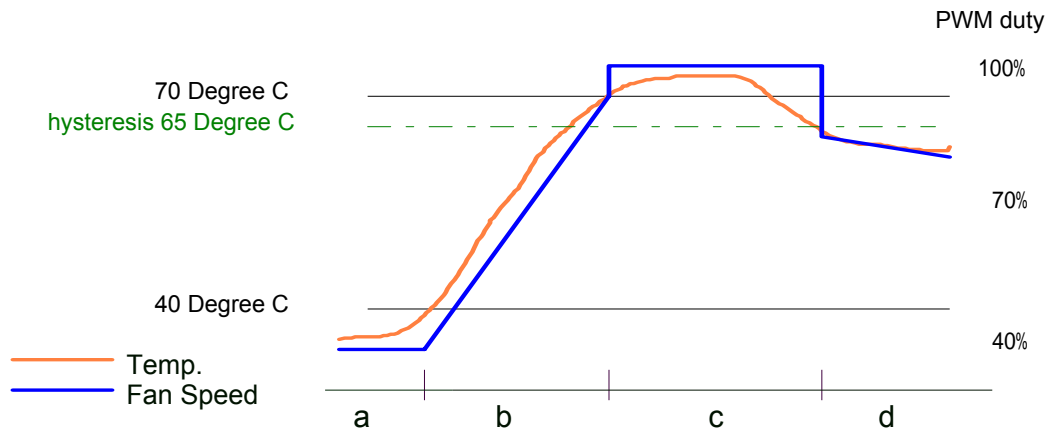


## Linear auto mode

Otherwise, F71863 supports linear auto mode. Below has a example to describe this mode. More detail, please refer the register description.

### A. Linear auto mode (PWM Duty I)

Set temperature as 70°C, 40°C and Duty as 100%, 70%, 40%

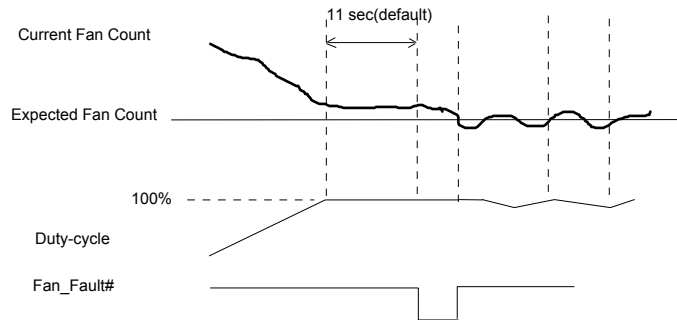


- Once temp. is under 40°C, the lowest fan speed keeps 40% PWM duty
- Once temp. is over 40°C and under 70°C, the fan speed will vary from 40% to 70% PWM duty and linearly increase with temp. variation. The temp.-fan speed monitoring and flash interval is 1sec.
- Once temp. goes over 70°C, fan speed will directly increase to 100% PWM duty (full speed)
- If set the hysteresis as 5°C(default is 4°C), once temp reduces under 65°C (not 70°C), fan speed reduces from 100% PWM duty and decrease linearly with temp..

## FAN\_FAULT#

Fan\_Fault# will be asserted when the fan speed doesn't meet the expected fan speed within a programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN\_FAULT# event.

(1). When PWM\_Duty reaches 0xFF, the fan speed count can't reach the fan expected count in time. (Figure 7-11)


**Fig 7-11**

(2). After the period of detecting fan full speed, when PWM\_Duty > Min. Duty, and fan count still in 0xFFF.

## 7.7 SPI Interface

Communication between the two devices is handling the serial peripheral interface (SPI). Every SPI system consist of one master and one or more slaves, where a master provides the SPI clock and slave receives clock from the master.

This design is only master function, for basic signal, master-out/slave-in (MOSI), master-in/slave-out (MISO), serial clock (SCK), and 4 slaves select (SS), are needed for SPI interface. Each of slave select supports from 512kbits to 4096kbits flash is decided by configuration register. Serial clock (SCK) signal frequency is varied from 24MHz to 187.5 KHz. The serial data (MOSI) for SPI interface translates to depend on SCK rising edge or falling edge is decided by configuration register.

## 7.8 ACPI Function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

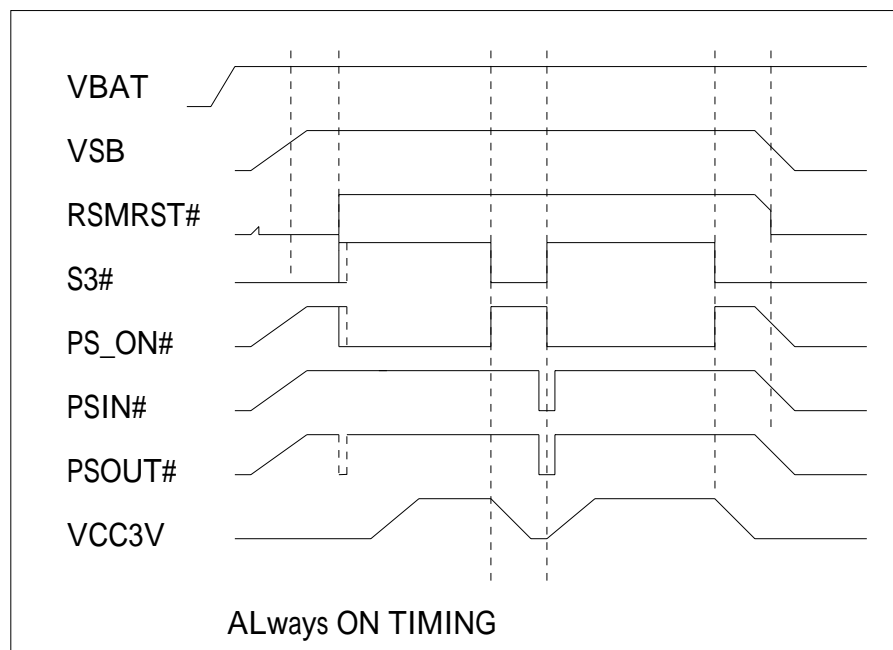
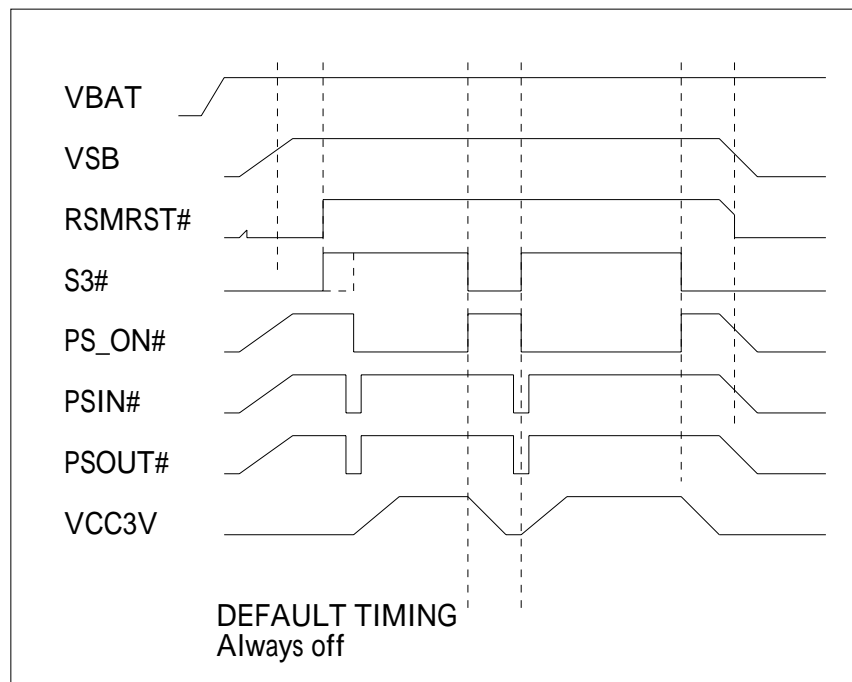
It is anticipated that only the following state transitions may happen:

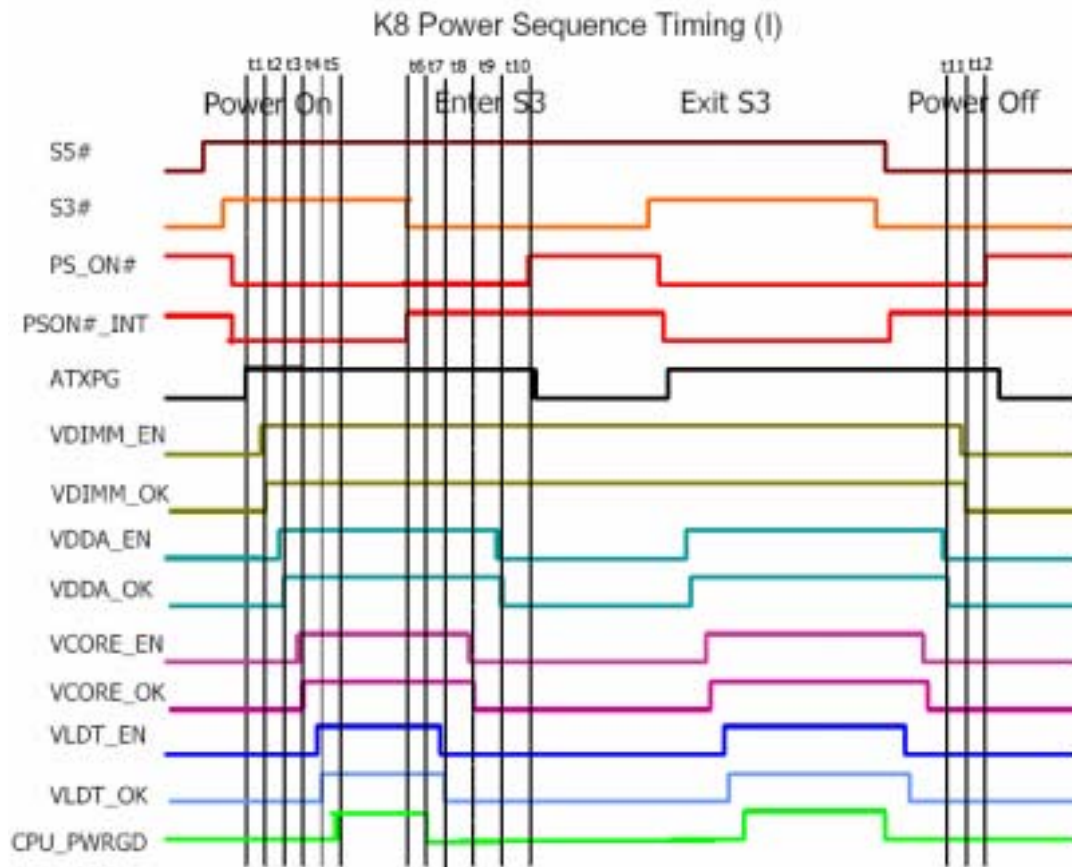
S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5.

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Among them, S3→S5 is illegal transition and won't be allowed by state machine. It is necessary to enter S0 first in order to get to S5 from S3. As for transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

The below diagram described the timing, the always on and always off, keep last state could be set in control register. In keep last state mode, one register will keep the status of before power loss. If it is power on before power loss, it will remain power on when power is resumed, otherwise, if it is power off before power loss, it will remain power off when power is resumed.



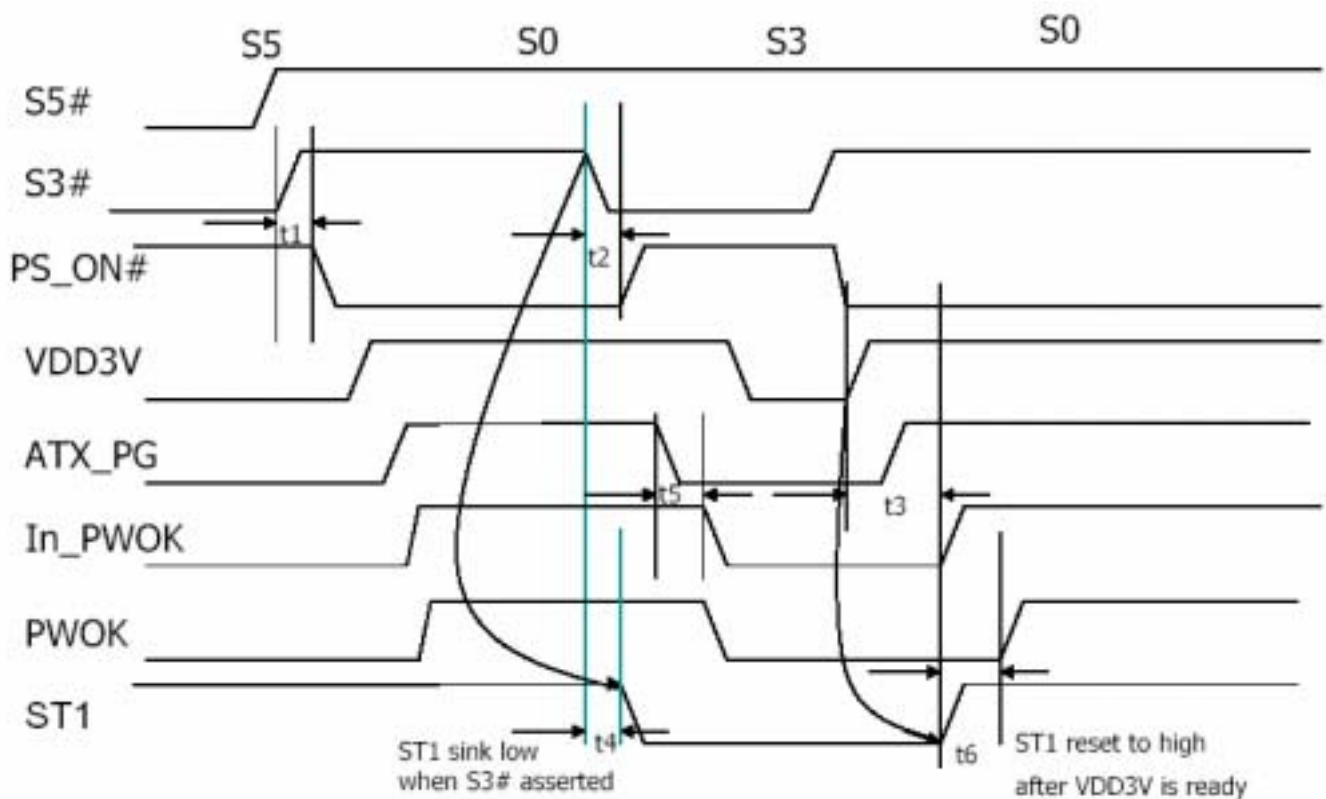
**K8 Power Sequence Timing diagram**

**K8 Power Sequence Timing (II)**

|     | Description                | Max | Typ  | Min |
|-----|----------------------------|-----|------|-----|
| t1  | ATXPG ↑ to VDIMM_EN ↑      | 1ms |      |     |
| t2  | VDIMM_OK ↑ to VDDA_EN ↑    | 1ms |      |     |
| t3  | VDDA_OK ↑ to VCORE_EN ↑    | 1ms |      |     |
| t4  | VCORE_OK ↑ to VLDT_EN ↑    | 1ms |      |     |
| t5  | VLDT_OK ↑ to CPU_PWRGD ↑   |     | 3ms  |     |
| t6  | PSON#_INT ↑ to CPU_PWRGD ↓ | 1ms |      |     |
| t7  | CPU_PWRGD ↓ to VLDT_EN ↓   | 1ms |      |     |
| t8  | VLDT_OK ↓ to VCORE_EN ↓    |     | 10ms |     |
| t9  | VCORE_OK ↓ to VDDA_EN ↓    |     | 10ms |     |
| t10 | VDDA_OK ↓ to PS_ON# ↑      |     | 10ms |     |
| t11 | VDDA_OK ↓ to VDIMM_EN ↓    |     | 4ms  |     |
| t12 | VDIMM_OK ↓ to PS_ON# ↑     |     | 10ms |     |

**ST1/ST2 Pins Timing diagram:**
**ST1/ST2 Timing (I)**

| pin \ State | S0  | S3  | S5   |
|-------------|-----|-----|------|
| STATUS1     | Tri | Low | Tri  |
| STATUS2     | Tri | Low | Low* |

Remark: STATUS2 will be tri-state in S5 if PME CRF7[1] set to one

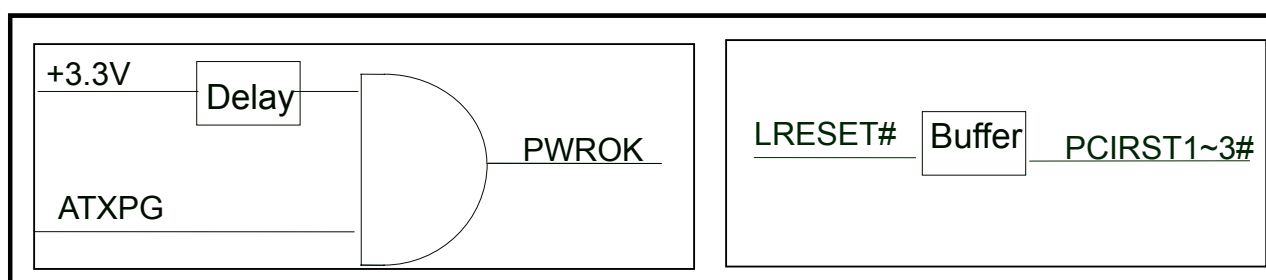
**ST1/ST2 Timing (II)**


### ST1/ST2 Timing (III)

| SYMBOL | PARAMETER                            | MIN | MAX | UNIT |
|--------|--------------------------------------|-----|-----|------|
| t1     | S3# inactive to PS_ON# active        | 8   | 12  | us   |
| t2     | S3# active to PS_ON# inactive        | 8   | 12  | us   |
| t3     | PS_ON#(VCC3V) active to ST1 inactive | 380 | 420 | ms   |
| t4     | ATXPG inactive to ST1 active         | 8   | 12  | us   |
| t5     | ATXPG inactive to PWOK inactive      | 8   | 12  | us   |
| t6     | ST1 inactive to PWOK active          | 1.2 | 2.2 | ms   |

### PCI Reset and PWROK Signals

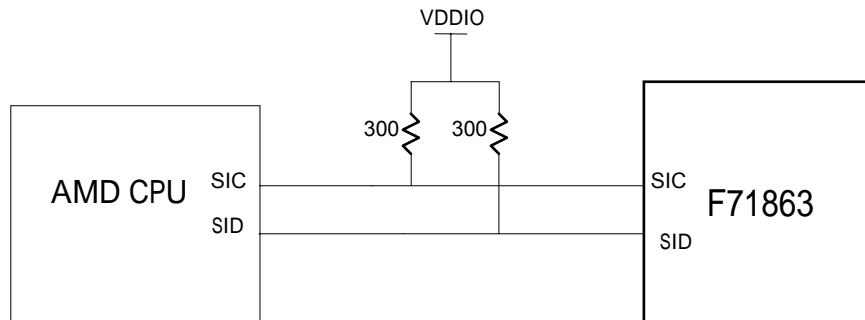
The F71863 supports 3 output buffers for 3 reset signals.



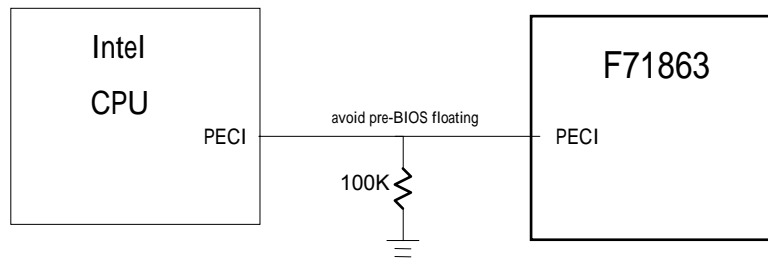
So far as the PWROK issue is as the figure above. PWROK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed by register. (100ms ~ 400ms)

## 7.9 AMDSI and Intel PECI Function

The F71863 provides Intel PECI/AMDSI interfaces for new generational CPU temperature sensing. In AMDSI interface, there are SIC and SID signals for temperature information reading from AMD CPU. The SIC signal is for clocking use, the other is for data transferring. More detail please refer register description.



In Intel PECE interface, the F71863 can connect to CPU directly. The F71863 can read the temperature data from CPU, than the fan control machine of F71863 can implement the Fan to cool down CPU temperature. The application circuit is as below. More detail please refer the register description.



## 8. Register Description

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT1 pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

- o 4e 87
- o 4e 87           ( enable configuration )
- o 4e aa           ( disable configuration )

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer each device chapter if you want more detail information.

### Global Control Registers

“-“ Reserved or Tri-State

| Global Control Registers |                                    |               |     |     |     |     |     |     |     |
|--------------------------|------------------------------------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Register 0x[HEX]         | Register Name                      | Default Value |     |     |     |     |     |     |     |
|                          |                                    | MSB           |     |     |     |     |     |     | LSB |
| 02                       | Software Reset Register            | -             | -   | -   | -   | -   | -   | -   | 0   |
| 07                       | Logic Device Number Register (LDN) | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 20                       | Chip ID Register                   | 0             | 0   | 0   | 0   | 0   | 1   | 1   | 0   |
| 21                       | Chip ID Register                   | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| 23                       | Vender ID Register                 | 0             | 0   | 0   | 1   | 1   | 0   | 0   | 1   |
| 24                       | Vender ID Register                 | 0             | 0   | 1   | 1   | 0   | 1   | 0   | 0   |
| 25                       | Software Power Down Register       | -             | -   | 0   | 0   | 0   | 0   | 0   | 0   |
| 26                       | UART IRQ Sharing Register          | 0             | -   | -   | -   | -   | -   | 0   | 0   |
| 27                       | ROM Address Select Register        | 0             | 0/1 | 1/0 | 1/0 | 0/1 | 0/1 | 0/1 | 0   |
| 28                       | Power LED Function Select Register | -             | -   | -   | -   | 0   | 0   | 0   | 0   |
| 29                       | Multi Function Select 1 Register   | -             | 0   | 0   | 0   | -   | 0   | 0   | 0   |
| 2A                       | Multi Function Select 2 Register   | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 2B                       | Multi Function Select 3 Register   | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 2C                       | Multi Function Select 4 Register   | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 2D                       | Wakeup Control Register            | 0             | -   | -   | -   | 1   | 0   | 0   | 0   |



Device Configuration Registers

“-“ Reserved or Tri-State

| FDC Device Configuration Registers (LDN CR00) |                             |               |   |   |   |   |   |     |   |
|---|-----------------------------|---------------|---|---|---|---|---|-----|---|
| Register<br>0x[HEX]                           | Register Name               | Default Value |   |   |   |   |   |     |   |
|   |                             | MSB           |   |   |   |   |   | LSB |   |
| 30  | FDC Device Enable Register  | -             | - | - | - | - | - | -   | 1 |
| 60  | Base Address High Register  | 0             | 0 | 0 | 0 | 0 | 0 | 1   | 1 |
| 61  | Base Address Low Register   | 1             | 1 | 1 | 1 | 0 | 0 | 0   | 0 |
| 70  | IRQ Channel Select Register | -             | - | - | - | 0 | 1 | 1   | 0 |
| 74  | DMA Channel Select Register | -             | - | - | - | - | 0 | 1   | 0 |
| F0  | FDD Mode Register           | -             | - | - | - | 1 | 1 | 1   | 0 |
| F2  | FDD Drive Type Register     | -             | - | - | - | - | - | 1   | 1 |
| F4  | FDD Selection Register      | -             | - | - | 0 | 0 | - | 0   | 0 |

| UART1 Device Configuration Registers (LDN CR01) |                              |               |   |   |   |   |   |     |   |
|---|------------------------------|---------------|---|---|---|---|---|-----|---|
| Register<br>0x[HEX]                             | Register Name                | Default Value |   |   |   |   |   |     |   |
|   |                              | MSB           |   |   |   |   |   | LSB |   |
| 30  | UART1 Device Enable Register | -             | - | - | - | - | - | -   | 1 |
| 60  | Base Address High Register   | 0             | 0 | 0 | 0 | 0 | 0 | 1   | 1 |
| 61  | Base Address Low Register    | 1             | 1 | 1 | 1 | 1 | 0 | 0   | 0 |
| 70  | IRQ Channel Select Register  | -             | - | - | - | 0 | 1 | 0   | 0 |
| F0  | RS485 Enable Register        | -             | - | - | 0 | - | - | -   | - |

| UART2 Device Configuration Registers (LDN CR02) |                              |               |   |   |   |   |   |     |   |
|---|------------------------------|---------------|---|---|---|---|---|-----|---|
| Register<br>0x[HEX]                             | Register Name                | Default Value |   |   |   |   |   |     |   |
|   |                              | MSB           |   |   |   |   |   | LSB |   |
| 30  | UART2 Device Enable Register | -             | - | - | - | - | - | -   | 1 |
| 60  | Base Address High Register   | 0             | 0 | 0 | 0 | 0 | 0 | 1   | 0 |
| 61  | Base Address Low Register    | 1             | 1 | 1 | 1 | 1 | 0 | 0   | 0 |
| 70  | IRQ Channel Select Register  | -             | - | - | - | 0 | 0 | 1   | 1 |
| F0  | RS485 Enable Register        | -             | - | - | 0 | 0 | 0 | -   | - |
| F1  | SIR Mode Control Register    | -             | - | - | 0 | 0 | 1 | 0   | 0 |

| Parallel Port Device Configuration Registers (LDN CR03) |                                      |               |   |   |   |   |   |     |   |
|---|--------------------------------------|---------------|---|---|---|---|---|-----|---|
| Register<br>0x[HEX]                                     | Register Name                        | Default Value |   |   |   |   |   |     |   |
|   |                                      | MSB           |   |   |   |   |   | LSB |   |
| 30  | Parallel Port Device Enable Register | -             | - | - | - | - | - | -   | 1 |
| 60  | Base Address High Register           | 0             | 0 | 0 | 0 | 0 | 0 | 1   | 1 |
| 61  | Base Address Low Register            | 0             | 1 | 1 | 1 | 1 | 0 | 0   | 0 |
| 70  | IRQ Channel Select Register          | -             | - | - | - | 0 | 1 | 1   | 1 |
| 74  | DMA Channel Select Register          | -             | - | - | 0 | - | 0 | 1   | 1 |

| F0  | PRT Mode Select Register           | 0             | 1 | 0 | 0 | 0   | 0 | 1 | 0 |
|---|------------------------------------|---------------|---|---|---|-----|---|---|---|
| <b>Hardware Monitor Device Configuration Registers (LDN CR04)</b> |                                    |               |   |   |   |     |   |   |   |
| Register<br>0x[HEX]   | Register Name                      | Default Value |   |   |   |     |   |   |   |
|   |                                    | MSB           |   |   |   | LSB |   |   |   |
| 30  | H/W Monitor Device Enable Register | -             | - | - | - | -   | - | - | 1 |
| 60  | Base Address High Register         | 0             | 0 | 0 | 0 | 0   | 0 | 1 | 0 |
| 61  | Base Address Low Register          | 1             | 0 | 0 | 1 | 0   | 1 | 0 | 1 |
| 70  | IRQ Channel Select Register        | -             | - | - | - | 0   | 0 | 0 | 0 |
| <b>KBC Device Configuration Registers (LDN CR05)</b>              |                                    |               |   |   |   |     |   |   |   |
| Register<br>0x[HEX]   | Register Name                      | Default Value |   |   |   |     |   |   |   |
|   |                                    | MSB           |   |   |   | LSB |   |   |   |
| 30  | KBC Device Enable Register         | -             | - | - | - | -   | - | - | 1 |
| 60  | Base Address High Register         | 0             | 0 | 0 | 0 | 0   | 0 | 0 | 0 |
| 61  | Base Address Low Register          | 0             | 1 | 1 | 0 | 0   | 0 | 0 | 0 |
| 70  | KB IRQ Channel Select Register     | -             | - | - | - | 0   | 0 | 0 | 0 |
| 72  | Mouse IRQ Channel Select Register  | -             | - | - | - | 0   | 0 | 0 | 0 |
| <b>GPIO Device Configuration Registers (LDN CR06)</b>             |                                    |               |   |   |   |     |   |   |   |
| Register<br>0x[HEX]   | Register Name                      | Default Value |   |   |   |     |   |   |   |
|   |                                    | MSB           |   |   |   | LSB |   |   |   |
| F0  | GPIO Output Enable Register        | -             | - | - | - | 0   | 0 | 0 | 0 |
| F1  | GPIO Output Data Register          | -             | - | - | - | 1   | 1 | 1 | 1 |
| F2  | GPIO Pin Status Register           | -             | - | - | - | -   | - | - | - |
| F3  | GPIO Drive Enable Register         | 0             | 0 | 0 | 0 | 0   | 0 | 0 | 0 |
| E0  | GPIO1 Output Enable Register       | 0             | 0 | 0 | 0 | 0   | 0 | 0 | 0 |
| E1  | GPIO1 Output Data Register         | 1             | 1 | 1 | 1 | 1   | 1 | 1 | 1 |
| E2  | GPIO1 Pin Status Register          | -             | - | - | - | -   | - | - | - |
| E3  | GPIO1 Drive Enable Register        | 0             | 0 | 0 | 0 | 0   | 0 | 0 | 0 |
| D0  | GPIO2 Output Enable Register       | 0             | 0 | 0 | 0 | 0   | 0 | 0 | 0 |
| D1  | GPIO2 Output Data Register         | 1             | 1 | 1 | 1 | 1   | 1 | 1 | 1 |
| D2  | GPIO2 Pin Status Register          | -             | - | - | - | -   | - | - | - |
| D3  | GPIO2 Drive Enable Register        | 0             | 0 | 0 | 0 | 0   | 0 | 0 | 0 |
| C0  | GPIO3 Output Enable Register       | -             | - | - | - | 0   | 0 | 0 | 0 |
| C1  | GPIO3 Output Data Register         | -             | - | - | - | 1   | 1 | 1 | 1 |
| C2  | GPIO3 Pin Status Register          | -             | - | - | - | -   | - | - | - |
| C3  | GPIO3 Drive Enable Register        | -             | - | - | - | 0   | 0 | 0 | 0 |
| B0  | GPIO4 Output Enable Register       | -             | - | 0 | 0 | 0   | 0 | 0 | 0 |
| B1  | GPIO4 Output Data Register         | -             | - | 1 | 1 | 1   | 1 | 1 | 1 |
| B2  | GPIO4 Pin Status Register          | -             | - | - | - | -   | - | - | - |
| B3  | GPIO4 Drive Enable Register        | -             | - | 0 | 0 | 0   | 0 | 0 | 0 |

| VID Device Configuration Registers (LDN CR07)          |                                  |               |   |   |   |   |   |     |   |
|--|----------------------------------|---------------|---|---|---|---|---|-----|---|
| Register<br>0x[HEX]                                    | Register Name                    | Default Value |   |   |   |   |   |     |   |
|  |                                  | MSB           |   |   |   |   |   | LSB |   |
| 30   | VID Device Enable Register       | -             | - | - | - | - | - | -   | 0 |
| 60   | Base Address High Register       | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| 61   | Base Address Low Register        | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| SPI Device Configuration Registers (LDN CR08)          |                                  |               |   |   |   |   |   |     |   |
| Register<br>0x[HEX]                                    | Register Name                    | Default Value |   |   |   |   |   |     |   |
|  |                                  | MSB           |   |   |   |   |   | LSB |   |
| F0   | SPI Control Register             | 0             | 0 | 0 | 1 | 0 | 0 | 0   | 0 |
| F1   | SPI Timeout Value Register       | 0             | 0 | 0 | 0 | 0 | 1 | 0   | 0 |
| F2   | SPI Baud Rate Divisor Register   | -             | - | - | - | - | 0 | 0   | 1 |
| F3   | SPI Status Register              | 0             | - | - | - | 0 | - | -   | - |
| F4   | SPI High Byte Data Register      | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| F5   | SPI Command Data Register        | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| F6   | SPI Chip Select Register         | -             | - | - | - | 0 | 0 | 0   | 0 |
| F7   | SPI Memory Mapping Register      | -             | - | - | - | - | - | -   | - |
| F8   | SPI Operate Register             | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| FA   | SPI Low Byte Data Register       | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| FB   | SPI Address High Byte Register   | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| FC   | SPI Address Medium Byte Register | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| FD   | SPI Address Low Byte Register    | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| FE   | SPI Program Byte Register        | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| FF   | SPI Write Data Register          | 0             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| PME and ACPI Device Configuration Registers (LDN CR0A) |                                  |               |   |   |   |   |   |     |   |
| Register<br>0x[HEX]                                    | Register Name                    | Default Value |   |   |   |   |   |     |   |
|  |                                  | MSB           |   |   |   |   |   | LSB |   |
| 30   | PME Device Enable Register       | -             | - | - | - | - | - | -   | 0 |
| F0   | PME Event Enable Register        | -             | 0 | 0 | 0 | 0 | 0 | 0   | 0 |
| F1   | PME Event Status Register        | -             | - | - | - | - | - | -   | - |
| F4   | ACPI Control Register            | 0             | 0 | 0 | 0 | 0 | 1 | 1   | 0 |
| F5   | ACPI Control Register            | 0             | 0 | 0 | 1 | 1 | 1 | 0   | 0 |

## 8.1 Global Control Registers

### 8.1.1 Software Reset Register — Index 02h

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-1 | Reserved | -   | -       | Reserved   |
| 0   | SOFT_RST | R/W | 0       | Write 1 to reset the register and device powered by VDD ( VCC ). |

### 8.1.2 Logic Device Number Register (LDN) — Index 07h

| Bit | Name | R/W | Default | Description   |
|-----|------|-----|---------|---|
| 7-0 | LDN  | R/W | 00h     | 00h: Select FDC device configuration registers.<br>01h: Select UART 1 device configuration registers.<br>02h: Select UART 2 device configuration registers.<br>03h: Select Parallel Port device configuration registers.<br>04h: Select Hardware Monitor device configuration registers.<br>05h: Select KBC device configuration registers.<br>06h: Select GPIO device configuration registers.<br>07h: Select VID device configuration registers.<br>08h: Select SPI device configuration registers.<br>0ah: Select PME & ACPI device configuration registers. |

### 8.1.3 Chip ID Register — Index 20h

| Bit | Name     | R/W | Default | Description            |
|-----|----------|-----|---------|------------------------|
| 7-0 | CHIP_ID1 | R   | 06h     | Chip ID 1 of F71863FG. |

### 8.1.4 Chip ID Register — Index 21h

| Bit | Name     | R/W | Default | Description           |
|-----|----------|-----|---------|-----------------------|
| 7-0 | CHIP_ID2 | R   | 01h     | Chip ID2 of F71863FG. |

### 8.1.5 Vendor ID Register — Index 23h

| Bit | Name       | R/W | Default | Description                    |
|-----|------------|-----|---------|--------------------------------|
| 7-0 | VENDOR_ID1 | R   | 19h     | Vendor ID 1 of Fintek devices. |

### 8.1.6 Vendor ID Register — Index 24h

| Bit | Name       | R/W | Default | Description                    |
|-----|------------|-----|---------|--------------------------------|
| 7-0 | VENDOR_ID2 | R   | 34h     | Vendor ID 2 of Fintek devices. |

### 8.1.7 Software Power Down Register — Index 25h

| Bit | Name     | R/W | Default | Description     |
|-----|----------|-----|---------|-----------------|
| 7-6 | Reserved | -   | -       | Reserved        |
| 5   | Reserved | R/W | 0       | Dummy register. |

|   |            |     |   |  |
|---|------------|-----|---|--|
| 4 | SOFTPD_HM  | R/W | 0 | Power down the Hardware Monitor device. This will stop the Hardware Monitor clock. |
| 3 | SOFTPD_PRT | R/W | 0 | Power down the Parallel Port device. This will stop the Parallel Port clock.       |
| 2 | SOFTPD_UR2 | R/W | 0 | Power down the UART 2 device. This will stop the UART 2 clock.                     |
| 1 | SOFTPD_UR1 | R/W | 0 | Power down the UART 1 device. This will stop the UART 1 clock.                     |
| 0 | SOFTPD_FDC | R/W | 0 | Power down the FDC device. This will stop the FDC clock.                           |

**8.1.8 UART IRQ Sharing Register — Index 26h**

| Bit | Name       | R/W | Default | Description   |
|-----|------------|-----|---------|---|
| 7   | CLK24M_SEL | R/W | 0       | 0: CLKIN is 48MHz<br>1: CLKIN is 24MHz  |
| 6-2 | Reserved   | -   | -       | Reserved.   |
| 1   | IRQ_MODE   | R/W | 0       | 0: PCI IRQ sharing mode (low level).<br>1: ISA IRQ sharing mode (low pulse).              |
| 0   | IRQ_SHAR   | R/W | 0       | 0: disable IRQ sharing of two UART devices.<br>1: enable IRQ sharing of two UART devices. |

**8.1.9 ROM Address Select Register — Index 27h**

| Bit | Name        | R/W | Default | Description   |
|-----|-------------|-----|---------|---|
| 7   | ROM_WR_EN   | R/W | 0       | 0: disable ROM writing<br>1: enable ROM writing   |
| 6   | SPI_EN      | R/W | -       | 0: SPI disable<br>1: SPI enable<br>This register is power on trapped by SOUT2/SPI_TRAP. Pull down to enable SPI.  |
| 5   | SPI_BIOS_EN | R/W | -       | 0: use SPI bridge for BIOS<br>1: Reserved<br>This register is power on trapped by DTR2#/FWH_TRAP. Pull down to enable SPI bridge for BIOS.  |
| 4   | PORT_4E_EN  | R/W | -       | 0: The configuration register port is 2E/2F.<br>1: The configuration register port is 4E/4F.<br>This register is power on trapped by SOUT1/ Config4E_2E. Pull down to select port 2E/2F.  |
| 3   | SEG_000E_EN | R/W | -       | 0: disable address 0x000E0000 – 0x000EFFFF decode<br>1: enable address 0x000E0000 – 0x000EFFFF decode<br>This register is power on trapped by SOUT2/SPI_DIS. Pull down to enable.   |
| 2   | SEG_FFF8_EN | R/W | -       | 0: disable address 0xFFFF80000 – 0xFFFFFFFF and 0x000F0000 – 0x000FFFFFF decode<br>1: enable address 0xFFFF80000 – 0xFFFFFFFF and 0x000F0000 – 0x000FFFFFF decode<br>This register is power on trapped by SOUT2/SPI_DIS. Pull down to enable. |

|   |             |     |   |   |
|---|-------------|-----|---|---|
| 1 | SEG_FFEF_EN | R/W | - | 0: disable address 0xFFEE – 0xFFEFFFFFF decode<br>1: enable address 0xFFEE0000 – 0xFFEFFFFFF decode<br>This register is power on trapped by SOUT2/SPI_DIS. Pull down to enable. |
| 0 | SEG_FFF0_EN | R/W | 0 | 0: disable address 0xFFFF0000 – 0xFFFF7FFF decode<br>1: enable address 0xFFFF0000 – 0xFFFF7FFF decode   |

**8.1.10 Power LED Function Select Register — Index 28h**

| Bit | Name       | R/W | Default | Description  |
|-----|------------|-----|---------|--|
| 7-4 | Reserved   | -   | -       | Reserved.  |
| 3   | GPIO43_SEL | R/W | 0       | 0: IRRX/GPIO43 functions as IRRX.<br>1: IRRX/GPIO43 functions as GPIO43.             |
| 2   | GPIO42_SEL | R/W | 0       | 0: IRTX/GPIO42 functions as IRTX.<br>1: IRTX/GPIO42 functions as GPIO42.             |
| 1   | GPIO41_SEL | R/W | 0       | 0: FANCTRL3/GPIO41 functions as FANCTRL3.<br>1: FANCTRL3/GPIO41 functions as GPIO41. |
| 0   | GPIO40_SEL | R/W | 0       | 0: FANIN3/GPIO40 functions as FANIN3.<br>1: FANIN3/GPIO40 functions as GPIO40.       |

**8.1.11 Multi Function Select 1 Register — Index 29h (Powered by VSB3V)**

| Bit | Name         | R/W | Default | Description  |
|-----|--------------|-----|---------|--|
| 7   | Reserved     | R/W | -       | Reserved   |
| 6   | FDD_PROT_STS | R/W | 0       | 0: FDD write-protect status depends on PIN18(WPT#)<br>1: FDD is write-protected  |
| 5   | LEC_VCC_PRO  | R/W | 0       | 0: LED_VCC (PIN65) is tri-state if VCC power loss<br>1: LED_VCC (PIN65) is still programmable while VCC power loss                               |
| 4   | KB_MO_SWP    | R/W | 0       | 0: KB/MOUSE signal as default.<br>1: KB/MOUSE signal swapped.  |
| 3   | Reserved     | R/W | -       | Reserved   |
| 2   | GPIO02_SEL   | R/W | 0       | 0: SLOTOCC#/GPIO02 will functions as SLOTOCC#.<br>1: SLOTOCC#/GPIO02 will functions as GPIO02.   |
| 1   | WDT_GP03_EN  | R/W | 0       | 0: GPIO03/WDTRST# will function as GPIO03<br>1: GPIO03/WDTRST# will function as WDTRST#.   |
| 0   | ALERT_GP_EN  | R/W | 0       | 0: GPIO15/LED_VSB/ALERT# will function as GPIO15/LED_VSB controlled by GPIO15_SEL register.<br>1: GPIO15/LED_VSB/ALERT# will function as ALERT#. |

**8.1.12 Multi Function Select 2 Register — Index 2Ah (Powered by VSB3V)**

| Bit | Name | R/W | Default | Description |
|-----|------|-----|---------|-------------|
|-----|------|-----|---------|-------------|

|     |            |     |       |  |
|-----|------------|-----|-------|--|
| 7-6 | VSBLED_SEL | R/W | 2'b00 | VSBLED function select, powered by VSB.<br>00: VSBLED always output low.<br>01: VSBLED tri-state<br>10: VSBLED output 0.5Hz clock.<br>11: VSBLED output 1Hz clock.<br>( clock output is inverse with VDDLED clock output ) |
| 5-4 | VDDLED_SEL | R/W | 2'b00 | VDDLED function select, powered by VDD.<br>00: VDDLED always output low.<br>01: VDDLED tri-state<br>10: VDDLED output 0.5Hz clock.<br>11: VDDLED output 1Hz clock.<br>( clock output is inverse with VSBLED clock output ) |
| 3   | GPIO33_SEL | R/W | 0     | 0: RSMRST#/GPIO33 functions as RSMRST#.<br>1: RSMRST#/GPIO33 functions as GPIO33.  |
| 2   | GPIO32_SEL | R/W | 0     | 0: PWROK/GPIO32 functions as PWROK.<br>1: PWROK/GPIO32 functions as GPIO32.  |
| 1   | GPIO31_SEL | R/W | 0     | 0: PS_ON#/GPIO31 functions as PS_ON#.<br>1: PS_ON#/GPIO31 functions as GPIO31.   |
| 0   | GPIO30_SEL | R/W | 0     | 0: S3#/GPIO30 functions as S3#.<br>1: S3#/GPIO30 functions as GPIO30.  |

**8.1.13 Multi Function Select 3 Register — Index 2Bh (Powered by VSB3V)**

| Bit | Name       | R/W | Default | Description   |
|-----|------------|-----|---------|---|
| 7   | Reserved   | R/W | 0       | Dummy register.   |
| 6   | GPIO16_SEL | R/W | 0       | 0: GPIO16/LED_VCC functions as GPIO16.<br>1: GPIO16/LED_VCC functions as LED_VCC.   |
| 5   | GPIO15_SEL | R/W | 0       | When register ALERT_GP_EN is 0, the register functions as:<br>0: GPIO15/LED_VSB/ALERT# functions as GPIO15.<br>1: GPIO15/LED_VSB/ALERT# functions as LED_VSB. |
| 4   | GPIO14_SEL | R/W | 0       | 0: GPIO14/FWH_DIS/WDTRST# functions as GPIO14 when SPI is disabled.<br>1: GPIO14/FWH_DIS/WDTRST# functions as WDTRST# when SPI is disabled.                   |
| 3   | GPIO13_SEL | R/W | 0       | 0: GPIO13/SPI_MOSI/BEEP functions as GPIO13 when SPI is disabled.<br>1: GPIO13/SPI_MOSI/BEEP functions as BEEP when SPI is disabled.                          |
| 2   | GPIO12_SEL | R/W | 0       | 0: GPIO12/SPI_MISO/FANCTRL1_1 functions as GPIO12 when SPI is disabled.<br>1: GPIO12/SPI_NISO/FANCTRL1_1 functions as FANCTRL1_1 when SPI is disabled.        |
| 1-0 | Reserved   | R/W | 0       | Reserved  |

**8.1.14 Multi Function Select 4 Register — Index 2Ch (Powered by VSB3V)**

| Bit | Name | R/W | Default | Description |
|-----|------|-----|---------|-------------|
|-----|------|-----|---------|-------------|

|   |            |     |   |  |
|---|------------|-----|---|--|
| 7 | GPIO27_SEL | R/W | 0 | 0: PWSOUT#/GPIO27 functions as PWSOUT#.<br>1: PWSOUT#/GPIO27 functions as GPIO27.    |
| 6 | GPIO26_SEL | R/W | 0 | 0: PWSIN#/GPIO26 functions as PWSIN#.<br>1: PWSIN#/GPIO26 functions as GPIO26.       |
| 5 | GPIO25_SEL | R/W | 0 | 0: PME#/GPIO25 functions as PME#.<br>1: PME#/GPIO25 functions as GPIO25.             |
| 4 | GPIO24_SEL | R/W | 0 | 0: ATXPG_IN/GPIO24 functions as ATXPG_IN.<br>1: ATXPG_IN/GPIO24 functions as GPIO24. |
| 3 | Reserved   | R/W | 0 | Reserved   |
| 2 | GPIO22_SEL | R/W | 0 | 0: PCIRST3#/GPIO22 functions as PCIRST3#.<br>1: PCIRST3#/GPIO22 functions as GPIO22. |
| 1 | GPIO21_SEL | R/W | 0 | 0: PCIRST2#/GPIO21 functions as PCIRST2#.<br>1: PCIRST2#/GPIO21 functions as GPIO21. |
| 0 | GPIO20_SEL | R/W | 0 | 0: PCIRST1#/GPIO20 functions as PCIRST1#.<br>1: PCIRST1#/GPIO20 functions as GPIO20. |

**8.1.15 Wakeup Control Register — Index 2Dh (Powered by VBAT)**

| Bit | Name       | R/W | Default | Description  |
|-----|------------|-----|---------|--|
| 7   | SPI_CS1_EN | R/W | 0       | This register decides the architecture of SPI when used as primary BIOS.<br>1: use two 4Mbits. (FWH_DIS will multi-functions as SPI_CS1#)<br>0: use one 8Mbits. (Divided into two 4Mbits. Originally use the higher part. If the higher part is booting fail, the memory address will be auto mapped to lower part.) |
| 6-4 | Reserved   | R/W | 0       | Dummy register.  |
| 3   | WAKEUP_EN  | R/W | 1       | 0: disable keyboard/mouse wake up.<br>1: enable keyboard/mouse wake up.  |
| 2-1 | KEY_SEL    | R/W | 00      | This registers select the keyboard wake up key.<br>When KEY_SEL_ADD is low, the register indicates<br>00: Wake up key is Ctrl + Esc.<br>01: Wake up key is Ctrl + F1.<br>10: Wake up key is Ctrl + Space.<br>11: Wake up key is any key.<br>Otherwise, wake up key is win98 wakeup key.                              |
| 0   | MO_SEL     | R/W | 0       | This register selects the mouse wake up key.<br>0: Wake up by click.<br>1: Wake up by click and movement.  |



## 8.2 FDC Registers (CR00)

### 8.2.1 FDC Configuration Registers

#### FDC Device Enable Register — Index 30h

| Bit | Name     | R/W | Default | Description                       |
|-----|----------|-----|---------|-----------------------------------|
| 7-1 | Reserved | -   | -       | Reserved                          |
| 0   | FDC_EN   | R/W | 1       | 0: disable FDC.<br>1: enable FDC. |

#### Base Address High Register — Index 60h

| Bit | Name         | R/W | Default | Description                  |
|-----|--------------|-----|---------|------------------------------|
| 7-0 | BASE_ADDR_HI | R/W | 03h     | The MSB of FDC base address. |

#### Base Address Low Register — Index 61h

| Bit | Name         | R/W | Default | Description                  |
|-----|--------------|-----|---------|------------------------------|
| 7-0 | BASE_ADDR_LO | R/W | F0h     | The LSB of FDC base address. |

#### IRQ Channel Select Register — Index 70h

| Bit | Name      | R/W | Default | Description                     |
|-----|-----------|-----|---------|---------------------------------|
| 7-4 | Reserved  | -   | -       | Reserved.                       |
| 3-0 | SELFDCIRQ | R/W | 06h     | Select the IRQ channel for FDC. |

#### DMA Channel Select Register — Index 74h

| Bit | Name      | R/W | Default | Description                     |
|-----|-----------|-----|---------|---------------------------------|
| 7-3 | Reserved  | -   | -       | Reserved.                       |
| 2-0 | SELFDCDMA | R/W | 010     | Select the DMA channel for FDC. |

#### FDD Mode Register — Index F0h

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-4 | Reserved  | -   | -       | Reserved.   |
| 3-2 | IF_MODE   | R/W | 11      | 00: Model 30 mode.<br>01: PS/2 mode.<br>10: Reserved.<br>11: AT mode (default). |
| 1   | FDMA MODE | R/W | 1       | 0: enable burst mode.<br>1: non-busrt mode (default).                           |
| 0   | EN3MODE   | R/W | 0       | 0: normal floppy mode (default).<br>1: enhanced 3-mode FDD.                     |

#### FDD Drive Type Register — Index F2h

| Bit | Name     | R/W | Default | Description |
|-----|----------|-----|---------|-------------|
| 7-2 | Reserved | -   | -       | Reserved.   |

|     |          |     |    |                 |
|-----|----------|-----|----|-----------------|
| 1-0 | FDD_TYPE | R/W | 11 | FDD drive type. |
|-----|----------|-----|----|-----------------|

**FDD Selection Register — Index F4h**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-5 | Reserved | -   | -       | Reserved.   |
| 4-3 | FDD_DRT  | R/W | 00      | Data rate table select, refer to table A.<br>00: select regular drives and 2.88 format.<br>01: 3-mode drive.<br>10: 2 mega tape.<br>11: reserved. |
| 2   | Reserved | -   | -       | Reserved.   |
| 1-0 | FDD_DT   | R/W | 00      | Drive type select, refer to table B.  |

**TABLE A**

| Data Rate Table Select |            | Data Rate |           | Selected Data Rate |      | DENSEL |
|------------------------|------------|-----------|-----------|--------------------|------|--------|
| FDD_DRT[1]             | FDD_DRT[0] | DATARATE1 | DATARATE0 | MFM                | FM   |        |
|                        |            | 0         | 0         | 500K               | 250K | 1      |
|                        |            | 0         | 1         | 300K               | 150K | 0      |
| 0                      | 0          | 1         | 0         | 250K               | 125K | 0      |
|                        |            | 1         | 1         | 1Meg               | ---  | 1      |
|                        |            | 0         | 0         | 500K               | 250K | 1      |
|                        |            | 0         | 1         | 500K               | 250K | 0      |
| 0                      | 1          | 1         | 0         | 250K               | 125K | 0      |
|                        |            | 1         | 1         | 1Meg               | ---  | 1      |
|                        |            | 0         | 0         | 500K               | 250K | 1      |
|                        |            | 0         | 1         | 2Meg               | ---  | 0      |
| 1                      | 0          | 1         | 0         | 250K               | 125K | 0      |
|                        |            | 1         | 1         | 1Meg               | ---  | 1      |

**TABLE B**

| Drive Type |         | DRV DENO  | Remark   |
|------------|---------|-----------|--|
| FDD_DT1    | FDD_DT0 |           |  |
| 0          | 0       | DENSEL    | 4/2/1 MB 3.5"<br>2/1 MB 5.25"<br>1/1.6/1 MB 3.5" (3-Mode ) |
| 0          | 1       | DATARATE1 |  |
| 1          | 0       | DENSEL#   |  |
| 1          | 1       | DATARATE0 |  |

### 8.3 UART1 Registers (CR01)

#### 8.3.1 UART 1 Configuration Registers

##### UART 1 Device Enable Register — Index 30h

| Bit | Name     | R/W | Default | Description                             |
|-----|----------|-----|---------|---|
| 7-1 | Reserved | -   | -       | Reserved                                |
| 0   | UR1_EN   | R/W | 1       | 0: disable UART 1.<br>1: enable UART 1. |

##### Base Address High Register — Index 60h

| Bit | Name         | R/W | Default | Description                     |
|-----|--------------|-----|---------|---------------------------------|
| 7-0 | BASE_ADDR_HI | R/W | 03h     | The MSB of UART 1 base address. |

##### Base Address Low Register — Index 61h

| Bit | Name         | R/W | Default | Description                     |
|-----|--------------|-----|---------|---------------------------------|
| 7-0 | BASE_ADDR_LO | R/W | F8h     | The LSB of UART 1 base address. |

##### IRQ Channel Select Register — Index 70h

| Bit | Name      | R/W | Default | Description                        |
|-----|-----------|-----|---------|------------------------------------|
| 7-4 | Reserved  | -   | -       | Reserved.                          |
| 3-0 | SELUR1IRQ | R/W | 4h      | Select the IRQ channel for UART 1. |

##### RS485 Enable Register — Index F0h

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-5 | Reserved | -   | -       | Reserved.  |
| 4   | RS485_EN | R/W | 0       | 0: RS232 driver.<br>1: RS485 driver. Auto drive RTS# low when transmitting data. |
| 3-0 | Reserved | -   | -       | Reserved.  |

## 8.4 UART 2 Registers (CR02)

### 8.4.1 UART 2 Configuration Registers

#### UART 2 Device Enable Register — Index 30h

| Bit | Name     | R/W | Default | Description                             |
|-----|----------|-----|---------|---|
| 7-1 | Reserved | -   | -       | Reserved                                |
| 0   | UR2_EN   | R/W | 1       | 0: disable UART 2.<br>1: enable UART 2. |

#### Base Address High Register — Index 60h

| Bit | Name         | R/W | Default | Description                     |
|-----|--------------|-----|---------|---------------------------------|
| 7-0 | BASE_ADDR_HI | R/W | 02h     | The MSB of UART 2 base address. |

#### Base Address Low Register — Index 61h

| Bit | Name         | R/W | Default | Description                     |
|-----|--------------|-----|---------|---------------------------------|
| 7-0 | BASE_ADDR_LO | R/W | F8h     | The LSB of UART 2 base address. |

#### IRQ Channel Select Register — Index 70h

| Bit | Name      | R/W | Default | Description                        |
|-----|-----------|-----|---------|------------------------------------|
| 7-4 | Reserved  | -   | -       | Reserved.                          |
| 3-0 | SELUR2IRQ | R/W | 3h      | Select the IRQ channel for UART 2. |

#### RS485 Enable Register — Index F0h

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-5 | Reserved | -   | -       | Reserved.  |
| 4   | RS485_EN | R/W | 0       | 0: RS232 driver.<br>1: RS485 driver. Auto drive RTS# low when transmitting data.   |
| 3   | RXW4C_IR | R/W | 0       | 0: No reception delay when SIR is changed form TX to RX.<br>1: Reception delays 4 characters time when SIR is changed form TX to RX.       |
| 2   | TXW4C_IR | R/W | 0       | 0: No transmission delay when SIR is changed form RX to TX.<br>1: Transmission delays 4 characters time when SIR is changed form RX to TX. |
| 1-0 | Reserved | -   | -       | Reserved.  |

#### SIR Mode Control Register — Index F1h

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7   | Reserved | -   | -       | Reserved.  |
| 6   | Reserved | -   | -       | Reserved.  |
| 5   | Reserved | -   | -       | Reserved.  |
| 4-3 | IRMODE   | R/W | 00      | 00: disable IR function.<br>01: disable IR function.<br>10: IrDA function, active pulse is 1.6uS.<br>11: IrDA function, active pulse is 3/16 bit time. |

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|   |          |     |   |  |
|---|----------|-----|---|--|
| 2 | HDUPLX   | R/W | 1 | 0: SIR is in full duplex mode for loopbak test. TXW4C_IR and RXW4C_IR are of no use.<br>1: SIR is in half duplex mode. |
| 1 | TXINV_IR | R/W | 0 | 0: IRTX is in normal condition.<br>1: inverse the IRTX.  |
| 0 | RXINV_IR | R/W | 0 | 0: IRRX is in normal condition.<br>1: inverse the IRRX.  |

## 8.5 Parallel Port Registers (CR03)

### 8.5.1 Parallel Port Configuration Registers

#### Parallel Port Device Enable Register — Index 30h

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-1 | Reserved | -   | -       | Reserved  |
| 0   | PRT_EN   | R/W | 1       | 0: disable Parallel Port.<br>1: enable Parallel Port. |

#### Base Address High Register — Index 60h

| Bit | Name         | R/W | Default | Description                            |
|-----|--------------|-----|---------|--|
| 7-0 | BASE_ADDR_HI | R/W | 03h     | The MSB of Parallel Port base address. |

#### Base Address Low Register — Index 61h

| Bit | Name         | R/W | Default | Description                            |
|-----|--------------|-----|---------|--|
| 7-0 | BASE_ADDR_LO | R/W | 78h     | The LSB of Parallel Port base address. |

#### IRQ Channel Select Register — Index 70h

| Bit | Name      | R/W | Default | Description                               |
|-----|-----------|-----|---------|---|
| 7-5 | Reserved  | -   | -       | Reserved.                                 |
| 3-0 | SELPRTIRQ | R/W | 7h      | Select the IRQ channel for Parallel Port. |

#### DMA Channel Select Register — Index 74h

| Bit | Name         | R/W | Default | Description   |
|-----|--------------|-----|---------|---|
| 7-5 | Reserved     | -   | -       | Reserved.   |
| 4   | ECP_DMA_MODE | R/W | 0       | 0: non-burst mode DMA.<br>1: enable burst mode DMA. |
| 3   | Reserved     | -   | -       | Reserved.   |
| 2-0 | SELPRTDMA    | R/W | 011     | Select the DMA channel for Parallel Port.           |

#### PRT Mode Select Register — Index F0h

| Bit | Name         | R/W | Default | Description   |
|-----|--------------|-----|---------|---|
| 7   | SPP_IRQ_MODE | R/W | 0       | Interrupt mode in non-ECP mode.<br>0: Level mode.<br>1: Pulse mode. |
| 6-3 | ECP_FIFO_THR | R/W | 1000    | ECP FIFO threshold.   |

|     |          |     |     |   |
|-----|----------|-----|-----|---|
| 2-0 | PRT_MODE | R/W | 010 | 000: Standard and Bi-direction (SPP) mode.<br>001: EPP 1.9 and SPP mode.<br>010: ECP mode (default).<br>011: ECP and EPP 1.9 mode.<br>100: Printer mode.<br>101: EPP 1.7 and SPP mode.<br>110: Reserved.<br>111: ECP and EPP1.7 mode. |
|-----|----------|-----|-----|---|

## 8.6 Hardware Monitor Registers (CR04)

### 8.6.1 Hardware Monitor Configuration Registers

#### Hardware Monitor Device Enable Register — Index 30h

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-1 | Reserved | -   | -       | Reserved  |
| 0   | HM_EN    | R/W | 1       | 0: disable Hardware Monitor.<br>1: enable Hardware Monitor. |

#### Base Address High Register — Index 60h

| Bit | Name         | R/W | Default | Description                               |
|-----|--------------|-----|---------|---|
| 7-0 | BASE_ADDR_HI | R/W | 02h     | The MSB of Hardware Monitor base address. |

#### Base Address Low Register — Index 61h

| Bit | Name         | R/W | Default | Description                               |
|-----|--------------|-----|---------|---|
| 7-0 | BASE_ADDR_LO | R/W | 95h     | The LSB of Hardware Monitor base address. |

#### IRQ Channel Select Register — Index 70h

| Bit | Name     | R/W | Default | Description                                  |
|-----|----------|-----|---------|--|
| 7-4 | Reserved | -   | -       | Reserved.                                    |
| 3-0 | SELMIRQ  | R/W | 0000    | Select the IRQ channel for Hardware Monitor. |

### 8.6.2 Device Registers

Before the device registers, the following is a register map order which shows a summary of all registers.

Please refer each one register if you want more detail information.

Register CR01 ~ CR03 → Configuration Registers

Register CR10 ~ CR4F → Voltage Setting Register

Register CR60 ~ CR8E → Temperature Setting Register

Register CR90 ~ CRDF → Fan Control Setting Register

→Fan1 Detail Setting CRA0 ~ CRAF

→Fan2 Detail Setting CRB0 ~ CRBF

→Fan3 Detail Setting CRC0 ~ CRCF

#### 8.6.2.1 Configuration Register — Index 01h

| Bit | Name       | R/W | Default | Description   |
|-----|------------|-----|---------|---|
| 7-3 | Reserved   | 0h  | 0       | Reserved  |
| 2   | POWER_DOWN | R/W | 0       | Hardware monitor function power down.   |
| 1   | FAN_START  | R/W | 1       | Set one to enable startup of fan monitoring operations; a zero puts the part in standby mode.                     |
| 0   | V_T_START  | R/W | 1       | Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode. |



**8.6.2.2 Configuration Register — Index 02h**

| Bit | Name         | R/W | Default | Description  |
|-----|--------------|-----|---------|--|
| 7   | Reserved     | R/W | 0       | Dummy register.  |
| 6   | CASE_BEEP_EN | R/W | 0       | 0: Disable case open event output via BEEP.<br>1: Enable case open event output via BEEP.  |
| 5-4 | OVT_MODE     | R/W | 0       | 00: The OVT# will be low active level mode.<br>01: The OVT# will be high active level mode.<br>10: The OVT# will indicate by 1Hz LED function.<br>11: The OVT# will indicate by (400/800HZ) BEEP output.         |
| 3   | Reserved     | R/W | 0       | Dummy register.  |
| 2   | CASE_SMI_EN  | R/W | 0       | 0: Disable case open event output via PME.<br>1: Enable case open event output via PME.  |
| 1-0 | ALERT_MODE   | R/W | 0       | 00: The ALERT# will be low active level mode.<br>01: The ALERT# will be high active level mode.<br>10: The ALERT# will indicate by 1Hz LED function.<br>11: The ALERT# will indicate by (400/800HZ) BEEP output. |

**8.6.2.3 Configuration Register — Index 03h**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-1 | Reserved | R/W | 0       | Return 0 when read.  |
| 0   | CASE_STS | R/W | 0       | Case open event status, write 1 to clear if case open event cleared. |

**8.6.2.4 Configuration Register — Index 0Ah**

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-6 | Reserved  | -   | 00      | Reserved.   |
| 5   | T1_IIR_EN | R/W | 0       | Set 1 to enable IIR for AMDSI/PECI reading.<br>The reading will be more stable.   |
| 4   | Reserved  | R/W | 0       | Reserved.   |
| 3-2 | VTT_SEL   | R/W | 0       | PECI (Vtt) voltage select.<br>00: Vtt is 1.23V<br>01: Vtt is 1.13V<br>10: Vtt is 1.00V<br>11: Vtt is 1.00V                                |
| 1-0 | MEAS_TYPE | R/W | 00      | CPU Temperature Measurement method.<br>00: with external diode.<br>01: with PECI interface.<br>10: with AMDSI interface.<br>11: reserved. |

**8.6.2.5 Configuration Register — Index 0Bh (MEAS\_TYPE == 2'b01)**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-4 | CPU_SEL  | R/W | 0       | Select the Intel CPU socket number.<br>0000: no CPU presented. PECI host will use Ping() command to find CPU address.<br>0001: CPU is in socket 0, i.e. PECI address is 0x30.<br>0010: CPU is in socket 0, i.e. PECI address is 0x31.<br>0100: CPU is in socket 0, i.e. PECI address is 0x32.<br>1000: CPU is in socket 0, i.e. PECI address is 0x33.<br>Otherwise are reserved. |
| 3-1 | Reserved | -   | 0       | Reserved.  |

|   |            |     |   |   |
|---|------------|-----|---|---|
| 0 | DOMAIN1_EN | R/W | 0 | If the CPU selected is dual core. Set this register 1 to read the temperature of domain1. |
|---|------------|-----|---|---|

**8.6.2.6 Configuration Register — Index 0Bh (MEAS\_TYPE == 2'b10)**

| Bit | Name      | R/W | Default | Description               |
|-----|-----------|-----|---------|---------------------------|
| 7-0 | AMDSI_VER | R   | -       | Return the AMDSI version. |

**8.6.2.7 Configuration Register — Index 0Ch (MEAS\_TYPE == 2'b01)**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-0 | TCC_TEMP | R/W | 8'h55   | TCC Activation Temperature.<br>The absolute value of CPU temperature is calculated by the equation:<br>CPU_TEMP = TCC_TEMP + PECI Reading.<br>The range of this register is 0 ~ 255. |

**8.6.2.8 Configuration Register — Index 0Ch (MEAS\_TYPE == 2'b10)**

| Bit | Name    | R/W | Default | Description               |
|-----|---------|-----|---------|---------------------------|
| 7-0 | NODE_ID | R   | -       | Return the AMDSI node id. |

**8.6.2.9 Configuration Register — Index 0Dh**

| Bit | Name     | R/W | Default | Description |
|-----|----------|-----|---------|-------------|
| 7-0 | Reserved | -   | -       | Reserved.   |

**8.6.2.10 Configuration Register — Index 0Eh**

| Bit | Name           | R/W | Default | Description   |
|-----|----------------|-----|---------|---|
| 7-4 | Reserved       | R/W | 0       | Reserved.   |
| 3   | PECI_SCALE_ADD | R/W | 0       | This register is used to indicate how to calculate the PECI reading with PECI_SCALE register.<br>0: The real value is the reading adds the value calculated by PECI_SCALE.<br>1: The real value is the reading adds the value calculated by PECI_SCALE.   |
| 2-0 | PECI_SCALE     | R/W | 0       | This register is used to control the PECI reading slope. See also PECI_SCALE_ADD register.<br>000: The real value is the PECI reading.<br>001: The real value is (1 ± 1/2) PECI reading.<br>010: The real value is (1 ± 1/4) PECI reading.<br>011: The real value is (1 ± 1/8) PECI reading.<br>100: The real value is (1 ± 1/16) PECI reading.<br>101: The real value is (1 ± 1/32) PECI reading.<br>110: The real value is (1 ± 1/64) PECI reading.<br>111: The real value is (1 ± 1/128) PECI reading. |

**8.6.2.11 Configuration Register — Index 0Fh**

| Bit | Name      | R/W | Default | Description |
|-----|-----------|-----|---------|-------------|
| 7-0 | Reserved. | -   | -       | Reserved    |

**Voltage Setting**
**8.6.2.12 Voltage1 Voltage reading and limit— Index 20h- 4Fh**

| Address | Attribute | Default Value | Description                                     |
|---------|-----------|---------------|---|
| 20h     | RO        | --            | VCC3V reading. The unit of reading is 8mV.      |
| 21h     | RO        | --            | V1 (Vcore) reading. The unit of reading is 8mV. |
| 22h     | RO        | --            | V2 reading. The unit of reading is 8mV.         |
| 23h     | RO        | --            | V3 reading. The unit of reading is 8mV.         |
| 24h     | RO        | --            | V4 reading. The unit of reading is 8mV.         |
| 25h     | RO        | --            | V5 reading. The unit of reading is 8mV.         |
| 26h     | RO        | --            | V6 reading. The unit of reading is 8mV.         |
| 27h     | RO        | --            | VSB3V reading. The unit of reading is 8mV.      |
| 28h     | RO        | --            | VBAT reading. The unit of reading is 8mV.       |
| 29~2Fh  | RO        | FF            | Reserved  |
| 30~4Fh  | RO        | FF            | Reserved  |

**Temperature Setting**
**8.6.2.13 Temperature PME# Enable Register — Index 60h**

| Bit | Name          | R/W | Default | Description   |
|-----|---------------|-----|---------|---|
| 7   | EN_T3_OVT_PME | R/W | 0       | If set this bit to 1, PME# signal will be issued when TEMP3 exceeds OVT limit setting.  |
| 6   | EN_T2_OVT_PME | R/W | 0       | If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.        |
| 5   | EN_T1_OVT_PME | R/W | 0       | If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.        |
| 4   | Reserved      | R/W | 0       | Reserved  |
| 3   | EN_T3_EXC_PME | R/W | 0       | If set this bit to 1, PME# signal will be issued when TEMP3 exceeds high limit setting. |
| 2   | EN_T2_EXC_PME | R/W | 0       | If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting. |
| 1   | EN_T1_EXC_PME | R/W | 0       | If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting. |
| 0   | Reserved      | R/W | 0       | Reserved  |

**8.6.2.14 Temperature Interrupt Status Register — Index 61h**

| Bit | Name       | R/W | Default | Description   |
|-----|------------|-----|---------|---|
| 7   | T3_OVT_STS | R/W | 0       | A one indicates TEMP3 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.   |
| 6   | T2_OVT_STS | R/W | 0       | A one indicates TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.   |
| 5   | T1_OVT_STS | R/W | 0       | A one indicates TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.   |
| 4   | Reserved   | R/W | 0       | Reserved  |
| 3   | T3_EXC_STS | R/W | 0       | A one indicates TEMP3 temperature sensor has exceeded high limit or below the “high limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored. |

|   |            |     |   |   |
|---|------------|-----|---|---|
| 2 | T2_EXC_STS | R/W | 0 | A one indicates TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored. |
| 1 | T1_EXC_STS | R/W | 0 | A one indicates TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored. |
| 0 | Reserved   | R/W | 0 | Reserved  |

**8.6.2.15 Temperature Real Time Status Register — Index 62h**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7   | T3_OVT   | R/W | 0       | Set when the TEMP3 exceeds the OVT limit. Clear when the TEMP3 is below the “OVT limit –hysteresis” temperature.   |
| 6   | T2_OVT   | R/W | 0       | Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.   |
| 5   | T1_OVT   | R/W | 0       | Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.   |
| 4   | Reserved | R/W | 0       | Reserved   |
| 3   | T3_EXC   | R/W | 0       | Set when the TEMP3 exceeds the high limit. Clear when the TEMP3 is below the “high limit –hysteresis” temperature. |
| 2   | T2_EXC   | R/W | 0       | Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature. |
| 1   | T1_EXC   | R/W | 0       | Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature. |
| 0   | Reserved | R/W | 0       | Reserved   |

**8.6.2.16 Temperature BEEP Enable Register — Index 63h**

| Bit | Name           | R/W | Default | Description   |
|-----|----------------|-----|---------|---|
| 7   | EN_T3_OVT_BEEP | R/W | 0       | If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds OVT limit setting.  |
| 6   | EN_T2_OVT_BEEP | R/W | 0       | If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.  |
| 5   | EN_T1_OVT_BEEP | R/W | 0       | If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.  |
| 4   | Reserved       | R/W | 0       | Reserved  |
| 3   | EN_T3_EXC_BEEP | R/W | 0       | If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds high limit setting. |
| 2   | EN_T2_EXC_BEEP | R/W | 0       | If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting. |
| 1   | EN_T1_EXC_BEEP | R/W | 0       | If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting. |
| 0   | Reserved       | R/W | 0       | Reserved  |

**8.6.2.17 OVT Output Enable Register 1 — Index 66h**

| Bit | Name        | R/W | Default | Description  |
|-----|-------------|-----|---------|--|
| 7   | EN_T3_ALERT | R   | 0       | Enable temperature 3 alert event (asserted when temperature over high limit) |
| 6   | EN_T2_ALERT | R   | 0       | Enable temperature 2 alert event (asserted when temperature over high limit) |
| 5   | EN_T1_ALERT | R   | 0       | Enable temperature 1 alert event (asserted when temperature over high limit) |
| 4   | Reserved    | R   | 0       | Reserved for temp4   |

|   |           |     |    |  |
|---|-----------|-----|----|--|
| 3 | EN_T3_OVT | R/W | 0  | Enable over temperature (OVT) mechanism of temperature3. |
| 2 | EN_T2_OVT | R/W | 0  | Enable over temperature (OVT) mechanism of temperature2. |
| 1 | EN_T1_OVT | R/W | 1  | Enable over temperature (OVT) mechanism of temperature1. |
| 0 | Reserved  | R   | 0h | Reserved.  |

**8.6.2.18 Temperature Sensor Type Register — Index 6Bh**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-4 | Reserved | RO  | 0       | --  |
| 3   | T3_MODE  | R/W | 1       | 0: TEMP3 is connected to a thermistor<br>1: TEMP3 is connected to a BJT.(default)   |
| 2   | T2_MODE  | R/W | 1       | 0: TEMP2 is connected to a thermistor.<br>1: TEMP2 is connected to a BJT. (default) |
| 1   | T1_MODE  | R/W | 1       | 0: TEMP1 is connected to a thermistor<br>1: TEMP1 is connected to a BJT.(default)   |
| 0   | Reserved | R   | 0h      | --  |

**8.6.2.19 TEMP1 Limit Hystersis Select Register -- Index 6Ch**

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-4 | TEMP1_HYS | R/W | 4h      | Limit hysteresis. (0~15 degree C)<br>Temperature and below the ( boundary – hysteresis ). |
| 3-0 | Reserved  | R   | 0h      | --  |

**8.6.2.20 TEMP2 and TEMP3 Limit Hystersis Select Register -- Index 6Dh**

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-4 | TEMP3_HYS | R/W | 2h      | Limit hysteresis. (0~15 degree C)<br>Temperature and below the ( boundary – hysteresis ). |
| 3-0 | TEMP2_HYS | R/W | 4h      | Limit hysteresis. (0~15 degree C)<br>Temperature and below the ( boundary – hysteresis ). |

**8.6.2.21 DIODE OPEN Status Register -- Index 6Fh**

| Bit | Name          | R/W | Default | Description  |
|-----|---------------|-----|---------|--|
| 7-4 | Reserved      | RO  | 0h      | Reserved   |
| 3   | T3_DIODE_OPEN | RO  | 0h      | External diode 3 is open   |
| 2   | T2_DIODE_OPEN | RO  | 0h      | External diode 2 is open   |
| 1   | T1_DIODE_OPEN | RO  | 0h      | This register indicates the abnormality of temperature 1 measurement.<br>When AMDSI interface is enabled, it indicates the error of not receiving ACK bit when read TCON command is asserted.<br>When PECl interface is enabled, it indicates a error code is received from PECl slave.<br>When external diode is used, it indicates the BJT is open or short. |
| 0   | Reserved      | R   | 0h      | --   |

## Temperature — Index 70h- 8Fh

| Address | Attribute | Default Value | Description |
|---------|-----------|---------------|-------------|
| 70h     | Reserved  | FFh           | Reserved    |

|        |          |     |  |
|--------|----------|-----|--|
| 71h    | Reserved | FFh | Reserved   |
| 72h    | RO       | --  | Temperature 1 reading. The unit of reading is 1°C. At the moment of reading this register. |
| 73h    | RO       | --  | Reserved   |
| 74h    | RO       | --  | Temperature 2 reading. The unit of reading is 1°C. At the moment of reading this register. |
| 75h    | RO       | --  | Reserved   |
| 76h    | RO       | --  | Temperature 3 reading. The unit of reading is 1°C. At the moment of reading this register. |
| 77-7Bh | RO       | --  | Reserved   |
| 7C-7Fh | RO       | FFh | Reserved   |
| 80h    | Reserved | FFh | Reserved   |
| 81h    | Reserved | FFh | Reserved   |
| 82h    | R/W      | 64h | Temperature sensor 1 OVT limit. The unit is 1°C.   |
| 83h    | R/W      | 55h | Temperature sensor 1 high limit. The unit is 1°C.  |
| 84h    | R/W      | 64h | Temperature sensor 2 OVT limit. The unit is 1°C.   |
| 85h    | R/W      | 55h | Temperature sensor 2 high limit. The unit is 1°C.  |
| 86h    | R/W      | 55h | Temperature sensor 3 OVT limit. The unit is 1°C.   |
| 87h    | R/W      | 46h | Temperature sensor 3 high limit. The unit is 1°C.  |
| 88-8Bh | RO       | --  | Reserved   |
| 8C~8Dh | RO       | FFh | Reserved   |

**8.6.2.22 Temperature Filter Select Register -- Index 8Eh**

| Bit | Name       | R/W | Default | Description   |
|-----|------------|-----|---------|---|
| 7-6 | IIR-QUEUR3 | R/W | 0h      | The queue time for second filter to quickly update values.<br>00: disable.<br>01: 16 times.<br>10: 32 times. (default)<br>11: 48 times. |
| 5-4 | IIR-QUEUR2 | R/W | 0h      | The queue time for second filter to quickly update values.<br>00: disable.<br>01: 16 times.<br>10: 32 times. (default)<br>11: 48 times. |
| 3-2 | IIR-QUEUR1 | R/W | 0h      | The queue time for second filter to quickly update values.<br>00: disable.<br>01: 16 times.<br>10: 32 times. (default)<br>11: 48 times. |
| 0   | Reserved   | R   | 0h      | --  |

**Fan Control Setting**
**8.6.2.23 FAN PME# Enable Register — Index 90h**

| Bit | Name        | R/W | Default | Description  |
|-----|-------------|-----|---------|--|
| 7-3 | Reserved    | RO  | 0h      | Reserved   |
| 2   | EN_FAN3_PME | R/W | 0h      | A one enables the corresponding interrupt status bit for PME# interrupt.<br>Set this bit 1 to enable PME# function for Fan3. |
| 1   | EN_FAN2_PME | R/W | 0h      | A one enables the corresponding interrupt status bit for PME# interrupt.<br>Set this bit 1 to enable PME# function for Fan2. |

|   |             |     |    |   |
|---|-------------|-----|----|---|
| 0 | EN_FAN1_PME | R/W | 0h | A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1. |
|---|-------------|-----|----|---|

**8.6.2.24 FAN Interrupt Status Register — Index 91h**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-3 | Reserved | RO  | 0       | Reserved   |
| 2   | FAN3_STS | R/W | --      | This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored. |
| 1   | FAN2_STS | R/W | --      | This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored. |
| 0   | FAN1_STS | R/W | --      | This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored. |

**8.6.2.25 FAN Real Time Status Register — Index 92h**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-3 | Reserved | --  | 0       | Reserved   |
| 2   | FAN3_EXC | RO  | --      | This bit set to high mean that fan3 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec. |
| 1   | FAN2_EXC | RO  | --      | This bit set to high mean that fan2 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec. |
| 0   | FAN1_EXC | RO  | --      | This bit set to high mean that fan1 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec. |

**8.6.2.26 FAN BEEP# Enable Register — Index 93h**

| Bit | Name            | R/W | Default | Description  |
|-----|-----------------|-----|---------|--|
| 7   | FULL_WITH_T3_EN | R/W | 0       | Set one will enable FAN to force full speed when T3 over high limit. |
| 6   | FULL_WITH_T2_EN | R/W | 0       | Set one will enable FAN to force full speed when T2 over high limit. |
| 5   | FULL_WITH_T1_EN | R/W | 0       | Set one will enable FAN to force full speed when T1 over high limit. |
| 4   | Reserved        | R/W | 0       | Reserved for local temperature.                                      |
| 3   | Reserved        | R   | 0       | Reserved.  |
| 2   | EN_FAN3_BEEP    | R/W | 0       | A one enables the corresponding interrupt status bit for BEEP.       |
| 1   | EN_FAN2_BEEP    | R/W | 0       | A one enables the corresponding interrupt status bit for BEEP.       |
| 0   | EN_FAN1_BEEP    | R/W | 0       | A one enables the corresponding interrupt status bit for BEEP.       |

**8.6.2.27 Fan Type Select Register -- Index 94h**

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-6 | Reserved  | R   | 0       | Reserved.   |
| 5-4 | FAN3_TYPE | R/W | 2'b 0S  | 00: Output PWM mode (pushpull) to control fans.<br>01: Use linear fan application circuit to control fan speed by fan's power terminal .<br>10: Output PWM mode (open drain) to control Intel 4-wire fans.<br>11: Reserved. |
| 3-2 | FAN2_TYPE | R/W | 2'b 0S  | 00: Output PWM mode (pushpull) to control fans.<br>01: Use linear fan application circuit to control fan speed by fan's power terminal .<br>10: Output PWM mode (open drain) to control Intel 4-wire fans.<br>11: Reserved. |

|     |           |     |        |  |
|-----|-----------|-----|--------|--|
| 1-0 | FAN1_TYPE | R/W | 2'b 0S | 00: Output PWM mode (push pull) to control fans.<br>01: Use linear fan application circuit to control fan speed by fan's power terminal .<br>10: Output PWM mode (open drain) to control Intel 4-wire fans.<br>11: Reserved. |
|-----|-----------|-----|--------|--|

S: Register default values are decided by trapping.

#### 8.6.2.28 Fan mode Select Register -- Index 96h

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-6 | Reserved  | R   | 0       | Reserved.   |
| 5-4 | FAN3_MODE | R/W | 1h      | 00: Reserved<br>01: Auto fan speed control, fan speed will follow different temperature by different <b>duty cycle</b> (voltage) that define in 0xB6-0xBE.<br>10: Reserved<br>11: Manual mode fan control, user can write expect <b>duty cycle</b> (PWM fan type) or voltage(linear fan type) to 0xC3, and F71883FG will output this value duty or voltage to control fan speed.    |
| 3-2 | FAN2_MODE | R/W | 1h      | 00: Reserved.<br>01: Auto fan speed control, fan speed will follow different temperature by different <b>duty cycle</b> (voltage) that define in 0xB6-0xBE.<br>10: Reserved.<br>11: Manual mode fan control, user can write expect <b>duty cycle</b> (PWM fan type) or voltage (linear fan type) to 0xB3, and F71883FG will output this value duty or voltage to control fan speed. |
| 1-0 | FAN1_MODE | R/W | 1h      | 00: Reserved.<br>01: Auto fan speed control, fan speed will follow different temperature by different <b>duty cycle</b> that define in 0xA6-0xAE.<br>10: Reserved.<br>11: Manual mode fan control, user can write expect <b>duty cycle</b> (PWM fan type) or voltage(linear fan type) to 0xA3, and F71883FG will output this value duty or voltage to control fan speed.            |

#### 8.6.2.29 Auto Fan1 and Fan2 Boundary Hystersis Select Register -- Index 98h

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-4 | FAN2_HYS | R/W | 4h      | 0000: Boundary hysteresis. (0~15 degree C)<br>Segment will change when the temperature over the boundary temperature and below the ( boundary – hysteresis ). |
| 3-0 | FAN1_HYS | R/W | 4h      | 0000: Boundary hysteresis. (0~15 degree C)<br>Segment will change when the temperature over the boundary temperature and below the ( boundary – hysteresis ). |

#### 8.6.2.30 Auto Fan3 and Fan4 Boundary Hystersis Select Register -- Index 99h

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-4 | Reserved | R   | 0       | Reserved.   |
| 3-0 | FAN3_HYS | R/W | 2h      | 0000: Boundary hysteresis. (0~15 degree C)<br>Segment will change when the temperature over the boundary temperature and below the ( boundary – hysteresis ). |

#### 8.6.2.31 Auto Fan3 and Fan4 Boundary Hystersis Select Register -- Index 9Bh

| Bit | Name     | R/W | Default | Description |
|-----|----------|-----|---------|-------------|
| 7-6 | Reserved | R   | 0       | Reserved.   |



|     |               |     |    |  |
|-----|---------------|-----|----|--|
| 5-4 | FAN3_RATE_SEL | R/W | 1h | Fan3 duty update rate:<br>00: 2Hz<br>01: 5Hz (default)<br>10: 10Hz<br>11: 20Hz |
| 3-2 | FAN2_RATE_SEL | R/W | 1h | Fan2 duty update rate:<br>00: 2Hz<br>01: 5Hz (default)<br>10: 10Hz<br>11: 20Hz |
| 1-0 | FAN1_RATE_SEL | R/W | 1h | Fan1 duty update rate:<br>00: 2Hz<br>01: 5Hz (default)<br>10: 10Hz<br>11: 20Hz |

**8.6.2.32 FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch**

| Bit | Name           | R/W | Default | Description   |
|-----|----------------|-----|---------|---|
| 7-4 | FAN2_STOP_DUTY | R/W | 5h      | When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4). |
| 3-0 | FAN1_STOP_DUTY | R/W | 5h      | When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4). |

**8.6.2.33 FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh**

| Bit | Name           | R/W | Default | Description   |
|-----|----------------|-----|---------|---|
| 7-4 | Reserved       | R   | 0       | Reserved.   |
| 3-0 | FAN3_STOP_DUTY | R/W | 5h      | When fan start, the FAN_CTRL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4). |

**8.6.2.34 Fan Fault Time Register -- Index 9Fh**

| Bit | Name          | R/W | Default | Description   |
|-----|---------------|-----|---------|---|
| 7-5 | Reserved      | --  | --      | Reservd   |
| 4   | FULL_DUTY_SEL | R/W | --      | 0: the full duty is 100%.<br>1: the full duty is 60% (default).<br>This register is power on trap by DTR1#. |
| 3-0 | Reserved      | R   | 0       | Reserved.   |

**Fan1 Index A0h- AFh**

| Address | Attribute | Default Value | Description |
|---------|-----------|---------------|-------------|
|---------|-----------|---------------|-------------|

|     |     |       |   |
|-----|-----|-------|---|
| A0h | RO  | 8'h0f | FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.            |
| A1h | RO  | 8'hff | FAN1 count reading (LSB).   |
| A2h | -   | -     | Reserved  |
| A3h | R/W | 8'h01 | The Value programming in this byte is duty value. In auto fan mode(CR96 bit5→0) this register is updated by hardware.<br>Ex: 5→ 5*100/255 %<br>255 → 100%   |
| A4h | R/W | 8'h03 | FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB. |
| A5h | R/W | 8'hff | FAN1 full speed count reading (LSB).  |

**8.6.2.35 VT1 BOUNDARY 1 TEMPERATURE – Index A6h**

| Bit | Name       | R/W | Default       | Description   |
|-----|------------|-----|---------------|---|
| 7   | Reserved   | RO  | 0             | Return 0 when read.   |
| 6-0 | BOUND1TMP1 | R/W | 3Ch<br>(60°C) | The 1 <sup>st</sup> BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is <b>exceed</b> this boundary, FAN1 expect value will load full speed duty 8'hFF. When VT1 temperature is <b>below</b> this boundary – hysteresis, FAN1 expect value will load from segment 1 register (index ABh). |

**8.6.2.36 VT1 BOUNDARY 2 TEMPERATURE – Index A9**

| Bit | Name       | R/W | Default       | Description   |
|-----|------------|-----|---------------|---|
| 7   | Reserved   | RO  | 0             | Return 0 when read.   |
| 6-0 | BOUND4TMP1 | R/W | 1Eh<br>(30°C) | The 2 <sup>st</sup> BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is <b>exceed</b> this boundary, FAN1 expect value will load from segment 1 register (index ABh). When VT1 temperature is <b>below</b> this boundary – hysteresis, FAN1 expect value will load from segment 2 register (index AEh). |

**8.6.2.37 FAN1 SEGMENT 1 SPEED COUNT – Index ABh**

| Bit | Name       | R/W | Default      | Description  |
|-----|------------|-----|--------------|--|
| 7-0 | SEC1SPEED1 | R/W | D9h<br>(85%) | The value that set in this byte is mean the expect PWM duty-cycle in this temperature section. |

**8.6.2.38 FAN1 SEGMENT 2 SPEED COUNT – Index AEh**

| Bit | Name       | R/W | Default      | Description  |
|-----|------------|-----|--------------|--|
| 7-0 | SEC2SPEED1 | R/W | 80h<br>(50%) | The value that set in this byte is mean the expect PWM duty-cycle in this temperature section. |

**8.6.2.39 FAN1 Temperature Mapping Select – Index AFh**

| Bit | Name         | R/W | Default | Description   |
|-----|--------------|-----|---------|---|
| 7-6 | Reserved     | --  | 0       | Reserved  |
| 5   | FAN1_UP_T_EN | R/W | 0       | Set 1 to force FAN1 to full speed if any temperature over its high limit. |

|     |                       |     |    |  |
|-----|-----------------------|-----|----|--|
| 4   | FAN1_INTERPOLATION_EN | R/W | 0  | Set 1 will enable the interpolation of the fan expect table.   |
| 3   | FAN1_JUMP_HIGH_EN     | R/W | 1  | This register controls the FAN1 duty movement when temperature over highest boundary.<br>0: The FAN1 duty will increases with the slope selected by FAN1_RATE_SEL register (Index 9Bh).<br>1: The FAN1 duty will directly jumps to full speed.                                       |
| 2   | FAN1_JUMP_LOW_EN      | R/W | 1  | This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis).<br>0: The FAN1 duty will decreases with the slope selected by FAN1_RATE_SEL register (Index 9Bh).<br>1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. |
| 1-0 | Fan1_temp_sel         | R/W | 1h | 0: reserved.<br>1: fan1 follow temperature 1.<br>2: fan1 follow temperature 2.<br>3: fan1 follow temperature 3.  |

**Fan2 Index B0h- BFh**

| Address | Attribute | Default Value | Description   |
|---------|-----------|---------------|---|
| B0h     | RO        | 8'h0f         | FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.            |
| B1h     | RO        | 8'hff         | FAN1 count reading (LSB).   |
| B2h     | R/W       | 8'h00         | Reserved  |
| B3h     | R/W       | 8'h01         | The Value programming in this byte is duty value. In auto fan mode(CR96 bit5→0) this register is updated by hardware.<br>Ex: 5→ 5*100/255 %<br>255 → 100%   |
| B4h     | R/W       | 8'h03         | FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB. |
| B5h     | R/W       | 8'hff         | FAN1 full speed count reading (LSB).  |

**8.6.2.40 VT2 BOUNDARY 1 TEMPERATURE – Index B6h**

| Bit | Name       | R/W | Default       | Description   |
|-----|------------|-----|---------------|---|
| 7   | Reserved   | RO  | 0             | Return 0 when read.   |
| 6-0 | BOUND1TMP2 | R/W | 3Ch<br>(60°C) | The 1 <sup>st</sup> BOUNDARY temperature for VT2 in temperature mode.<br>When VT2 temperature is <b>exceed</b> this boundary, FAN2 expect value will load full speed duty 8'hFF.<br>When VT2 temperature is <b>below</b> this boundary – hysteresis, FAN2 expect value will load from segment 1 register (index BBh). |

**8.6.2.41 VT2 BOUNDARY 2 TEMPERATURE – Index B9**

| Bit | Name     | R/W | Default | Description         |
|-----|----------|-----|---------|---------------------|
| 7   | Reserved | RO  | 0       | Return 0 when read. |

|     |            |     |               |   |
|-----|------------|-----|---------------|---|
| 6-0 | BOUND2TMP1 | R/W | 1Eh<br>(30°C) | The 2 <sup>st</sup> BOUNDARY temperature for VT1 in temperature mode.<br>When VT1 temperature is <b>exceed</b> this boundary, FAN1 expect value will load from segment 1 register (index BBh).<br>When VT1 temperature is <b>below</b> this boundary – hysteresis, FAN1 expect value will load from segment 2 register (index BEh). |
|-----|------------|-----|---------------|---|

**8.6.2.42 FAN2 SEGMENT 1 SPEED COUNT – Index BBh**

| Bit | Name       | R/W | Default      | Description  |
|-----|------------|-----|--------------|--|
| 7-0 | SEC1SPEED2 | R/W | D9h<br>(85%) | The value that set in this byte is mean the expect PWM duty-cycle in this temperature section. |

**8.6.2.43 FAN2 SEGMENT 2 SPEED COUNT – Index BEh**

| Bit | Name       | R/W | Default      | Description  |
|-----|------------|-----|--------------|--|
| 7-0 | SEC2SPEED2 | R/W | 80h<br>(50%) | The value that set in this byte is mean the expect PWM duty-cycle in this temperature section. |

**8.6.2.44 FAN2 Temperature Mapping Select – Index BFh**

| Bit | Name                  | R/W | Default | Description  |
|-----|-----------------------|-----|---------|--|
| 7-6 | Reserved              | --  | 0       | Reserved   |
| 5   | FAN2_UP_T_EN          | R/W | 0       | Set 1 to force FAN2 to full speed if any temperature over its high limit.  |
| 4   | FAN2_INTERPOLATION_EN | R/W | 0       | Set 1 will enable the interpolation of the fan expect table.   |
| 3   | FAN2_JUMP_HIGH_EN     | R/W | 1       | This register controls the FAN2 duty movement when temperature over highest boundary.<br>0: The FAN2 duty will increases with the slope selected by FAN2_RATE_SEL register (Index 9Bh).<br>1: The FAN2 duty will directly jumps to full speed.                                       |
| 2   | FAN2_JUMP_LOW_EN      | R/W | 1       | This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis).<br>0: The FAN2 duty will decreases with the slope selected by FAN2_RATE_SEL register (Index 9Bh).<br>1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. |
| 1-0 | Fan2_temp_sel         | R/W | 2h      | 0: reserved.<br>1: fan2 follow temperature 1.<br>2: fan2 follow temperature 2.<br>3: fan2 follow temperature 3.  |

**Fan3 Index C0h- CFh**

| Address | Attribute | Default Value | Description  |
|---------|-----------|---------------|--|
| C0h     | RO        | 8'h0F         | FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB. |
| C1h     | RO        | 8'hff         | FAN3 count reading (LSB).  |
| C2h     | -         | -             | Reserved.  |

|     |     |       |   |
|-----|-----|-------|---|
| C3h | R/W | 8'h01 | The Value programming in this byte is duty value. In auto fan mode(CR96 bit5→0) this register is updated by hardware.<br>Ex: 5→ 5*100/255 %<br>255 → 100%   |
| C4h | R/W | 8'h03 | FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB. |
| C5h | R/W | 8'hff | FAN3 full speed count reading (LSB).  |

**8.6.2.45 VT3 BOUNDARY 1 TEMPERATURE – Index C6h**

| Bit | Name       | R/W | Default       | Description   |
|-----|------------|-----|---------------|---|
| 7   | Reserved   | RO  | 0             | Return 0 when read.   |
| 6-0 | BOUND1TMP3 | R/W | 3Ch<br>(60°C) | The 1 <sup>st</sup> BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is <b>exceed</b> this boundary, FAN3 expect value will load the full speed duty 8'hFF. When VT3 temperature is <b>below</b> this boundary – hysteresis, FAN3 expect value will load from segment 1 register (index CBh). |

**8.6.2.46 VT3 BOUNDARY 2 TEMPERATURE – Index C9**

| Bit | Name       | R/W | Default       | Description   |
|-----|------------|-----|---------------|---|
| 7   | Reserved   | RO  | 0             | Return 0 when read.   |
| 6-0 | BOUND2TMP3 | R/W | 1Eh<br>(30°C) | The 2 <sup>st</sup> BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is <b>exceed</b> this boundary, FAN3 expect value will load from segment 1 register (index CBh). When VT3 temperature is <b>below</b> this boundary – hysteresis, FAN3 expect value will load from segment 2 register (index CEh). |

**8.6.2.47 FAN3 SEGMENT 1 SPEED COUNT – Index CBh**

| Bit | Name       | R/W | Default      | Description  |
|-----|------------|-----|--------------|--|
| 7-0 | SEC1SPEED3 | R/W | D9h<br>(85%) | The value that set in this byte is mean the expect PWM duty-cycle in this temperature section. |

**8.6.2.48 FAN3 SEGMENT 2 SPEED COUNT – Index CEh**

| Bit | Name       | R/W | Default      | Description  |
|-----|------------|-----|--------------|--|
| 7-0 | SEC2SPEED3 | R/W | 80h<br>(50%) | The value that set in this byte is mean the expect PWM duty-cycle in this temperature section. |

**8.6.2.49 FAN3 Temperature Mapping Select – Index CFh**

| Bit | Name                  | R/W | Default | Description  |
|-----|-----------------------|-----|---------|--|
| 7-6 | Reserved              | --  | 0       | Reserved   |
| 5   | FAN3_UP_T_EN          | R/W | 0       | Set 1 to force FAN3 to full speed if any temperature over its high limit.  |
| 4   | FAN3_INTERPOLATION_EN | R/W | 0       | Set 1 will enable the interpolation of the fan expect table.   |
| 3   | FAN3_JUMP_HIGH_EN     | R/W | 1       | This register controls the FAN3 duty movement when temperature over highest boundary.<br>0: The FAN3 duty will increases with the slope selected by FAN3_RATE_SEL register (Index 9Bh).<br>1: The FAN3 duty will directly jumps to full speed. |

|     |                  |     |    |   |
|-----|------------------|-----|----|---|
| 2   | FAN3_JUMP_LOW_EN | R/W | 1  | <p>This register controls the FAN3 duty movement when temperature under (highest boundary – hysteresis).</p> <p>0: The FAN3 duty will decreases with the slope selected by FAN3_RATE_SEL register (Index 9Bh).</p> <p>1: The FAN3 duty will directly jumps to the value of SEC1SPEED3 register.</p> |
| 1-0 | Fan3_temp_sel    | R/W | 3h | <p>0: reserved.</p> <p>1: fan3 follow temperature 1.</p> <p>2: fan3 follow temperature 2.</p> <p>3: fan3 follow temperature 3.</p>  |

## 8.7 KBC Registers (CR05)

### 8.7.1 KBC Configuration Registers

#### KBC Device Enable Register — Index 30h

| Bit | Name     | R/W | Default | Description                       |
|-----|----------|-----|---------|-----------------------------------|
| 7-1 | Reserved | -   | -       | Reserved                          |
| 0   | KBC_EN   | R/W | 1       | 0: disable KBC.<br>1: enable KBC. |

#### Base Address High Register — Index 60h

| Bit | Name         | R/W | Default | Description  |
|-----|--------------|-----|---------|--|
| 7-0 | BASE_ADDR_HI | R/W | 00h     | The MSB of KBC command port address. The address of data port is command port address + 4; |

#### Base Address Low Register — Index 61h

| Bit | Name         | R/W | Default | Description  |
|-----|--------------|-----|---------|--|
| 7-0 | BASE_ADDR_LO | R/W | 60h     | The LSB of KBC command port address. The address of data port is command port address + 4. |

#### KB IRQ Channel Select Register — Index 70h

| Bit | Name     | R/W | Default | Description                                    |
|-----|----------|-----|---------|--|
| 7-4 | Reserved | -   | -       | Reserved.                                      |
| 3-0 | SELKIRQ  | R/W | 0h      | Select the IRQ channel for keyboard interrupt. |

#### Mouse IRQ Channel Select Register — Index 72h

| Bit | Name     | R/W | Default | Description                                      |
|-----|----------|-----|---------|--|
| 7-4 | Reserved | -   | -       | Reserved.  |
| 3-0 | SELMIRQ  | R/W | 0h      | Select the IRQ channel for PS/2 mouse interrupt. |

## 8.8 GPIO Registers (CR06)

### 8.8.1 GPIO0 Registers

#### GPIO0 Output Enable Register — Index F0h

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-4 | Reserved  | -   | 0       | Reserved  |
| 3   | GPIO03_OE | R/W | 0       | 0: GPIO03 is in input mode.<br>1: GPIO03 is in output mode. |
| 2   | GPIO02_OE | R/W | 0       | 0: GPIO02 is in input mode.<br>1: GPIO02 is in output mode. |
| 1   | Reserved  | R/W | 0       | Reserved  |
| 0   | Reserved  | R/W | 0       | Reserved  |

#### GPIO0 Output Data Register — Index F1h

| Bit | Name       | R/W | Default | Description  |
|-----|------------|-----|---------|--|
| 7-4 | Reserved   | -   | 0       | Reserved   |
| 3   | GPIO03_VAL | R/W | 1       | 0: GPIO03 outputs 0 when in output mode.<br>1: GPIO03 outputs 1 when in output mode. |
| 2   | GPIO02_VAL | R/W | 1       | 0: GPIO02 outputs 0 when in output mode.<br>1: GPIO02 outputs 1 when in output mode. |
| 1   | Reserved   | R/W | 1       | Reserved   |
| 0   | Reserved   | R/W | 1       | Reserved   |

#### GPIO0 Pin Status Register — Index F2h

| Bit | Name      | R/W | Default | Description                        |
|-----|-----------|-----|---------|------------------------------------|
| 7-4 | Reserved  | -   | 0       | Reserved                           |
| 3   | GPIO03_IN | R   | -       | The pin status of GPIO03/WDTRST#.  |
| 2   | GPIO02_IN | R   | -       | The pin status of SLOTOCC#/GPIO02. |
| 1   | Reserved  | R   | -       | Reserved                           |
| 0   | Reserved  | R   | -       | Reserved                           |

#### GPIO0 Drive Enable Register — Index F3h

| Bit | Name          | R/W | Default | Description   |
|-----|---------------|-----|---------|---|
| 7-4 | Reserved      | -   | 0       | Reserved  |
| 3   | GPIO03_DRV_EN | R/W | 0       | 0: GPIO03 is open drain in output mode.<br>1: GPIO03 is push pull in output mode. |
| 2   | GPIO02_DRV_EN | R/W | 0       | 0: GPIO02 is open drain in output mode.<br>1: GPIO02 is push pull in output mode. |
| 1   | Reserved      | R/W | 0       | Reserved  |
| 0   | Reserved      | R/W | 0       | Reserved  |



**8.8.2 GPIO1 Registers**
**GPIO1 Output Enable Register — Index E0h**

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7   | Reserved  | R/W | 0       | Reserved  |
| 6   | GPIO16_OE | R/W | 0       | 0: GPIO16 is in input mode.<br>1: GPIO16 is in output mode. |
| 5   | GPIO15_OE | R/W | 0       | 0: GPIO15 is in input mode.<br>1: GPIO15 is in output mode. |
| 4   | GPIO14_OE | R/W | 0       | 0: GPIO14 is in input mode.<br>1: GPIO14 is in output mode. |
| 3   | GPIO13_OE | R/W | 0       | 0: GPIO13 is in input mode.<br>1: GPIO13 is in output mode. |
| 2   | GPIO12_OE | R/W | 0       | 0: GPIO12 is in input mode.<br>1: GPIO12 is in output mode. |
| 1   | GPIO11_OE | R/W | 0       | 0: GPIO11 is in input mode.<br>1: GPIO11 is in output mode. |
| 0   | GPIO10_OE | R/W | 0       | 0: GPIO10 is in input mode.<br>1: GPIO10 is in output mode. |

**GPIO1 Output Data Register — Index E1h**

| Bit | Name       | R/W | Default | Description  |
|-----|------------|-----|---------|--|
| 7   | Reserved   | R/W | 1       | Reserved   |
| 6   | GPIO16_VAL | R/W | 1       | 0: GPIO16 outputs 0 when in output mode.<br>1: GPIO16 outputs 1 when in output mode. |
| 5   | GPIO15_VAL | R/W | 1       | 0: GPIO15 outputs 0 when in output mode.<br>1: GPIO15 outputs 1 when in output mode. |
| 4   | GPIO14_VAL | R/W | 1       | 0: GPIO14 outputs 0 when in output mode.<br>1: GPIO14 outputs 1 when in output mode. |
| 3   | GPIO13_VAL | R/W | 1       | 0: GPIO13 outputs 0 when in output mode.<br>1: GPIO13 outputs 1 when in output mode. |
| 2   | GPIO12_VAL | R/W | 1       | 0: GPIO12 outputs 0 when in output mode.<br>1: GPIO12 outputs 1 when in output mode. |
| 1   | GPIO11_VAL | R/W | 1       | 0: GPIO11 outputs 0 when in output mode.<br>1: GPIO11 outputs 1 when in output mode. |
| 0   | GPIO10_VAL | R/W | 1       | 0: GPIO10 outputs 0 when in output mode.<br>1: GPIO10 outputs 1 when in output mode. |

**GPIO1 Pin Status Register — Index E2h**

| Bit | Name      | R/W | Default | Description  |
|-----|-----------|-----|---------|--|
| 7   | Reserved  | R   | -       | Reserved   |
| 6   | GPIO16_IN | R   | -       | The pin status of GPIO16/LED_VCC                   |
| 5   | GPIO15_IN | R   | -       | The pin status of GPIO15/LED_VSB/ALERT#.           |
| 4   | GPIO14_IN | R   | -       | The pin status of GPIO14/FWH_DIS/WDTRST#/SPI_CS1#. |
| 3   | GPIO13_IN | R   | -       | The pin status of GPIO13/SPI_MOSI/BEEP.            |

|   |           |   |   |   |
|---|-----------|---|---|---|
| 2 | GPIO12_IN | R | - | The pin status of GPIO12/SPI_MISO/FANCTRL1_1. |
| 1 | GPIO11_IN | R | - | The pin status of GPIO11/SPI_CS.              |
| 0 | GPIO10_IN | R | - | The pin status of GPIO10/SPI_CLK.             |

**GPIO1 Drive Enable Register — Index E3h**

| Bit | Name          | R/W | Default | Description   |
|-----|---------------|-----|---------|---|
| 7   | Reserved      | R/W | 0       | Reserved  |
| 6   | GPIO16_DRV_EN | R/W | 0       | 0: GPIO16 is open drain in output mode.<br>1: GPIO16 is push pull in output mode. |
| 5   | GPIO15_DRV_EN | R/W | 0       | 0: GPIO15 is open drain in output mode.<br>1: GPIO15 is push pull in output mode. |
| 4   | GPIO14_DRV_EN | R/W | 0       | 0: GPIO14 is open drain in output mode.<br>1: GPIO14 is push pull in output mode. |
| 3   | GPIO13_DRV_EN | R/W | 0       | 0: GPIO13 is open drain in output mode.<br>1: GPIO13 is push pull in output mode. |
| 2   | GPIO12_DRV_EN | R/W | 0       | 0: GPIO12 is open drain in output mode.<br>1: GPIO12 is push pull in output mode. |
| 1   | GPIO11_DRV_EN | R/W | 0       | 0: GPIO11 is open drain in output mode.<br>1: GPIO11 is push pull in output mode. |
| 0   | GPIO10_DRV_EN | R/W | 0       | 0: GPIO10 is open drain in output mode.<br>1: GPIO10 is push pull in output mode. |

**8.8.3 GPIO2 Registers**
**GPIO2 Output Enable Register — Index D0h**

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7   | GPIO27_OE | R/W | 0       | 0: GPIO27 is in input mode.<br>1: GPIO27 is in output mode. |
| 6   | GPIO26_OE | R/W | 0       | 0: GPIO26 is in input mode.<br>1: GPIO26 is in output mode. |
| 5   | GPIO25_OE | R/W | 0       | 0: GPIO25 is in input mode.<br>1: GPIO25 is in output mode. |
| 4   | GPIO24_OE | R/W | 0       | 0: GPIO24 is in input mode.<br>1: GPIO24 is in output mode. |
| 3   | Reserved  | R/W | 0       | Reserved  |
| 2   | GPIO22_OE | R/W | 0       | 0: GPIO22 is in input mode.<br>1: GPIO22 is in output mode. |
| 1   | GPIO21_OE | R/W | 0       | 0: GPIO21 is in input mode.<br>1: GPIO21 is in output mode. |
| 0   | GPIO20_OE | R/W | 0       | 0: GPIO20 is in input mode.<br>1: GPIO20 is in output mode. |

**GPIO2 Output Data Register — Index D1h**

| Bit | Name | R/W | Default | Description |
|-----|------|-----|---------|-------------|
|-----|------|-----|---------|-------------|

|   |            |     |   |  |
|---|------------|-----|---|--|
| 7 | GPIO27_VAL | R/W | 1 | 0: GPIO27 outputs 0 when in output mode.<br>1: GPIO27 outputs1 when in output mode.  |
| 6 | GPIO26_VAL | R/W | 1 | 0: GPIO26 outputs 0 when in output mode.<br>1: GPIO26 outputs1 when in output mode.  |
| 5 | GPIO25_VAL | R/W | 1 | 0: GPIO25 outputs 0 when in output mode.<br>1: GPIO25 outputs 1 when in output mode. |
| 4 | GPIO24_VAL | R/W | 1 | 0: GPIO24 outputs 0 when in output mode.<br>1: GPIO24 outputs 1 when in output mode. |
| 3 | Reserved   | R/W | 1 | Reserved   |
| 2 | GPIO22_VAL | R/W | 1 | 0: GPIO22 outputs 0 when in output mode.<br>1: GPIO22 outputs 1 when in output mode. |
| 1 | GPIO21_VAL | R/W | 1 | 0: GPIO21 outputs 0 when in output mode.<br>1: GPIO21 outputs 1 when in output mode. |
| 0 | GPIO20_VAL | R/W | 1 | 0: GPIO20 outputs 0 when in output mode.<br>1: GPIO20 outputs 1 when in output mode. |

**GPIO2 Pin Status Register — Index D2h**

| Bit | Name      | R/W | Default | Description                        |
|-----|-----------|-----|---------|------------------------------------|
| 7   | GPIO27_IN | R   | -       | The pin status of PWSOUT#/GPIO27.  |
| 6   | GPIO26_IN | R   | -       | The pin status of PWSIN#/GPIO26.   |
| 5   | GPIO25_IN | R   | -       | The pin status of PME#/GPIO25.     |
| 4   | GPIO24_IN | R   | -       | The pin status of ATXPG_IN/GPIO24. |
| 3   | Reserved  | R   | -       | Reserved                           |
| 2   | GPIO22_IN | R   | -       | The pin status of PCIRST3#/GPIO22. |
| 1   | GPIO21_IN | R   | -       | The pin status of PCIRST2#/GPIO21. |
| 0   | GPIO20_IN | R   | -       | The pin status of PCIRST1#/GPIO20. |

**GPIO2 Drive Enable Register — Index D3h**

| Bit | Name          | R/W | Default | Description   |
|-----|---------------|-----|---------|---|
| 7   | GPIO27_DRV_EN | R/W | 0       | 0: GPIO27 is open drain in output mode.<br>1: GPIO27 is push pull in output mode. |
| 6   | GPIO26_DRV_EN | R/W | 0       | 0: GPIO26 is open drain in output mode.<br>1: GPIO26 is push pull in output mode. |
| 5   | GPIO25_DRV_EN | R/W | 0       | 0: GPIO25 is open drain in output mode.<br>1: GPIO25 is push pull in output mode. |
| 4   | GPIO24_DRV_EN | R/W | 0       | 0: GPIO24 is open drain in output mode.<br>1: GPIO24 is push pull in output mode. |
| 3   | Reserved      | R/W | 0       | Reserved  |
| 2   | GPIO22_DRV_EN | R/W | 0       | 0: GPIO22 is open drain in output mode.<br>1: GPIO22 is push pull in output mode. |
| 1   | GPIO21_DRV_EN | R/W | 0       | 0: GPIO21 is open drain in output mode.<br>1: GPIO21 is push pull in output mode. |
| 0   | GPIO20_DRV_EN | R/W | 0       | 0: GPIO20 is open drain in output mode.<br>1: GPIO20 is push pull in output mode. |

**8.8.4 GPIO3 Registers**
**GPIO3 Output Enable Register — Index C0h**

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-4 | Reserved  | -   | -       | Reserved.   |
| 3   | GPIO33_OE | R/W | 0       | 0: GPIO33 is in input mode.<br>1: GPIO33 is in output mode. |
| 2   | GPIO32_OE | R/W | 0       | 0: GPIO32 is in input mode.<br>1: GPIO32 is in output mode. |
| 1   | GPIO31_OE | R/W | 0       | 0: GPIO31 is in input mode.<br>1: GPIO31 is in output mode. |
| 0   | GPIO30_OE | R/W | 0       | 0: GPIO30 is in input mode.<br>1: GPIO30 is in output mode. |

**GPIO3 Output Data Register — Index C1h**

| Bit | Name       | R/W | Default | Description  |
|-----|------------|-----|---------|--|
| 7-4 | Reserved   | -   | -       | Reserved.  |
| 3   | GPIO33_VAL | R/W | 1       | 0: GPIO33 outputs 0 when in output mode.<br>1: GPIO33 outputs 1 when in output mode. |
| 2   | GPIO32_VAL | R/W | 1       | 0: GPIO32 outputs 0 when in output mode.<br>1: GPIO32 outputs 1 when in output mode. |
| 1   | GPIO31_VAL | R/W | 1       | 0: GPIO31 outputs 0 when in output mode.<br>1: GPIO31 outputs 1 when in output mode. |
| 0   | GPIO30_VAL | R/W | 1       | 0: GPIO30 outputs 0 when in output mode.<br>1: GPIO30 outputs 1 when in output mode. |

**GPIO3 Pin Status Register — Index C2h**

| Bit | Name      | R/W | Default | Description                       |
|-----|-----------|-----|---------|-----------------------------------|
| 7-4 | Reserved  | -   | -       | Reserved.                         |
| 3   | GPIO33_IN | R   | -       | The pin status of RSMRST#/GPIO33. |
| 2   | GPIO32_IN | R   | -       | The pin status of PWROK/GPIO32.   |
| 1   | GPIO31_IN | R   | -       | The pin status of PS_ON#/GPIO31.  |
| 0   | GPIO30_IN | R   | -       | The pin status of S3#/GPIO30.     |

**GPIO3 Drive Enable Register — Index C3h**

| Bit | Name          | R/W | Default | Description   |
|-----|---------------|-----|---------|---|
| 7-4 | Reserved      | -   | -       | Reserved.   |
| 3   | GPIO33_DRV_EN | R/W | 0       | 0: GPIO33 is open drain in output mode.<br>1: GPIO33 is push pull in output mode. |
| 2   | GPIO32_DRV_EN | R/W | 0       | 0: GPIO32 is open drain in output mode.<br>1: GPIO32 is push pull in output mode. |
| 1   | GPIO31_DRV_EN | R/W | 0       | 0: GPIO31 is open drain in output mode.<br>1: GPIO31 is push pull in output mode. |

|   |               |     |   |   |
|---|---------------|-----|---|---|
| 0 | GPIO30_DRV_EN | R/W | 0 | 0: GPIO30 is open drain in output mode.<br>1: GPIO30 is push pull in output mode. |
|---|---------------|-----|---|---|

### 8.8.5 GPIO4 Registers

#### GPIO4 Output Enable Register — Index B0h

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-4 | Reserved  | -   | -       | Reserved.   |
| 3   | GPIO43_OE | R/W | 0       | 0: GPIO43 is in input mode.<br>1: GPIO43 is in output mode. |
| 2   | GPIO42_OE | R/W | 0       | 0: GPIO42 is in input mode.<br>1: GPIO42 is in output mode. |
| 1   | GPIO41_OE | R/W | 0       | 0: GPIO41 is in input mode.<br>1: GPIO41 is in output mode. |
| 0   | GPIO40_OE | R/W | 0       | 0: GPIO40 is in input mode.<br>1: GPIO40 is in output mode. |

#### GPIO4 Output Data Register — Index B1h

| Bit | Name       | R/W | Default | Description  |
|-----|------------|-----|---------|--|
| 7-4 | Reserved   | -   | -       | Reserved.  |
| 3   | GPIO43_VAL | R/W | 1       | 0: GPIO43 outputs 0 when in output mode.<br>1: GPIO43 outputs 1 when in output mode. |
| 2   | GPIO42_VAL | R/W | 1       | 0: GPIO42 outputs 0 when in output mode.<br>1: GPIO42 outputs 1 when in output mode. |
| 1   | GPIO41_VAL | R/W | 1       | 0: GPIO41 outputs 0 when in output mode.<br>1: GPIO41 outputs 1 when in output mode. |
| 0   | GPIO40_VAL | R/W | 1       | 0: GPIO40 outputs 0 when in output mode.<br>1: GPIO40 outputs 1 when in output mode. |

#### GPIO4 Pin Status Register — Index B2h

| Bit | Name      | R/W | Default | Description                        |
|-----|-----------|-----|---------|------------------------------------|
| 7-4 | Reserved  | -   | -       | Reserved.                          |
| 3   | GPIO43_IN | R   | -       | The pin status of IRRX/GPIO43      |
| 2   | GPIO42_IN | R   | -       | The pin status of IRTX/GPIO42.     |
| 1   | GPIO41_IN | R   | -       | The pin status of FANCTRL3/GPIO41. |
| 0   | GPIO40_IN | R   | -       | The pin status of FANIN3/GPIO40.   |

#### GPIO4 Drive Enable Register — Index B3h

| Bit | Name          | R/W | Default | Description   |
|-----|---------------|-----|---------|---|
| 7-4 | Reserved      | -   | -       | Reserved.   |
| 3   | GPIO43_DRV_EN | R/W | 0       | 0: GPIO43 is open drain in output mode.<br>1: GPIO43 is push-pull in output mode. |
| 2   | GPIO42_DRV_EN | R/W | 0       | 0: GPIO42 is open drain in output mode.<br>1: GPIO42 is push-pull in output mode. |

|   |               |     |   |   |
|---|---------------|-----|---|---|
| 1 | GPIO41_DRV_EN | R/W | 0 | 0: GPIO41 is open drain in output mode.<br>1: GPIO41 is push-pull in output mode. |
| 0 | GPIO40_DRV_EN | R/W | 0 | 0: GPIO40 is open drain in output mode.<br>1: GPIO40 is push-pull in output mode. |

## 8.9 VID Registers (CR07)

### 8.9.1 VID Configuration Registers

#### VID Device Enable Register — Index 30h

| Bit | Name     | R/W | Default | Description                       |
|-----|----------|-----|---------|-----------------------------------|
| 7-1 | Reserved | -   | 0       | Reserved                          |
| 0   | VID_EN   | R/W | 0       | 0: disable VID.<br>1: enable VID. |

#### Base Address High Register — Index 60h

| Bit | Name         | R/W | Default | Description                  |
|-----|--------------|-----|---------|------------------------------|
| 7-0 | BASE_ADDR_HI | R/W | 00h     | The MSB of VID base address. |

#### Base Address Low Register — Index 61h

| Bit | Name         | R/W | Default | Description                  |
|-----|--------------|-----|---------|------------------------------|
| 7-0 | BASE_ADDR_LO | R/W | 00h     | The LSB of VID base address. |

### 8.9.2 Device Registers

#### 8.9.2.1 Configuration Register — Index 00h (\* cleared by slotocc\_n and watch dog timeout)

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7   | WDOUT_EN  | R/W | 0       | If this bit is set to 1 and watchdog timeout event occurs, WDTRST# output is enabled. |
| 6-3 | Reserved  | -   | 0       | Return 0 when read.   |
| 2*  | OTF_EN    | R/W | 0       | This bit is used to enable vid on-the-fly function.                                   |
| 1:0 | Dummy Reg | R/W | 0       | Dummy register.   |

#### 8.9.2.2 VID Offset Register 0 — Index 01h

| Bit | Name       | R/W | Default | Description                            |
|-----|------------|-----|---------|--|
| 7:4 | Reserved   | R   | -       | Reserved                               |
| 3-0 | VID_OFFSET | R/W | 0       | VID offset. VID_OFFSET[3] is sign bit. |

#### 8.9.2.3 VID Manual Register — Index 02h

| Bit | Name        | R/W | Default | Description  |
|-----|-------------|-----|---------|--|
| 7*  | MANUAL_MODE | R/W | 0       | If this bit is set to 1 and OTF_EN is 0, VIDOUT will be VID_MANUAL |
| 6   | KEY_OK      | R   | -       | This bit is 1 represents that the serial key is entered correctly. |
| 5-4 | Reserved    | R   | -       | Return 0 when read.  |
| 3-0 | VID_MANUAL  | R/W | 0       | Manually assigned VIDOUT value                                     |

#### 8.9.2.4 Serial Key Data Register — Index 03h

| Bit | Name | R/W | Default | Description |
|-----|------|-----|---------|-------------|
|-----|------|-----|---------|-------------|

|     |          |     |   |   |
|-----|----------|-----|---|---|
| 7-0 | KEY_DATA | R/W | 0 | Write serial data to this register correctly, the KEY_OK bit will be set to 1. Hence, users are able to write key protected registers. The sequence to enable KEY_OK is 0x32, 0x5D, 0x42, 0xAC. When KEY_OK is set, write this register 0x35 will clear KEY_OK. |
|-----|----------|-----|---|---|

**8.9.2.5 VIDIN Register — Index 04h (\* cleared by slotcc\_n and watch dog timeout)**

| Bit | Name     | R/W | Default | Description               |
|-----|----------|-----|---------|---------------------------|
| 7-4 | Reserved | R   | 0       | Reserved                  |
| 3-0 | VID_IN   | R   | -       | Return the VID_IN status. |

**8.9.2.6 Watchdog Timer Configuration Register 1— Index 05h**

| Bit | Name        | R/W | Default | Description  |
|-----|-------------|-----|---------|--|
| 7   | Reserved    | R   | 0       | Reserved   |
| 6   | WDTMOUT_STS | R/W | 0       | If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.                 |
| 5   | WD_EN       | R/W | 0       | If this bit is set to 1, the counting of watchdog time is enabled.   |
| 4   | WD_PULSE    | R/W | 0       | Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.  |
| 3   | WD_UNIT     | R/W | 0       | Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.   |
| 2   | WD_HACTIVE  | R/W | 0       | Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.                                 |
| 1:0 | WD_PSWIDTH  | R/W | 0       | Select output pulse width of RSTOUT#<br>0: 1 ms                      1: 25 ms<br>2: 125 ms                    3: 5 sec |

**8.9.2.7 Watchdog Timer Configuration Register 2 — Index 06h**

| Bit | Name    | R/W | Default | Description            |
|-----|---------|-----|---------|------------------------|
| 7:0 | WD_TIME | R/W | 0       | Time of watchdog timer |

**8.9.2.8 Output Voltage Control Register 1 — Index 07h (\* cleared by slotcc\_n and watch dog timeout)**

| Bit | Name        | R/W | Default | Description  |
|-----|-------------|-----|---------|--|
| 7-6 | Dummy Reg   | R/W | 0       | Dummy register.  |
| 5   | REG_RST_SEL | R/W | 0       | 0: The VID registers is reseted when VDD power lose and watch dog timeout.<br>1: The VID registers is reseted by slotcc_n and watch dog timeout. |
| 4   | Reserved    | R/W | 0       | Reserved   |
| 3-0 | Dummy Reg   | R/W | 0       | Dummy registers.   |



## 8.10 SPI Registers (CR08)

### 8.10.1 Configuration Register SPI Control Register — Index F0h

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-6 | Reserved | -   | -       | Reserved.  |
| 5   | SPTIE    | R/W | 0       | SPI interrupt enable. Set to 1, SPIE interrupt enabled, set to 0 SPIE interrupt disabled.  |
| 4   | MSTR     | R/W | 1       | Master mode select. Set to 1, SPI function is master mode; set to 0 is disable SPI function  |
| 3   | CPOL     | R/W | 0       | Clock polarity this bit selects inverted or non-inverted SPI clock. Set to 1, active low clock selected; SCK idles high. Set to 0, active high clock selected; SCK idles low.  |
| 2   | CPHA     | R/W | 0       | Clock phase. This bit is used to shift the SCK serial clock. Set to 1, the first SCK edge is issued at the beginning of the transfer operation. Set to 0, the first SCK edge is issued one-half cycle into the transfer operation. |
| 1   | Reserved | -   | 0       | Reserved   |
| 0   | LSBFE    | R/W | 0       | This bit control data shift from lsb or msb. Set to 1, data is transferred from lsb to msb. Set to 0, data is transferred from msb to lsb.   |

### SPI Timeout Register — Index F1h

| Bit | Name      | R/W | Default | Description  |
|-----|-----------|-----|---------|--|
| 7-0 | TIMER_VAL | R/W | 8'h04   | The time in second to assert FWH_DIS signal when SPI is used as backup BIOS. |

### SPI Baud Rate Divisor Register — Index F2h

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-3 | Reserved | -   | 0       | Reserved   |
| 2-0 | BAUD_VAL | R/W | 1       | This register decides to SCK frequency. Baud rate divisor equation is $33\text{MHz}/2^*(\text{BAUD\_VAL})$ .<br>00: 33MHz.<br>01: 16.7MHz. |

### SPI Status Register — Index F3h

| Bit | Name           | R/W | Default | Description   |
|-----|----------------|-----|---------|---|
| 7   | SPIE           | R/W | 0       | SPI interrupt status. When SPI is transferred or received data from device finish, this bit will be set. Write 1 to clear this bit.   |
| 6   | FWH_DIS        | R/W | -       | When SPI is used as backup BIOS, this bit will set when time in second reaches the value programmed in TIMER_VAL (CRF1). Write one to clear this register.<br>When SPI is used as primary BIOS, this register will always be 1.   |
| 5   | SPE            | R   | -       | This bit reflects the SPI_EN register. (which will be 1 when SPI is enabled.)   |
| 4   | SPIO_TIMER_DIS | R/W | -       | When SPI is used as primary BIOS, it will also have backup function as used in backup BIOS. The bit will set to 1 when the time in second reaches the value programmed in TIMER_VAL (CRF1). That is the first SPI could not function well. Then a reset signal will asserted and reboot the system with the second SPI. (I could be another SPI with chip-selected by FWH_DIS or another 4Mbits of an 8Mbits SPI. The SPI_CS1_EN (CR2D[4]) determines the method). Write one to clear this bit. |

|     |          |   |   |  |
|-----|----------|---|---|--|
| 3   | SPTEF    | R | 0 | SPI operation status. When SPI is transferred or received data from device, this bit will be set 1, Clear by SPI operation finish. |
| 2-0 | Reserved | - | - | Reserved   |

**SPI High Byte Data Register — Index F4h**

| Bit | Name   | R/W | Default | Description  |
|-----|--------|-----|---------|--|
| 7-0 | H_DATA | R   | 0       | When SPI is received 16 bits data from device. This register saves high byte data. |

**SPI command data Register — Index F5h**

| Bit | Name     | R/W | Default | Description   |
|-----|----------|-----|---------|---|
| 7-0 | CMD_DATA | R/W | 0       | This register provides command value for flash command. |

**SPI chip select Register — Index F6h**

| Bit | Name      | R/W | Default | Description                       |
|-----|-----------|-----|---------|-----------------------------------|
| 7-4 | Reserved  | -   | -       | Reserved                          |
| 3   | Dummy_Reg | R/W | 0       | Dummy register.                   |
| 2   | Dummy_Reg | R/W | 0       | Dummy register.                   |
| 1   | Dummy_Reg | R/W | 0       | Dummy register.                   |
| 0   | CS0       | R/W | 0       | Chip select 0. To select device 0 |

**SPI memory mapping Register — Index F7h**

| Bit | Name     | R/W | Default | Description  |
|-----|----------|-----|---------|--|
| 7-3 | Reserved | -   | 0       | Reserved   |
| 2-0 | Mem_map  | R/W | -       | This register decides memory size.<br>3'b000: one of the memory sizes is 512k bytes.<br>3'b001: one of the memory sizes is 1024k bytes.<br>3'b100: one of the memory sizes is 2048k bytes.<br>3'b011: one of the memory sizes is 4096k bytes.<br>3'b100: one of the memory sizes if 8092k bytes. |

**SPI operate Register — Index F8h**

| Bit | Name         | R/W | Default | Description  |
|-----|--------------|-----|---------|--|
| 7   | TYPE         | R/W | 0       | This bit decide flash continuous programming mode. Set to 1, if programming continuous mode is same as the SST flash. Set to 0 if programming continuous mode is same as the ATMEL flash |
| 6   | IO_SPI       | R/W | 0       | This bit control SPI function transfer 8 bit command to device. Clear 0 by operation finish.   |
| 5   | RDSR         | R/W | 0       | This bit control SPI function read status from to device. Clear 0 by operation finish.   |
| 4   | WRSR         | R/W | 0       | This bit control SPI function write status to device. Clear 0 by operation finish.   |
| 3   | SECTOR_ERASE | R/W | 0       | This bit control SPI function sector erase device. Clear 0 by operation finish.  |
| 2   | READ_ID      | R/W | 0       | This bit control SPI function read id from device. Clear 0 by operation finish.  |

|   |      |     |   |  |
|---|------|-----|---|--|
| 1 | PROG | R/W | 0 | This bit control SPI function program data to device or set to 1 when memory cycle for LPC interface program flash. Clear 0 by operation finish. |
| 0 | READ | R/W | 0 | This bit control SPI function read data from device or set to 1 when memory cycle for LPC interface read flash. Clear 0 by operation finish.     |

**SPI Low Byte Data Register — Index FAh**

| Bit | Name   | R/W | Default | Description   |
|-----|--------|-----|---------|---|
| 7-0 | L_DATA | R   | 0       | When SPI is received 16 bits or 8 bits data from device. This register saves low byte data. |

**SPI address high byte Register — Index FBh**

| Bit | Name        | R/W | Default | Description   |
|-----|-------------|-----|---------|---|
| 7-0 | Addr_H_byte | R/W | 0       | This register provides high byte address for sector erase, program, read operation. |

**SPI address medium byte Register — Index FCh**

| Bit | Name        | R/W | Default | Description   |
|-----|-------------|-----|---------|---|
| 7-0 | Addr_M_byte | R/W | 0       | This register provides medium byte address for sector erase, program, read operation. |

**SPI address low byte Register — Index FDh**

| Bit | Name        | R/W | Default | Description  |
|-----|-------------|-----|---------|--|
| 7-0 | Addr_L_byte | R/W | 0       | This register provides low byte address for sector erase, program, read operation. |

**SPI program byte Register — Index FEh**

| Bit | Name      | R/W | Default | Description   |
|-----|-----------|-----|---------|---|
| 7-0 | PORG_BYTE | R/W | 0       | This register provides number to program flash for continuous mode. |

**SPI write data Register — Index FFh**

| Bit | Name   | R/W | Default | Description  |
|-----|--------|-----|---------|--|
| 7-0 | WR_dat | R/W | 0       | This register provides data to write flash for program, write status function. |

## 8.11 PME and ACPI Registers (CR0A)

### 8.11.1 Configuration Register

#### Device Enable Register — Index 30h

| Bit | Name     | R/W | Default | Description                       |
|-----|----------|-----|---------|-----------------------------------|
| 7-1 | Reserved | -   | -       | Reserved                          |
| 0   | PME_EN   | R/W | 0       | 0: disable PME.<br>1: enable PME. |

#### PME Event Enable Register — Index F0h

| Bit | Name       | R/W | Default | Description   |
|-----|------------|-----|---------|---|
| 7   | Reserved   | -   | -       | Reserved  |
| 6   | MO_PME_EN  | R/W | 0       | Mouse PME event enable.<br>0: disable mouse PME event.<br>1: enable mouse PME event.                                  |
| 5   | KB_PME_EN  | R/W | 0       | Keyboard PME event enable.<br>0: disable keyboard PME event.<br>1: enable keyboard PME event.                         |
| 4   | HM_PME_EN  | R/W | 0       | Hardware monitor PME event enable.<br>0: disable hardware monitor PME event.<br>1: enable hardware monitor PME event. |
| 3   | PRT_PME_EN | R/W | 0       | Parallel port PME event enable.<br>0: disable parallel port PME event.<br>1: enable parallel port PME event.          |
| 2   | UR2_PME_EN | R/W | 0       | UART 2 PME event enable.<br>0: disable UART 2 PME event.<br>1: enable UART 2 PME event.                               |
| 1   | UR1_PME_EN | R/W | 0       | UART 1 PME event enable.<br>0: disable UART 1 PME event.<br>1: enable UART 1 PME event.                               |
| 0   | FDC_PME_EN | R/W | 0       | FDC PME event enable.<br>0: disable FDC PME event.<br>1: enable FDC PME event.  |

#### PME Event Status Register — Index F1h

| Bit | Name      | R/W | Default | Description  |
|-----|-----------|-----|---------|--|
| 7   | Reserved  | -   | -       | Reserved   |
| 6   | MO_PME_ST | R/W | -       | Mouse PME event status.<br>0: Mouse has no PME event.<br>1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.          |
| 5   | KB_PME_ST | R/W | -       | Keyboard PME event status.<br>0: Keyboard has no PME event.<br>1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event. |

|   |            |     |   |  |
|---|------------|-----|---|--|
| 4 | HM_PME_ST  | R/W | - | Hardware monitor PME event status.<br>0: Hardware monitor has no PME event.<br>1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event. |
| 3 | PRT_PME_ST | R/W | - | Parallel port PME event status.<br>0: Parallel port has no PME event.<br>1: Parallel port has a PME event to assert. Write 1 to clear to be ready for next PME event.          |
| 2 | UR2_PME_ST | R/W | - | UART 2 PME event status.<br>0: UART 2 has no PME event.<br>1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.                               |
| 1 | UR1_PME_ST | R/W | - | UART 1 PME event status.<br>0: UART 1 has no PME event.<br>1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.                               |
| 0 | FDC_PME_ST | R/W | - | FDC PME event status.<br>0: FDC has no PME event.<br>1: FDC has a PME event to assert. Write 1 to clear to be ready for next PME event.  |

**ACPI Control Register — Index F4h**

| Bit | Name         | R/W | Default | Description  |
|-----|--------------|-----|---------|--|
| 7   | TS3          | R/W | 0       | Set to 1 into S1 state.<br>Two wake up methods:<br>1. PME wake up event ( Must write this bit to 0.<br>2. PS_OUT# wake up event ( Auto clear this bit.             |
| 6   | SPI_RST_EN   | R/W | 0       | Set one to enable the reset signal from SPI via the PWROK or PCIRST#. (SPI as backup BIOS will assert a reset signal when FWH doesn't response in 4 seconds)       |
| 5   | KEY_SEL_ADD  | R/W | 0       | Set this bit one and KEY_SEL (CR2D[2:1]) 2'b00 will select windows 98 wakeup key as keyboard wakeup key.   |
| 4   | EN_KBWAKEUP  | R/W | 0       | Set one to enable keyboard wakeup event asserted via PWSOUT#.  |
| 3   | EN_MOWAKEUP  | R/W | 0       | Set one to enable mouse wakeup event asserted via PWSOUT#.   |
| 2-1 | PWRCTRL      | R/W | 11      | The ACPI Control the PSON_N to always on or always off or keep last state<br>00 : keep last state<br>10 : Always on<br>01 : Reserved (always on)<br>11: Always off |
| 0   | VSB_PWR_LOSS | R/W | 0       | When VSB 3V comes, it will set to 1, and write 1 to clear it   |

**ACPI Control Register — Index F5h**

| Bit | Name | R/W | Default | Description |
|-----|------|-----|---------|-------------|
|-----|------|-----|---------|-------------|

|     |              |     |    |  |
|-----|--------------|-----|----|--|
| 7   | SEL_S3       | R/W | 0  | 1: selected by TS3<br>TS3<br>0: chip decided into S3 state from S3 pin<br>1 : chip direct into S3 state<br>0: chip decided into S3 state from VDD (VCC) power detect ok., which chip detects voltage circuit |
| 6   | Reserved     | R/W | 0  | Dummy register   |
| 5   | RSTCON_EN    | R/W | 0  | 0: Enable RSTCON# output via PWROK.<br>1: Enable RSTCON# output via PCIRST#.   |
| 4-3 | DELAY        | R/W | 11 | The PWROK delay timing from VDD3VOK by followed setting<br>00 : 100ms<br>01 : 200ms<br>10 : 300ms<br>11 : 400ms  |
| 2   | VINDB_EN     | R/W | 1  | Enable the PCIRSTIN_N and ATXPWGD de-bounce.   |
| 1   | PCIRST_DB_EN | R/W | 0  | Enable the LRESET_N de-bounce.   |
| 0   | Reserved     | R/W | 0  | Dummy register.  |

**ACPI Control Register — Index F7h**

| Bit | Name         | R/W | Default | Description   |
|-----|--------------|-----|---------|---|
| 7-4 | Reserved     | R/W | 0       | Reserved.   |
| 3-2 | Reserved     | R/W | 0       | Dummy registers.  |
| 1   | PWR_STS2_TRI | R/W | 0       | Set this bit to one will cause Pin55 be tri-state Status in S5 state.                                     |
| 0   | PWR_STS_EN   | R/W | 1       | Enable power status pins. Pin77 will be S5# function. P56 will be ST1 function. P55 will be ST2 function. |

## 9. Electron Characteristic

### 9.1 Absolute Maximum Ratings

| PARAMETER             | RATING          | UNIT |
|-----------------------|-----------------|------|
| Power Supply Voltage  | -0.5 to 5.5     | V    |
| Input Voltage         | -0.5 to VDD+0.5 | V    |
| Operating Temperature | 0 to 70         | °C   |
| Storage Temperature   | -55 to 150      | °C   |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

### 9.2 DC Characteristics

( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ )

| Parameter                        | Conditions   | MIN | TYP                | MAX                | Unit |
|----------------------------------|--|-----|--------------------|--------------------|------|
| Temperature Error, Remote Diode  | $60^\circ\text{C} < T_D < 145^\circ\text{C}$ , $V_{CC} = 3.0\text{V}$ to $3.6\text{V}$<br>$0^\circ\text{C} < T_D < 60^\circ\text{C}$ $100^\circ\text{C} < T_D < 145^\circ\text{C}$ |     | $\pm 1$<br>$\pm 1$ | $\pm 3$<br>$\pm 3$ | °C   |
| Supply Voltage range             |  | 3.0 | 3.3                | 3.6                | V    |
| Average operating supply current |  |     | 10                 |                    | mA   |
| Standby supply current           |  |     | 5                  |                    | uA   |
| Resolution                       |  |     | 1                  |                    | °C   |
| Power on reset threshold         |  |     | 2.2                | 2.4                | V    |
| Diode source current             | High Level   |     | 95                 |                    | uA   |
|                                  | Low Level  |     | 10                 |                    | uA   |

### 9.3 DC Characteristics Continued

( $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ )

| PARAMETER  | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|--|------|------|------|------|------|------------|
| <b>I/OD<sub>12t5v</sub>-TTL level bi-directional pin with schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.</b> |      |      |      |      |      |            |
| Input Low Voltage  | VIL  |      |      | 0.8  | V    |            |
| Input High Voltage   | VIH  | 2.0  |      |      | V    |            |
| Output Low Current   | IOL  |      | +12  |      | mA   | VOL = 0.4V |
| Input High Leakage   | ILIH |      |      | +1   | μA   | VIN = VDD  |
| Input Low Leakage  | ILIL | -1   |      |      | μA   | VIN = 0V   |
| <b>I/OD<sub>16t5v</sub>-TTL level bi-directional pin, Open-drain output with 16 mA sink capability, 5V tolerance.</b>                      |      |      |      |      |      |            |
| Input Low Voltage  | VIL  |      |      | 0.8  | V    |            |
| Input High Voltage   | VIH  | 2.0  |      |      | V    |            |
| Output Low Current   | IOL  |      | +16  |      | mA   | VOL = 0.4V |

|   |      |     |     |     |    |             |
|---|------|-----|-----|-----|----|-------------|
| Input High Leakage  | ILIH |     |     | +1  | μA | VIN = VDD   |
| Input Low Leakage   | ILIL | -1  |     |     | μA | VIN = 0V    |
| <b>I/OOD<sub>12t</sub>-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function.</b> |      |     |     |     |    |             |
| Input Low Threshold Voltage   | Vt-  |     |     | 0.8 | V  | VDD = 3.3 V |
| Input High Threshold Voltage  | Vt+  | 2.0 |     |     | V  | VDD = 3.3 V |
| Output Low Current  | IOL  |     | -12 | -9  | mA | VOL = 0.4 V |
| Output High Current   | IOH  | +9  | +12 |     | mA | VOH = 2.4V  |
| Input High Leakage  | ILIH |     |     | +1  | μA | VIN = VDD   |
| Input Low Leakage   | ILIL | -1  |     |     | μA | VIN = 0V    |
| <b>I/O<sub>12t</sub>- TTL level bi-directional pin, Output pin with 12mA source-sink capability.</b>  |      |     |     |     |    |             |
| Input Low Threshold Voltage   | Vt-  |     |     | 0.6 | V  | VDD = 3.3 V |
| Input High Threshold Voltage  | Vt+  | 0.9 |     |     | V  | VDD = 3.3 V |
| Output High Current   | IOH  | +9  | +12 |     | mA | VOH = 2.4V  |
| Input High Leakage  | ILIH |     |     | +1  | μA | VIN = 1.2V  |
| Input Low Leakage   | ILIL | -1  |     |     | μA | VIN = 0V    |
| <b>IN<sub>ts</sub> - TTL level input pin with schmitt trigger</b>   |      |     |     |     |    |             |
| Input Low Voltage   | VIL  |     |     | 0.8 | V  |             |
| Input High Voltage  | VIH  | 2.0 |     |     | V  |             |
| Input High Leakage  | ILIH |     |     | +1  | μA | VIN = VDD   |
| Input Low Leakage   | ILIL | -1  |     |     | μA | VIN = 0 V   |
| <b>IN<sub>tsv</sub> - TTL level input pin with 5V tolerance.</b>  |      |     |     |     |    |             |
| Input Low Voltage   | VIL  |     |     | 0.8 | V  |             |
| Input High Voltage  | VIH  | 2.0 |     |     | V  |             |
| Input High Leakage  | ILIH |     |     | +1  | μA | VIN = VDD   |
| Input Low Leakage   | ILIL | -1  |     |     | μA | VIN = 0 V   |
| <b>IN<sub>tsv</sub> - TTL level input pin with schmitt trigger, 5V tolerance.</b>   |      |     |     |     |    |             |
| Input Low Voltage   | VIL  |     |     | 0.8 | V  |             |
| Input High Voltage  | VIH  | 2.0 |     |     | V  |             |
| Input High Leakage  | ILIH |     |     | +1  | μA | VIN = VDD   |
| Input Low Leakage   | ILIL | -1  |     |     | μA | VIN = 0 V   |
| <b>OD<sub>12</sub>-Open-drain output with 12 mA sink capability.</b>  |      |     |     |     |    |             |
| Output Low Current  | IOL  |     | -12 |     | mA | VOL = 0.4V  |
| <b>OD<sub>12-5v</sub>-Open-drain output with 12 mA sink capability, 5V tolerance.</b>   |      |     |     |     |    |             |
| Output Low Current  | IOL  |     | -12 |     | mA | VOL = 0.4V  |
| <b>OD<sub>24</sub>-Open-drain output with 24 mA sink capability.</b>  |      |     |     |     |    |             |
| Output Low Current  | IOL  |     | -24 |     | mA | VOL = 0.4V  |
| <b>OD<sub>16-u10-5v</sub>-Open-drain output with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.</b>                                       |      |     |     |     |    |             |
| Output Low Current  | IOL  |     | -16 |     | mA | VOL = 0.4V  |
| <b>O<sub>8</sub>- Output pin with 8 mA source-sink capability.</b>  |      |     |     |     |    |             |
| Output High Current   | IOH  | +6  | +8  |     | mA | VOH = 2.4V  |
| <b>O<sub>8-u47-5v</sub>- Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.</b>   |      |     |     |     |    |             |
| Output High Current   | IOH  | +6  | +8  |     | mA | VOH = 2.4V  |
| <b>O<sub>12</sub>- Output pin with 12 mA source-sink capability.</b>  |      |     |     |     |    |             |
| Output High Current   | IOH  | +9  | +12 |     | mA | VOH = 2.4V  |
| <b>O<sub>30</sub>- Output pin with 30 mA source-sink capability.</b>  |      |     |     |     |    |             |
| Output High Current   | IOH  | +26 | +30 |     | mA | VOH = 2.4V  |

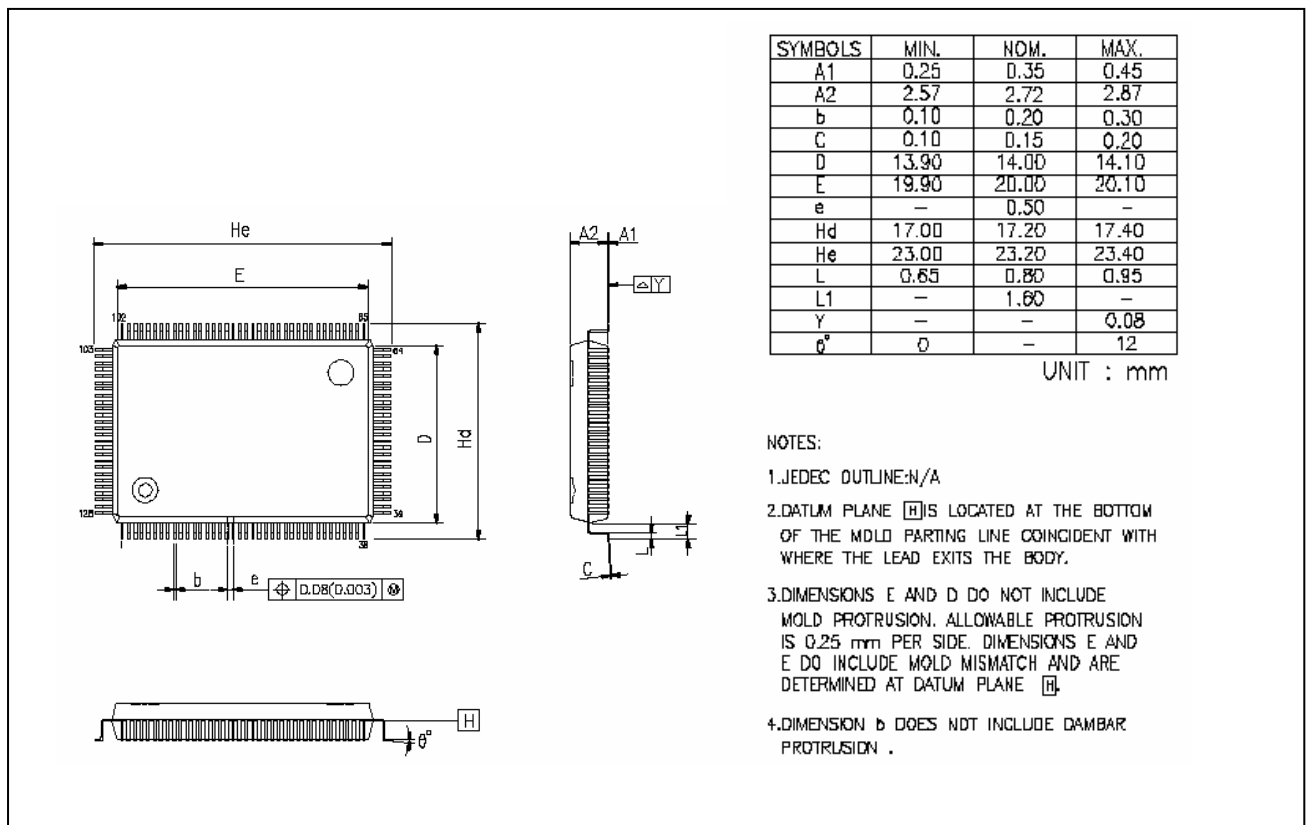


## 10. Ordering Information

| Part Number | Package Type           | Production Flow          |
|-------------|------------------------|--------------------------|
| F71863FG    | 128-PQFP Green Package | Commercial, 0°C to +70°C |

## 11. Package Dimensions

### 128 PQFP



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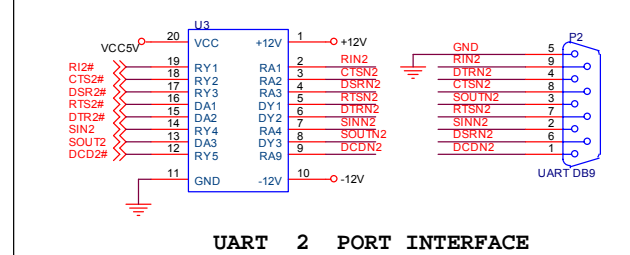
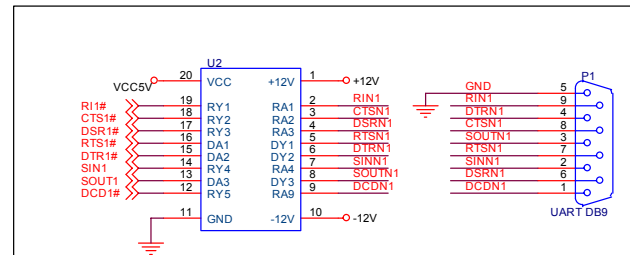
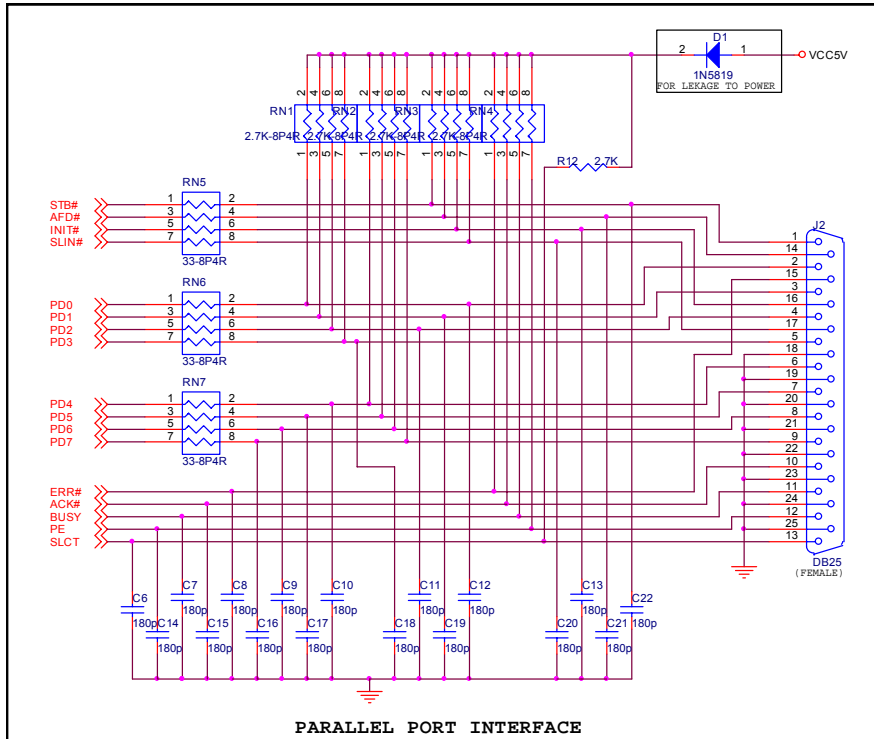
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FAX : 866-2-8227-8037

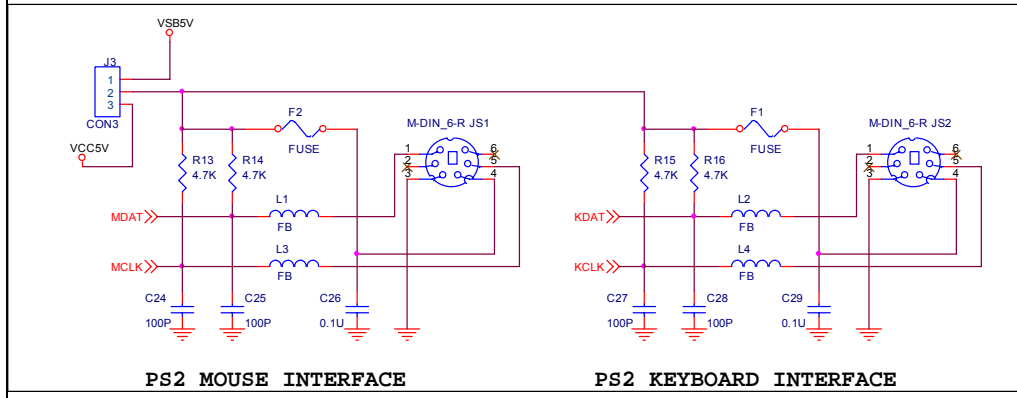
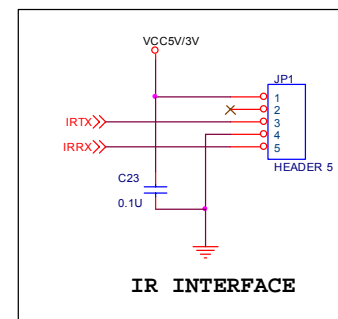
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# F71863



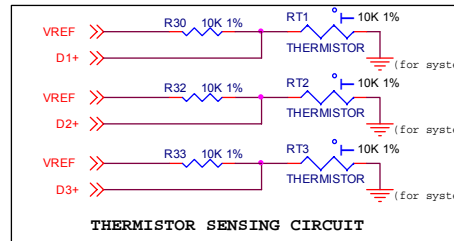
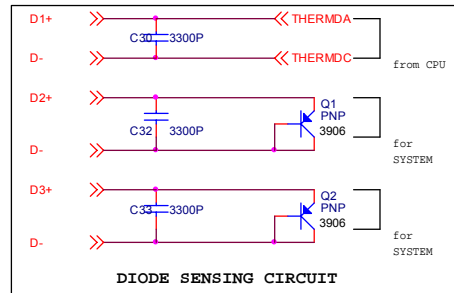
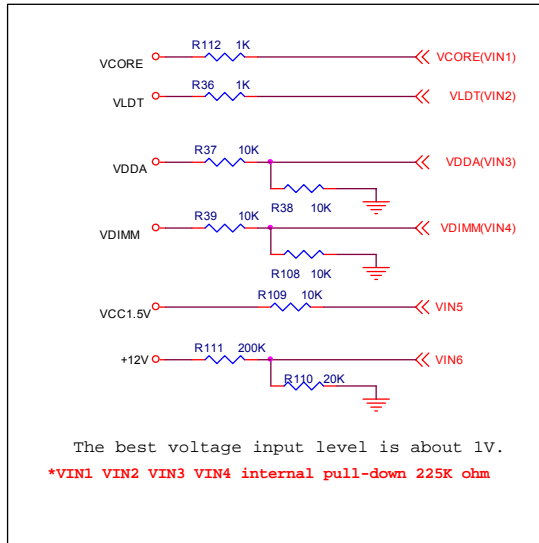
RING-IN Wake-up not supported by F71863.  
Please use chipset RING-IN for wake-up function



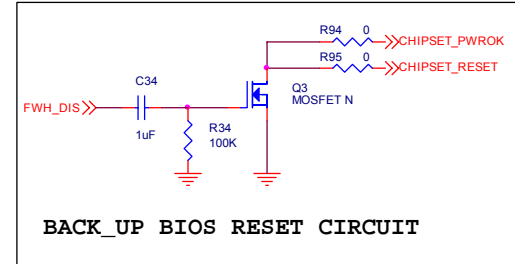
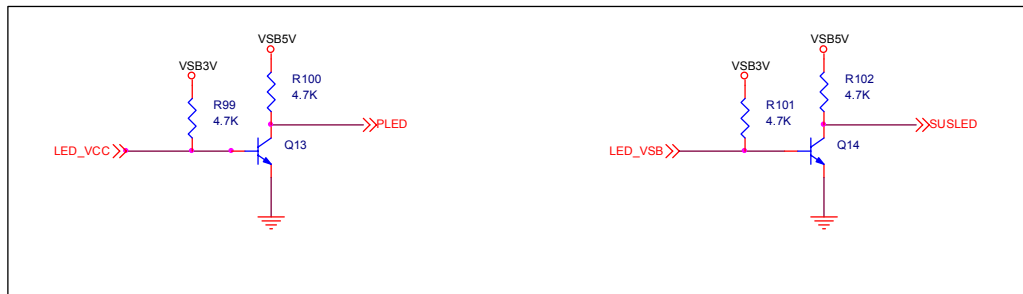
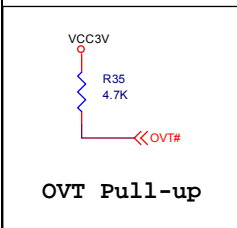
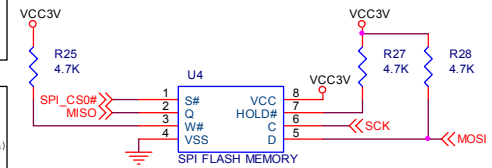
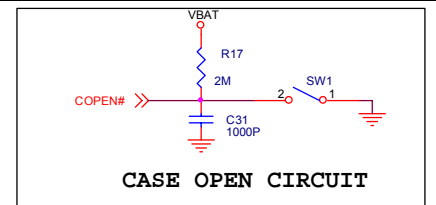
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|-------------------------------------|----------------------|--------------|
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| Feature Integration Technology Inc. |                      |              |
| Size                                | Document Number      | Rev          |
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| Date:                               | Friday, May 02, 2008 | Sheet 2 of 7 |

# F71863

## VOLTAGE SENSING.

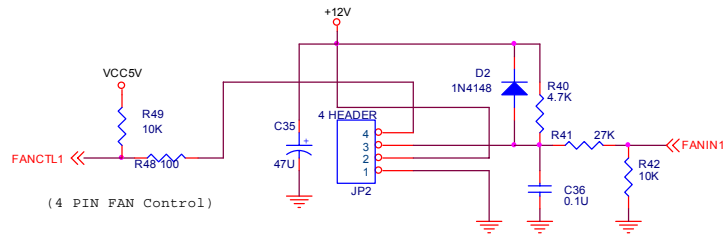


## Temperature Sensing



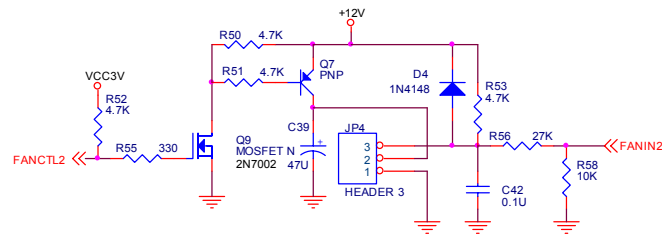
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| Date:                              | Monday, July 21, 2008       | Sheet 3 of 7 |

# F71863

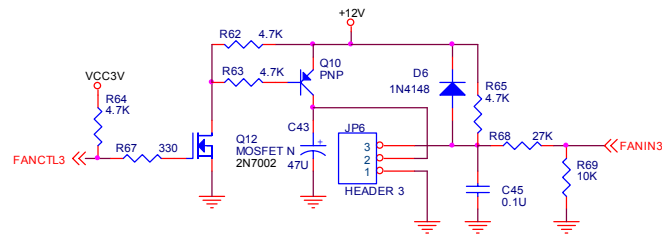


(4 PIN FAN Control)

PWM FAN 1 SPEED CONTROL

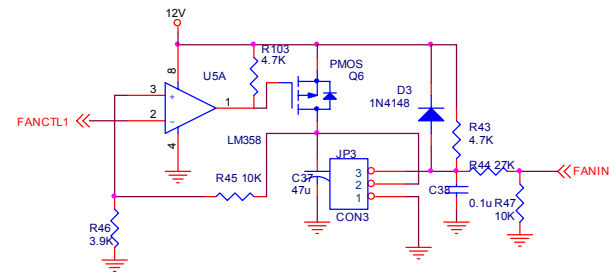


PWM FAN 2 SPEED CONTROL

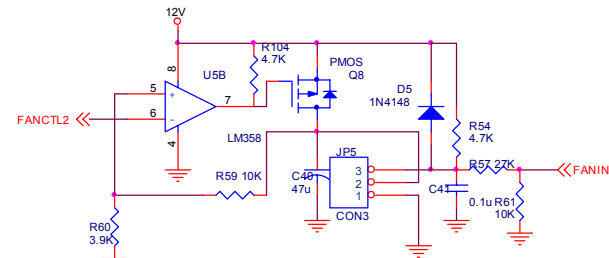


PWM FAN 3 SPEED CONTROL

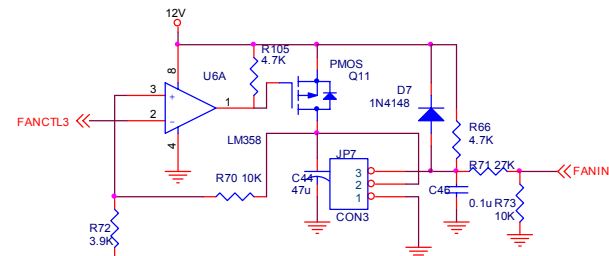
FAN CONTROL FOR PWM OR DC



DC FAN Control with OP 1



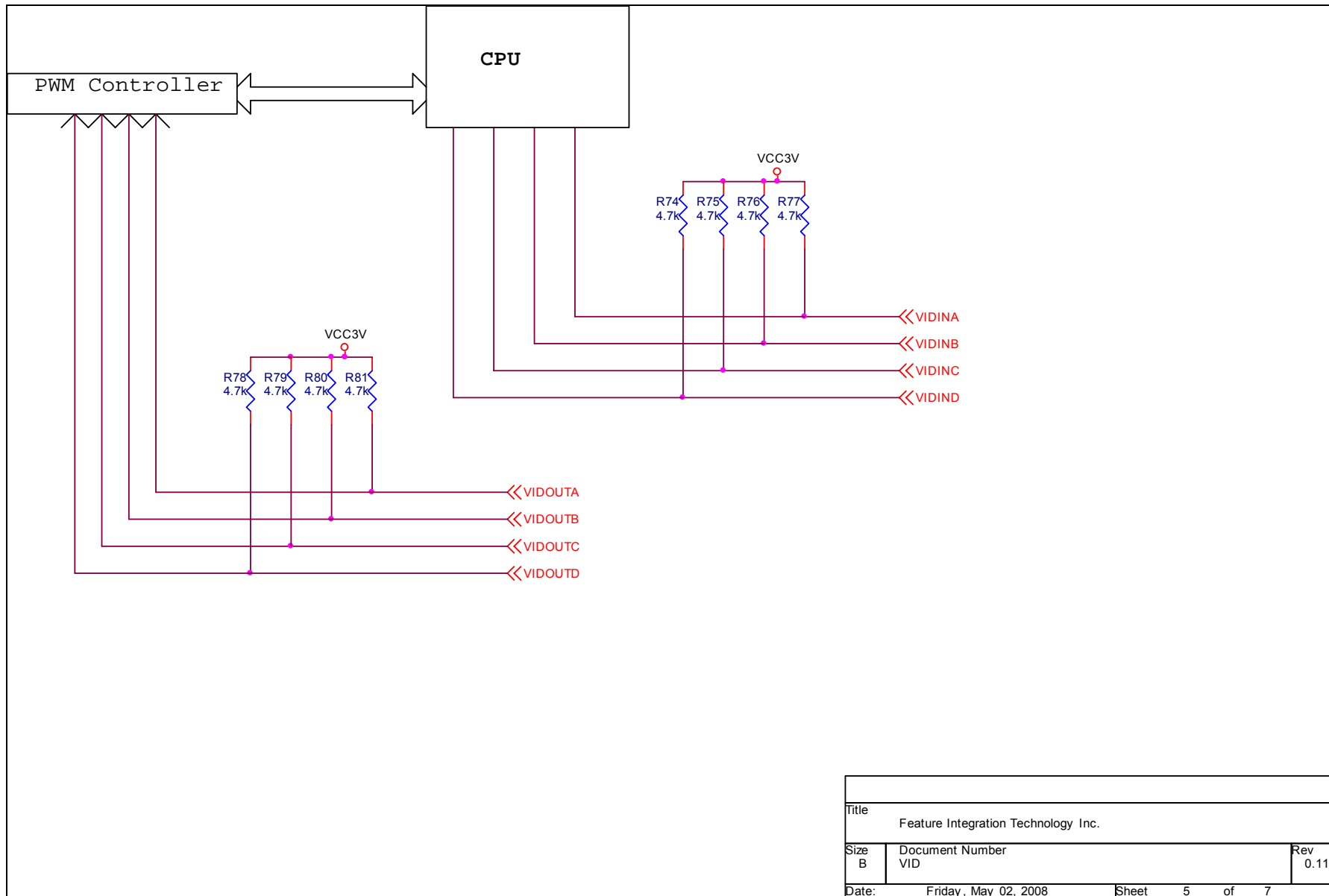
DC FAN Control with OP 2



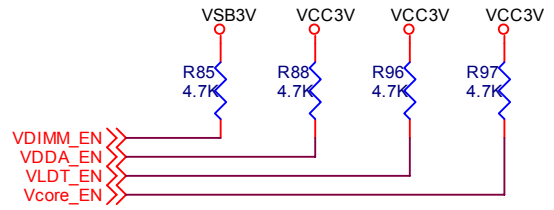
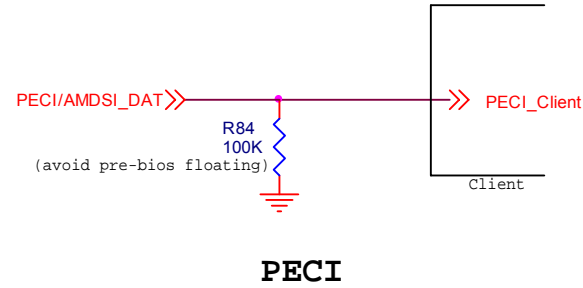
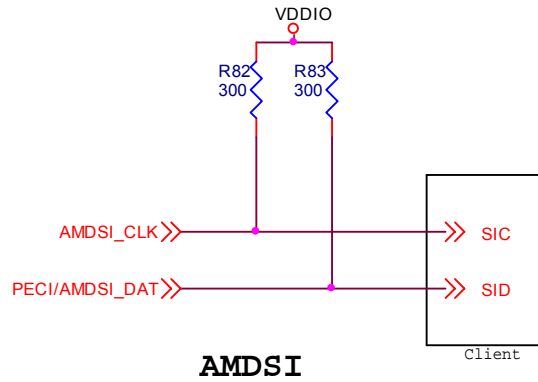
DC FAN Control with OP 3

|                                     |                      |              |
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| B                                   | FAN Control          | 0.11         |
| Date:                               | Friday, May 02, 2008 | Sheet 4 of 7 |

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**Power Sequence Pull-up R**



**CPU\_PWRGD Pull-Up**

|                                     |                      |              |
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| Size                                | Document Number      | Rev          |
| A                                   | AMDSI/PECCI          | 0.11         |
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