AViA-9600™ Family

Single-Chip Digital Set-Top Box Solution

1 Introduction

The AViA-9600 family of processors is an advanced solution for digital set-top box (STB) applications including hard disk drive (HDD) time-shifting and web access. This highly integrated silicon provides a wide array of features and interfaces, including:

- MPEG-2 transport demultiplexer
- DVB and DES descramblers
- MPEG-2 video and audio decoders
- Dolby Digital AC-3 audio decoder
- Advanced graphics display list processor
- 150 MHz SPARC CPU with 32KB cache
- Unified Memory Architecture
- Multiple host interface modes:
  - *PCI synchronous (master, slave)*
  - *68K-style asynchronous (master, slave)*
  - *Coldfire/PowerPC synchronous (slave)*
  - *Hitachi SH4 synchronous (slave)*
- Synchronous/asynchronous Flash support
- IDE/ATAPI disk drive interface (master)
- OpenCable POD, DVB-CI, or NRSS-B card interface (master)
- Interface for two SmartCards
- IEEE 1394, USB Host, IDC, IEEE 1284 Peripheral, Modem DAA, UART, Infrared, SPI, and GPIO interfaces
- Digital video encoder (DENC)
- Digital video capture and output

1.1 Product Benefits

The AViA-9600 is a fourth generation design with a powerful SPARC processor (along with four other embedded RISC processors or DSPs), advanced graphics engine, extensive audio feature set, and a comprehensive set of I/O peripherals.

Key benefits:

- Platform for digital time-shifting – hard disk (IDE) interface, copy protection, and trick play modes
- Support for sophisticated user interface – advanced graphics display list processor, copy engine, color expander, and enhanced text display
- Home peripherals connectivity via USB, IEEE 1394 and 1284
- BOM cost reduction – unified memory, integrated peripherals, and soft modem
- Flexible solution – architecture that allows customized and software-configurable transport demuxing and A/V decoding, as well as a choice of external CPUs (plus the internal host)
- Support for bandwidth-demanding applications – high performance CPU, DDR SDRAM, dedicated graphics accelerators, as well as multiple DMA channels
- Worldwide deployment support – multiple CAS, descrambling algorithms, and transport formats
- Superior display quality – crisp slow motion with progressive scan output, flicker filter
- Home theater experience – versatile audio support with MP3, MPEG-2 5.1, AC3 and DTS support

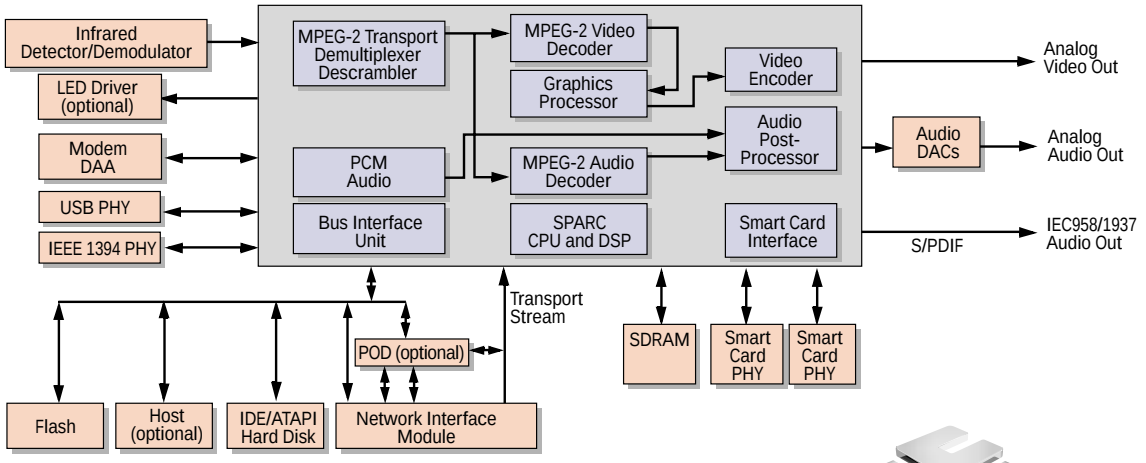

Figure 1. Fully Configured Set-Top Box Design Using the AViA-9600

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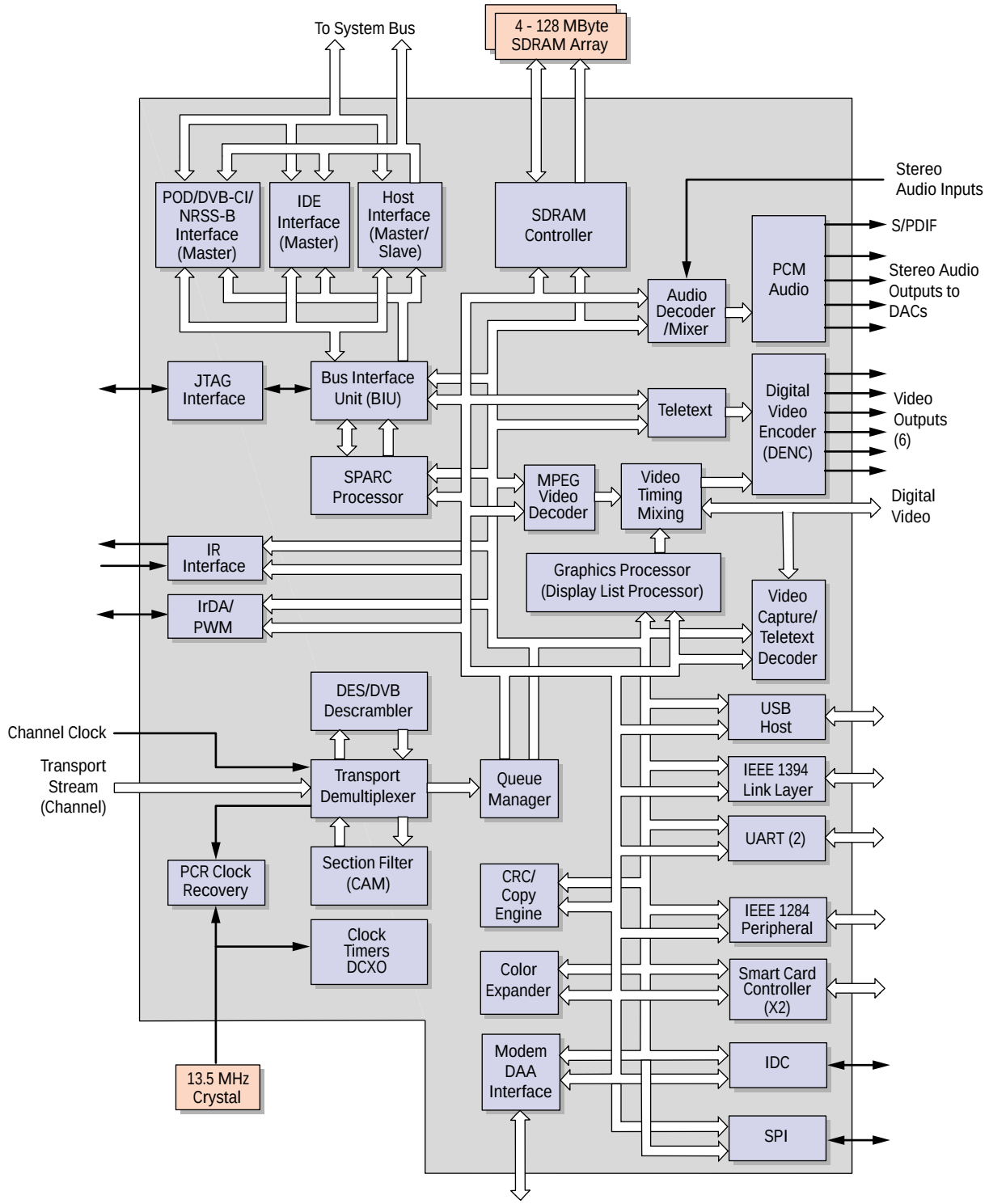

Figure 2. AViA-9600 Internal Architecture Diagram

1.2 Typical Applications

The versatility and high level of integration of the AViA-9600 make it an ideal set-top box solution (see Figure 1). The complex logic needed to decode and display the MPEG-2 video and audio from the network or a hard disk drive is contained in a single device. The AViA-9600 integrates a powerful CPU, thus enabling "hostless" applications.

The remaining devices that can be added to complete a fully configured set-top box design include:

- Network interface module (NIM)
- IR detector/demodulator, LED driver (IR blaster)
- Audio DACs
- 4 to 128 MBytes of SDRAM
- Flash memory
- Two SmartCard PHY
- POD, NRSS-B/DVB-CI interface socket
- Modem DAA (if NIM is one-way only)
- USB PHY
- IEEE 1394 PHY
- IDE hard disk drive

The integrated IDE/ATAPI interface is included to allow a hard disk drive to be added into the set-top box for time-shift DVR (digital video recorder) or data broadcasting applications. The interface can also support a DVD-ROM drive, enabling a combination DVD player/set-top box design.

2 AViA-9600 Internal Architecture

Figure 2 shows the internal architecture of the AViA-9600 family. Each of the key functional blocks are discussed in the following sections.

2.1 Embedded CPU

An embedded microSPARC V8 CPU is integrated into the AViA-9600. In low-cost systems this CPU can be used as the system host. In high-end systems, this CPU can serve as a coprocessor for a variety of tasks such as peripheral management, graphics accelerator, or section builder.

Key features:

- Supports clock speeds up to 150 MHz
- 5-stage 32-bit integer pipeline (nearly 1 instruction per clock in real systems)
- 16K instruction cache (4-way set-associative)
- 16K data cache (4-way set-associative with write-back), partitionable into cache and data memory areas
- Supervisor/user modes and read/write restriction modes for system reliability
- Two timers
- Interrupt controller to route each peripheral IRQ to any of the 16 IRQ levels
- Integrated 32-bit DSP unit that executes in parallel with the main SPARC engine to support certain audio processing and soft-modem

2.2 Graphics Subsystem

The AViA-9600 graphics subsystem includes the Graphics Processor (Display List Processor), the Copy/CRC Engines and Color Expander. The Graphics Processor executes a "display list" in the SDRAM; this is a special program that contains a sequence of instructions for drawing the display. The graphics subsystem also provides two dynamically reloadable color look-up tables (CLUTs). These, together with the display list architecture, provide the flexibility to support an arbitrary number of overlapping regions and planes, subject only to SDRAM bandwidth and clock speed constraints.

Key features:

- Multiple overlapping regions with independent resolution, pixel coding method, and CLUT
- Two 256x32 dynamically reloadable CLUTs (for fast switching between adjacent regions with different CLUTs)
- Anti-flicker filter, selectable on a per-region basis
- Square pixel support
- Overlay and continuous scaling of both analog and digital video channels
- Multiple color modes include:
  - *4-bit per pixel (bpp) and 8 bpp CLUT modes*
  - *16-bit direct RGBA mode (5,5,5,1 or 4,4,4,4 or 5,6,5)*
  - *32-bit direct RGBA mode (8,8,8,8)*
  - *256 levels of alpha blending with 24 bits of color*
  - *8 bpp squashed YUV mode*
  - *16 bpp direct YUV mode*
- Color Expansion Accelerator for fast font rendering and region fills
  - *Shifting for word alignment and kerning support for font display*
  - *Expansion of one or two-bit fonts to color display mode (8 or 16-bit pixels)*
- Copy Engine for fast rendering of rectangles and bitmaps, memory-to-memory copy (blitting), compositing and scrolling
  - *Region-based operations*
  - *Chroma-key copy operations*
  - *Alpha blending of two objects or solid color*
  - *Full 16 logical raster-operators with plane mask*
  - *Clip mask*
- Overlay of high resolution, multi-color hardware cursor (implemented as a region)
- Video and graphics mixing with alpha blending; for example:
  - *Picture in Graphics (PIG); i.e., real-time video overlaid on graphics*
  - *Enhanced EPG display and web browsing*
- CCIR-656 video in/out port for direct video input (progressive/interlaced) or DENC bypass; the input port also allows the graphics subsystem to lock to the timing of an external video source
- Real-time decimation for video capture
- Closed caption and teletext pass-through

2.3 Host Bus Interface

The AViA-9600 has a highly flexible external bus interface that supports a wide range of system configurations. The AViA-9600 bus interface can be configured for both master and slave modes. In master mode, the internal SPARC acts as the set-top box host. When an external host is used, the AViA-9600 operates in slave mode.

- Slave modes:
  - *68000*
  - *PowerPC 823, 823E*
  - *Coldfire 5206, 5307, 5407*
  - *SH4*
  - *PCI 2.1*
- Master modes:
  - *Host interface to external peripherals with 68000-style asynchronous transfer or transfers with SRAM/Flash/ROM timing (similar to Intel-style transfers, and therefore also supports certain Intel or ISA-bus peripherals)*
  - *Host interface to external peripherals with Coldfire-style synchronous mode*
  - *PCI 2.1 (when the AViA-9600 runs as a PCI device)*
  - *Synchronous and asynchronous Flash support*
  - *IDE/ATAPI controller (for disk drives and DVD drives)*
  - *POD/DVB-CI/NRSS-B host interface controller (PCMCIA)*
  - *DMA controller*
  - *Eight Chip Selects for external ROM, Flash ROM, etc.*
  - *IRQ input (to embedded SPARC)*

2.4 Transport Demux

The AViA-9600 includes a powerful dedicated RISC CPU for flexible processing of transport streams*. The transport demux also includes a Content Addressable Memory (CAM) that facilitates fast searches required in section header filtering.

The Transport Demux block supports transport streams in DVB (MPEG-2), DSS/DirecTV and DVD (PES) formats. The descrambler supports a wide range of conditional access and copy protection schemes applied to transport streams, including DVB common mode and DES descrambling. Other hardware support includes DVB Teletext, channel buffering with DRAM, and CRC checking.

The Transport Demux supports 32 filters, with 8 bytes of filter condition and mask per filter, multiple sections per transport packet, and input bit rates up to 80 Mbps (actual performance depends on the aggregate feature set of the microcode).

The microprogrammable Transport Demux architecture provides the flexibility for implementing custom transport stream filtering and error resilience schemes, including lost packet detection and handling. It also facilitates the support of system requirements such as seamless splicing. In addition, there is a Program Clock Reference (PCR) recovery facility and DCXO control system.

* This CPU is in addition to the embedded SPARC processor.

2.5 MPEG Video Decode

The AViA-9600 uses a proven, microcode-driven MPEG decoder core based on the C-Cube AViA-60x™ product. The decoder is implemented using a dedicated CPU core with hardware-assist for specialized operations. For example, operations such as "decode with A/V sync" require virtually no host CPU overhead. The audio/video decoder supports the MPEG-2 MP@ML standard.

The MPEG decoder operation is controlled by microcode which is downloaded to the AViA-9600 by the host CPU. This design allows easy upgrade of decoder features simply by changing the microcode. The host software controls the decoder through a high-level API. In addition, frame and error interrupts are also available as options. This model allows implementations to be up and running very quickly with minimal software driver development.

The microcode API for the AViA-9600 is compatible with that of the AViA-60x decoders. This allows an easy transition between C-Cube chips. C-Cube also offers sample software drivers that are architected to facilitate support of different middleware or operating systems.

The microcode offers a number of extended features used in STB applications, including:

- VBI (such as Closed Caption and EDS) data extraction from the MPEG video elementary stream layer
- Clip mode decode
- Independent audio and video decode
- Bit error masking and recovery
- Still picture decode and manipulation
- Pan-and-scan display
- Letterbox (4:3, 16:9, 20:9)
- Video scaling

The AViA-9600 decoder is fully compliant with the European Digital Video Broadcast (DVB) standard, specified in the DVB Implementation Guidelines (TM 1214, Rev. 9).

The video decoder can decode a video stream from one of the following sources:

- Transport Demux
- IDE/ATAPI
- IEEE 1394
- DRAM

The AViA-9600 can master video timing when decoding MPEG video. Decoded video can be sent to the CCIR-656 output port and to the internal DENC. If an external DENC is used, the internal AViA-9600 DENC can be used for a graphics-free program output (e.g., for output to a VCR).

The video decoder supports all resolutions specified in MPEG-2 MP@ML. MPEG-1 bitstreams can also be decoded per MP@ML specifications. Several aspect ratios are supported through pan-and-scan or letterbox modes.

The video decoder core used by the AViA-9600 is also implemented in C-Cube DVD products. DVD-STB combination applications can be supported by the AViA-9600 with alternate microcode.

2.6 Audio Decode

The AViA-9600 audio decoder is capable of decoding MPEG-1 Layer II (Musicam), MPEG-1 Layer III (MP3), MPEG-2 5.1, Dolby AC-3 and DTS.

After decoding Dolby AC-3, the AViA-9600 outputs the six channels to three of the I^2S-compatible digital audio outputs, and downmixed Dolby Prologic audio to the fourth output. The audio stream can also be simultaneously sent to the S/PDIF interface in IEC-1937 (compressed) or IEC-958 (uncompressed) format.

The audio decoder can decode an audio stream from the same sources as the video decoder (see above). Locally sourced PCM audio clips can be played and mixed with decoded MPEG or AC-3 Streams. Independent volume control is available.

2.7 Memory Control

The AViA-9600 uses an unified DRAM memory system that is designed to support a number of configurations of SDRAM (Single Data Rate or Double Data Rate) or SGRAM. The 32-bit wide data bus is clocked at up to 150 MHz, providing a maximum throughput of 1.2 GB/s. Configurations from 4 MB (with two 1MB x 16 parts) to 128 MB are supported. Alternatively, a 16-bit interface can be configured when DDR SDRAM is used. The number of peripherals, as well as usage of graphics in the design, affect the DRAM bandwidth requirements. Some configurations may require 32-bit DDR SDRAM.

2.8 IEEE 1394

The IEEE 1394 Link Layer Interface of the AViA-9600 supports any PHY layer chip compliant to Annex J of the IEEE 1394 standard. The interface can operate at both 100 and 200 Mbps.

All basic IEEE 1394 transfer types are supported:

- Asynchronous
- Isochronous
- Cycle Master

The isochronous capability supports simultaneous transmit and receive channels. Isochronous transport stream inputs can be routed to either DRAM or the video decoder. Isochronous transport stream outputs can be sourced from DRAM or the Transport Demux. The Transport Demux can remap the audio and video PID values. It also time-stamps the packets according to the 1394 clock reference.

The AViA-9600 IEEE 1394 implementation includes the 5C copy protection.

2.9 Universal Serial Bus (USB)

The AViA-9600 includes a USB 1.1-compliant host controller. This controller implements the host side of the USB protocol, supporting peripherals such as keyboards and printers. Control, Bulk, Interrupt, and Isochronous transfer types are supported at 3 Mbps and 12 Mbps. Data transfers are handled by hardware DMA to DRAM. Interrupts are available for a wide range of USB events.

2.10 NABTS Teletext Decode

The AViA-9600 includes a port that accepts parallel CCIR-656 input. This video path feeds a number of devices including a NABTS Teletext Decoder, the Video Capture system, and the Graphics mixer. The VBI decoder uses the luma samples from the CCIR-656 data stream to decode and extract the NABTS data from a programmable set of lines.

2.11 Other STB Peripherals and Interfaces

A number of other useful peripherals are included in the AViA-9600, including:

- Two ISO 7816-compliant SmartCard controllers (T=0 or T=1)
- IEEE1284 parallel port
- IR transmitter, receiver
- IrDA
- Modem DAA interface
- Pulse width modulator (PWM)
- Serial peripheral interface (SPI)
- Inter-device communication (IDC)
- Two UARTs with hardware flow control
- General-purpose I/O (GPIO)

The SmartCard controller supports DMA transfer between the AViA-9600 DRAM and the SmartCard device. Messages can be sent by DMA to the SmartCard and then the response is sent back by DMA, at which point an IRQ is generated to alert the CPU. The IRQ can be routed to either the AViA-9600 embedded CPU or an external CPU.

The AViA-9600 integrates a multi-function parallel port peripheral interface controller for various applications that require high-speed, bi-directional, parallel communication with a host computer. This 1284 interface supports the Compatible, Reverse Nibble, Reverse Byte, Enhanced Parallel Port (EPP), and Enhanced Capability Port (ECP) modes of the IEEE 1284-1994 Standard Signaling Method for a Bi-Directional Parallel Port Peripheral Interface for Personal Computers. The AViA-9600 implementation does not support the Run Length Encoding (RLE) feature of the ECP protocol.

The IR receiver works in two modes. In the first mode it accepts demodulated pulse sequences from the IR diode receiver (IR detector/demodulator). In the other mode it takes in a modulated digital waveform directly, performs digital filtering, and transfers a list of edge timings via DMA to the

DRAM. This technique allows the AViA-9600 to support all standard remote control protocols and IR codes. The IR transmitter generates modulated carrier pulse sequences similar to those produced by universal remote control units. This design allows the implementation of a "learning remote" without the need for a VCR IR code database.

The IrDA port supports Infrared Device Architecture-compliant devices such as keyboards to communicate with the set-top box.

The pulse-width modulator (PWM) allows the board designer to control a variety of external devices, or to support clock recovery.

The IDC interface supports an I^2C-compatible bus. It allows background communications between the various components in the system. The IDC bus is a simple, two-wire medium for bi-directional, inter-device communications. The two signals, Clock and Data, are common to every device connected to the bus. Each device has a unique address and can act as either a transmitter or a receiver.

The UARTs implement standard bi-directional, full-duplex asynchronous serial communication with external devices at up to 115 Kbps. The UARTs are implemented with hardware handshake (flow control).

The SPI is a 3-wire bi-directional synchronous serial interface. It allows the AViA-9600 to control devices such as NIM, audio DACs and certain front-end loaders for combo DVD/STB designs.

The AViA-9600 also supports a number of programmable GPIO connections for LEDs, buttons, etc.

2.12 DENC

The AViA-9600 includes an internal DENC (Digital Video Encoder) with the following key features:

- Six DACs
  - *One for Composite Video (CVBS)*
  - *Two for S-Video (Y/C)*
  - *Three for RGB or YPrPb*
- NTSC, PAL, and SECAM formats
- Drive double-terminated loads (0 to 1.3 volts into 37.5 ohms)
- Full SCART support
- DVB Teletext (WST), Closed Caption, Extended Data Service (EDS) and V-chip data insertion
- VBI pass-through
- Macrovision copy protection

The DENC uses the same timing as the graphics subsystem. The AViA-9600 can also be used with an external DENC. In such a case, the internal DENC can be used as a VCR video interface that allows users to record programs without graphic overlay.

System	CPU	150 MHz microSPARC V8, 16K+16K cache/SRAM
	Host Interfaces	PCI, 68K, PowerPC, Coldfire, SH4
	Peripheral Interfaces	IEEE 1394 (with 5C copy protection), USB Host, IDC, SPI, IR transmit/receive, IrDA, IEEE 1284 Peripheral, two UARTs, modem DAA
	Card Sockets	Two SmartCard, POD/NRSS-B/DVB-CI
	Disk Drive	IDE/ATAPI
	Memory	4 - 128 Mbytes SDRAM (SDR or DDR) or SGRAM
	JTAG	Boundary Scan and Debug Port
Video	Decoding Standards	MPEG-1, MPEG-2 MP@ML
	Compressed Resolutions	• 720, 704, 640, 544, 528, 480, 352, 320 x 480 and 352 x 240 @30Hz and 24 Hz • 720, 704, 640, 544, 528, 480, 352 x 576 and 352 x 288 @ 25 Hz • 384 x 240 @ 24 Hz
	Aspect Ratios	4:3, 16:9, 20:9, DTG Active Format Descriptor
	Video Encoder	NTSC, PAL, SECAM; 6 DACs
	Graphics Subsystem	• Display List Processor; supports unlimited number of planes and (overlapping) regions, picture-in-graphics (PIG) • Flicker filter, selectable per region • Continuous video scaling • 256 levels of alpha blending • Two 256x32CLUTs supporting fast dynamic reload • Two Copy Engines • Color Expander • NABTS Teletext decode • Digital video input
Audio	Decoding Standards	MPEG-1 Layers II and III (MP3), MPEG-2 5.1, Dolby Digital 5.1 channel, DTS
	Output Channels	• 6-channel PCM and S/PDIF (IEC-1937/IEC-958); • Dolby Digital or MPEG-2 5.1 downmixed to Dolby Prologic or 2-channel PCM
Transport	Stream Parsing	MPEG-2 ISO13818-2, up to 80 Mbps
	PID Filtering	Hardware section filters with CAM, 32 PIDs
	Descrambling	DVB, DES
Physical	Input Voltages	3.3 V – 5% (I/O), 1.8 V – 5% (Core)
	Clock Frequencies	Input = 13.5 or 27MHz, Operating = 150 MHz
	Packaging	308 Ball Grid Array

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