IIT VPIC

MPA Family PCI Inlay & Control Chip

OVERVIEW

The IIT VPIC device connects video capture/display IC's, multimedia subsystems and image compression ICs to the PCI bus. The VPIC provides a glueless interface to the IIT MPA family of chips enabling MPEG and H.320 (video conferencing) applications.

The VPIC has 4 DMA channels, three output and one input. Two of the output channels are dedicated to motion video and are used to transfer captured or decoded video to the PCI graphics card from the VPIC chip or from any other image capture device. The additional input and output channels are used for host communication such as program overlay download. Motion video transfer to the VPIC from a video capture card or motherboard video source is also possible via a dedicated I/O port.

The video display DMA channels are programmable for display window size, to support the video output scaling modes of the VPIC device and are also able to perform clipping for up to two rectangular occluding windows.

In addition to glueless connection to the VCP, the VPIC is also able to support an additional, I/O mapped device. This feature is useful for setup of video, audio capture or presentation devices, or for control of other peripheral devices.

FEATURES

- Glueless interface to IIT MPA family
- Support for 32 or 64 bit PCI
- Zero waitstate operation for 33MHz PCI
- Fully PCI compliant
- Two display DMA channels for video inlay on graphics accelerator cards
- Programmable clipping for up to two rectangular overlapping windows
- Additional read and write DMA channels
- Auxiliary component host port
- Supplied with DCI driver and sample software

The VPIC can support both 32 and 64 bit PCI bus width standards. This makes multimedia subsystem designs using VPIC and VCP easily transportable between a number of PC and workstation platforms.

Supplied in a low cost, 160 PQFP package, the VPIC plus VCP or MPP combination is the best solution for real time MPEG decoding, MPEG authoring, high speed JPEG acceleration, real-time video conferencing and a wide range of advanced multimedia applications.

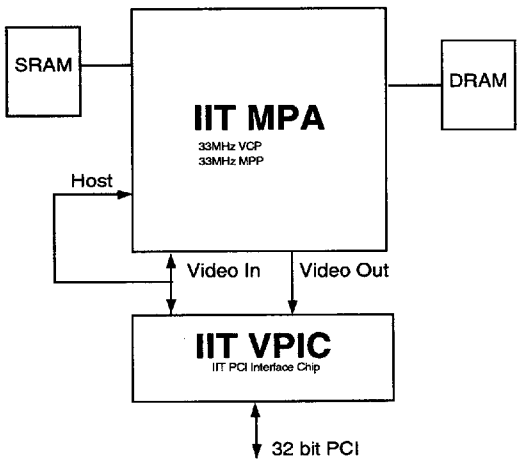

Figure 1 . VPIC System

2445 Mission College Boulevard, Santa Clara, California 95054. Telephone (408) 727-1885. Fax (408) 980-0432

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MPEG is the Moving Picture Experts Group of the ISO/IEC. References to "MPEG" in this document refer to the ISO/IEC JTC1 SC29 committee draft ISO 11172 dated 9th Jan 1992.

H.261 refers to the International Standard described in recommendation H.261 of the CCITT Working Party 15-1.

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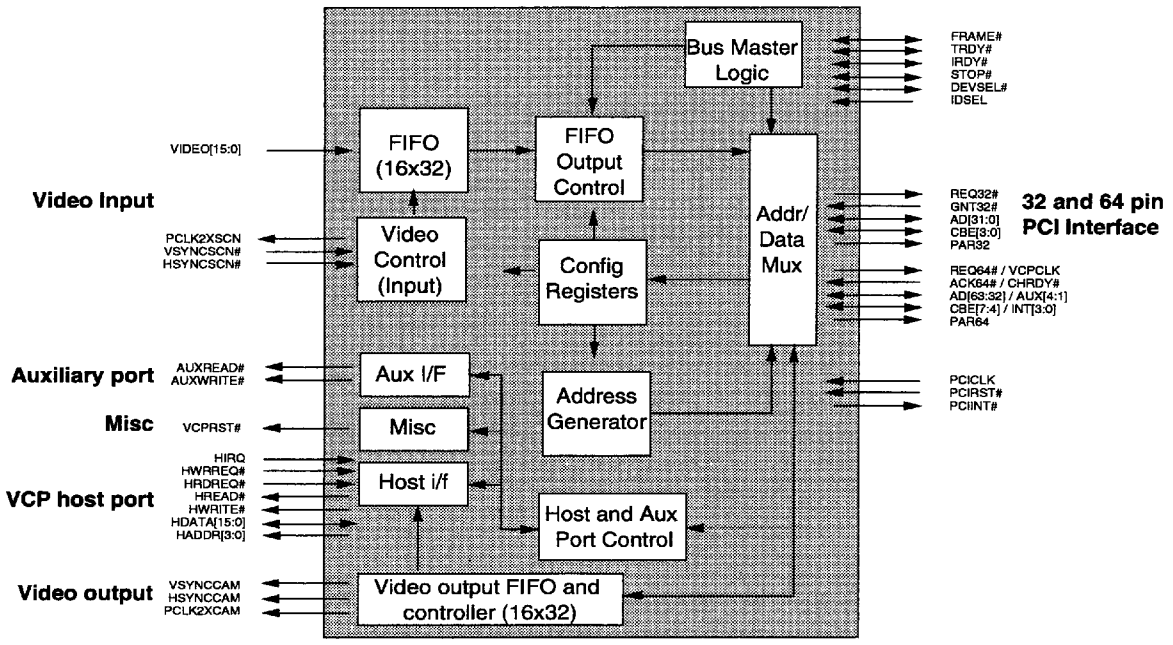

Figure 2. VPIC Block Diagram

INTRODUCTION

Figure 2 shows the block diagram of the VPIC chip. The VPIC has full 32 or 64 bit PCI bus implementation including the additional hardware for plug and play. The VPIC has the ability to Master the PCI bus and can be programmed for variable latency buses.

The VPIC provides a glueless, PCI, interface to the IIT Video Compression Processor (VCP), Multimedia Playback processor (MPP) device and other members of the IIT Multimedia Processor Architecture (MPA) family. In addition, the VPIC is able to control additional devices, such as a RAMDAC or video capture chip, via an additional pair of read and write strobes called AUXREAD# and AUXWRITE#. The VPIC maps setup and control addresses for the VCP and auxiliary device into the PCI address space enabling convenient control of the peripherals.

The VPIC can slave to, or be master of, 4 DMA channels. Two channels are used for video output, the remaining two channels are used for data I/O and are targetted at the Host port. With the exception of the two display DMA channels, each of the DMA channels has an associated on chip FIFO to improve DMA transfer efficiency. The two display DMA channels share a FIFO. When in slave mode the VPIC appears as a memory mapped device, occupying 4K locations per channel.

The VPIC Video Input port connects directly to the VCP or MPP video output or "screen" port. Video clock timing is derived from the PCI clock and is selectable to be equal to, or half of, the PCI clock frequency. The timing of horizontal and vertical sync is supplied by a programmable CRT controller on the VCP. The VPIC controls the supply of video data by gating the video clock of the VCP.

The VPIC is able to take 16 or 24 bit data from the VCP and map this into Trucolor, 16 bit or 8 bit per pixel data formats suitable for Display Controller Interface (DCI) compatible video and graphics devices. In 8 bit mode the pixel values are dithered to enhance the subjective image quality and may be used as the index to a color palette or lookup table.

It is often useful to define GUI objects that overlap the video window. The VPIC can clip two, programmable, rectangular segments from each video display channel before the video is transferred to the display device.

To allow video capture from additional capture cards or motherboard based video resources the VPIC connects to the VCP video input bus. The host port is used to carry data from the VPIC chip to the VCP, the pixel clock is used to indicate valid pixels on the bus. Video timing is derived from timing sent to the VPIC by the video source through the VSYNCCAM and HSYNCCAM pins.

FUNCTIONAL DESCRIPTION

VIDEO PORT

The Video Input port VIDEO[15:0] is used to connect the VPIC to the YSCN[7:0] and UVSCN[7:0] ports of the VCP chip or equivalent video source. Figures 6 to 11 show the input and output connectivity for each mode of the VPIC.

The video clock (PCLK2XSCN) is generated by the VPIC and is used to control the rate of transfer of video data from the VCP to the video port. The PCI bus clock is usually 33MHz and this rate can be output on the PCLK2XSCN pin. The VCP device can support video clock rates up to, but not exceeding VCP CPUCLK; if the VCP CPUCLK rate is less than the PCI clock rate then the PCLK2XSCN should be selected to be half speed, by resetting the Double_clock bit inside the VPIC.

The expected screen width is pre-programmed in to the VPIC to enable the chip to generate the addresses correctly for the display active region. Pixels outside this area are assumed blank and are ignored. VCP HSYNCSCN signal is programmed to supply a horizontal reference that allows the VPIC to place the video in the correct place in the target screen area. The maximum screen width is 2047 pixels, the maximum screen height is limited by the VCP or the display driver and is reset by the VSYNCSCN signal.

The VSYNCSCN and HSYNCSCN signals give the VPIC a reference point for the first line and first pixel on the screen, however, in most video implementations, pixels at these locations are usually blank. To avoid unnecessary DMA traffic, blank pixels are not transmitted. By programming the DMA Index registers the user can alert the VPIC to the location of active video between the sync pulses, and also the areas of interest within a larger active screen region. Figure 3 shows a typical MPEG SIF screen with overlay segment definitions.

The VPIC has two video output DMA channels, each channel can output a live video stream to be inlaid

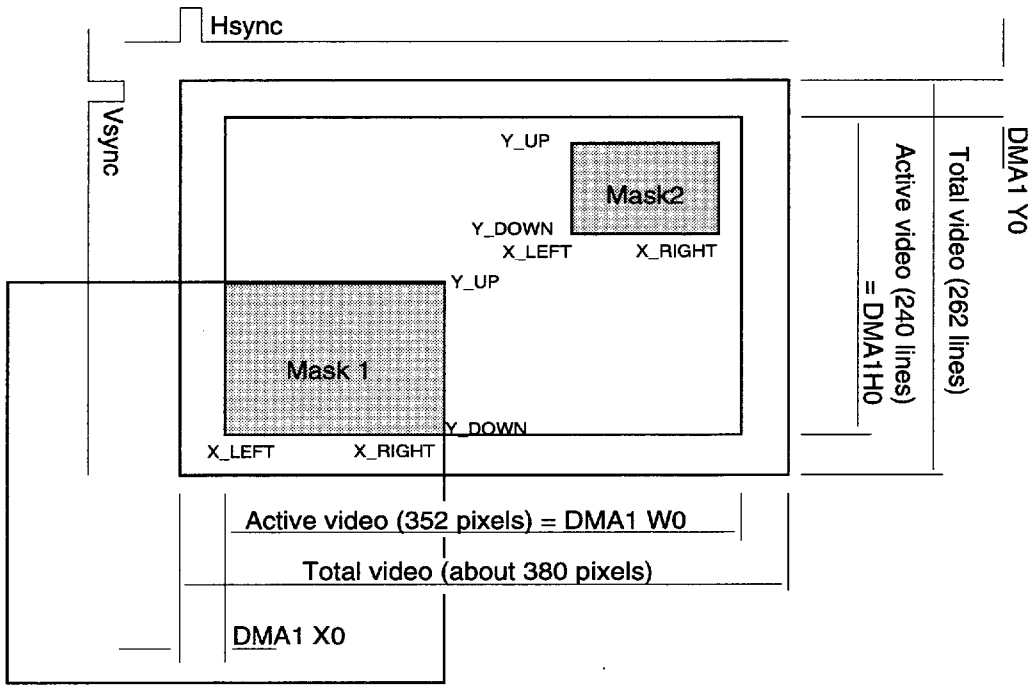

Figure 3. VPIC Video Input Timing

into the system graphics accelerator memory for display. Since only one display DMA channel can write data to the graphics subsystem at any one time, the display DMA channels share the VPIC display FIFO. The destination of the FIFOs output is alternately controlled by DMA channel 1 and 2 control settings. This swapping of control is performed on the VCP vertical sync signal, VSYNCSCN.

Each of the VPICs video display channels is able to define 2 rectangular clipping masks that restrict video output to locations under the mask. This is useful for situations where the video window is sent into the background, reducing bus bandwidth and graphics processing cycles.

The VCP is capable of generating both progressive and interlaced screen output. The VPIC is unable to recognize interlaced images and should only be used in progressive mode.

Figures 4 and 5 show the AC timing of the VPIC video input bus. The VPIC outputs the PCLK2XSCN clock to the VCP and latches the data on the VIDEO[15:0] bus on the fallingedge of this clock.

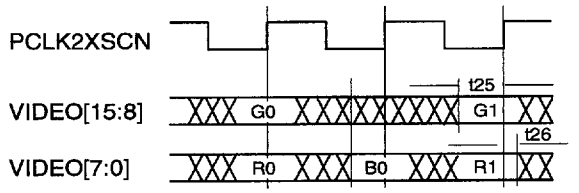

Figure 4. 1x Clock Video Out Bus Timing

Symbol	Description	33MHz	
		Min	Max
t6	PCLK2XCAM and PCLK2XSCN period	30ns	-
t23	Video data and syncs setup time to PCLK2XSCN	6ns	-
t24	Video data and syncs hold time to PCLK2XSCN	2ns	-

Figure 5. Video Port Timing

VIDEO OUPUT

The VPIC video output DMA channel can share data lines with the Host Port, but has independent clock and timing.

The target for video transfers from the PCI bus through the VPIC (VCP or other device) must be set up to take syncs and clocks from an external source and must be able to accept an irregular pixel clock timing. The VPIC drives the pixel clock whenever the data on the Host Port is for the video channel. This data may include blanking period. The VSYNCCAM and HSYNCCAM signals are also synchronous to the PCLK2XCAM clock.

Figure 7 shows the timing of the video port driven by the video input I/O channel. The input video I/O channel has a 4x32 bit data fifo to improve the efficiency of video Transfer.

The VCP chip requires video input to be in 16 bit Y, UV (4:2:2) format. Two 16 bit samples can be packed into one 32 bit video input word.

	Description	33MHz	
		Min	Max
t26	PCLK2XCAM to HDATA output delay	0	8ns

Figure 6. VPIC to VCP Video Timing

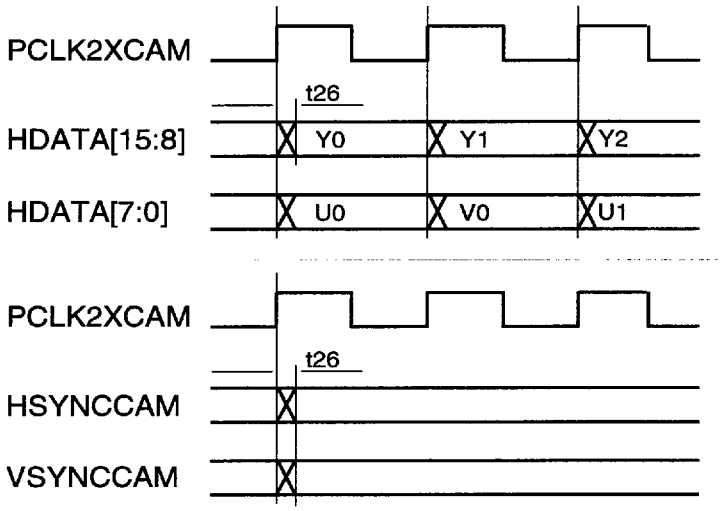

Figure 7. HDATA and Syncs for Video from VPIC to VCP

VIDEO FORMATS

The VPIC is able to supply 4x8, 2x15, 2x16 and 1x24+alpha bit formats to the PCI bus for transfer to the graphics display. The VPIC is also able to accept either 16 bit or 24 bit RGB data from the VCP, or any other video source.

Figures 8 and 9 show the component maps for the 16-bit color modes. In 16 bit to 2x15 bit mode two, 16 bit, words of video data are mapped into one 32 bit word of PCI data. The first word to enter the VPIC is packed into the least significant 15 bits of the output word. The second word is packed into the most significant bits. The extra bit (bits 31 and 15) are always zero. The blue component loses bit 0 which is cropped, not rounded.

16 bit to 2x16 bit mode is similar to the 16 bit to 2x15 bit mode with the exception that all of the video data is used. This is shown in Figure 9.

Video input 16 bit format
Video output 2x15 bit

	VPIC[31:0]	
	0	31
	R[7]	30
	R[6]	29
	R[5]	28
	R[4]	27
	R[3]	26
	G[7]	25
	G[6]	24
	G[5]	23
	G[4]	22
	G[3]	21
	B[7]	20
	B[6]	19
	B[5]	18
	B[4]	17
	B[3]	16

VCP			VPIC VIDEO[15:0]			
Pins\time	K	K+1	Pins\time	K	K+1	
Y[7]	R1[7]	R2[7]	VIDEO[15]	R1[7]	R2[7]	0
Y[6]	R1[6]	R2[6]	VIDEO[14]	R1[6]	R2[6]	R1[7]
Y[5]	R1[5]	R2[5]	VIDEO[13]	R1[5]	R2[5]	R1[6]
Y[4]	R1[4]	R2[4]	VIDEO[12]	R1[4]	R2[4]	R1[5]
Y[3]	R1[3]	R2[3]	VIDEO[11]	R1[3]	R2[3]	R1[4]
Y[2]	G1[7]	G2[7]	VIDEO[10]	G1[7]	G2[7]	R1[3]
Y[1]	G1[6]	G2[6]	VIDEO[9]	G1[6]	G2[6]	G1[7]
Y[0]	G1[5]	G2[5]	VIDEO[8]	G1[5]	G2[5]	G1[6]
UV[7]	G1[4]	G2[4]	VIDEO[7]	G1[4]	G2[4]	G1[5]
UV[6]	G1[3]	G2[3]	VIDEO[6]	G1[3]	G2[3]	G1[4]
UV[5]	G1[2]	G2[2]	VIDEO[5]	G1[2]	G2[2]	G1[3]
UV[4]	B1[7]	B2[7]	VIDEO[4]	B1[7]	B2[7]	B1[7]
UV[3]	B1[6]	B2[6]	VIDEO[3]	B1[6]	B2[6]	B1[6]
UV[2]	B1[5]	B2[5]	VIDEO[2]	B1[5]	B2[5]	B1[5]
UV[1]	B1[4]	B2[4]	VIDEO[1]	B1[4]	B2[4]	B1[4]
UV[0]	B1[3]	B2[3]	VIDEO[0]	B1[3]	B2[3]	B1[3]

Figure 8. Map of 16 bit RGB to 2x15 bit, via VPIC

Video input 16 bit format
Video output 2x16 bit

	VPIC[31:0]	
	R2[7]	31
	R2[6]	30
	R2[5]	29
	R2[4]	28
	R2[3]	27
	G2[7]	26
	G2[6]	25
	G2[5]	24
	G2[4]	23
	G2[3]	22
	G2[2]	21
	B2[7]	20
	B2[6]	19
	B2[5]	18
	B2[4]	17
	B2[3]	16

VCP			VPIC VIDEO[15:0]			
Pins\time	K	K+1	Pins\time	K	K+1	
Y[7]	R1[7]	R2[7]	VIDEO[15]	R1[7]	R2[7]	R1[7]
Y[6]	R1[6]	R2[6]	VIDEO[14]	R1[6]	R2[6]	R1[6]
Y[5]	R1[5]	R2[5]	VIDEO[13]	R1[5]	R2[5]	R1[5]
Y[4]	R1[4]	R2[4]	VIDEO[12]	R1[4]	R2[4]	R1[4]
Y[3]	R1[3]	R2[3]	VIDEO[11]	R1[3]	R2[3]	R1[3]
Y[2]	G1[7]	G2[7]	VIDEO[10]	G1[7]	G2[7]	G1[7]
Y[1]	G1[6]	G2[6]	VIDEO[9]	G1[6]	G2[6]	G1[6]
Y[0]	G1[5]	G2[5]	VIDEO[8]	G1[5]	G2[5]	G1[5]
UV[7]	G1[4]	G2[4]	VIDEO[7]	G1[4]	G2[4]	G1[4]
UV[6]	G1[3]	G2[3]	VIDEO[6]	G1[3]	G2[3]	G1[3]
UV[5]	G1[2]	G2[2]	VIDEO[5]	G1[2]	G2[2]	G1[2]
UV[4]	B1[7]	B2[7]	VIDEO[4]	B1[7]	B2[7]	B1[7]
UV[3]	B1[6]	B2[6]	VIDEO[3]	B1[6]	B2[6]	B1[6]
UV[2]	B1[5]	B2[5]	VIDEO[2]	B1[5]	B2[5]	B1[5]
UV[1]	B1[4]	B2[4]	VIDEO[1]	B1[4]	B2[4]	B1[4]
UV[0]	B1[3]	B2[3]	VIDEO[0]	B1[3]	B2[3]	B1[3]

Figure 9. Map of 16 bit RGB to 2x16bit, via VPIC

Figures 10 and 11 show the component maps for 24 bit color modes. When configured in 24 bit mode, the VCP transfers G on the Y channel and RB multiplexed on the UV channel. RGB is a fully sampled color space, which means that the same G information is output twice, once for each R and B component. The VPIC chip does not need to sample G twice; G is sampled at the same time as R.

Some graphics adapters can accept YUV color space. In this case, in the output PCI word, G maps to Y, R maps to U and B maps to V.

The most significant 8 bits of the 32 bit PCI word is not needed for the color information. This byte is programmable via a VPIC register to any value and can be used for brightness, transparency or keying information.

Additionally, the VPIC is able to swap the R and B channels to create BGR video for applications that require this. This is shown in Figure 11.

Video input 24 bit.
Video output 24 bit BGR + 8 bit alpha

VPIC[31:0]	
a[7]	31
a[6]	30
a[5]	29
a[4]	28
a[3]	27
a[2]	26
a[1]	25
a[0]	24
B[7]	23
B[6]	22
B[5]	21
B[4]	20
B[3]	19
B[2]	18
B[1]	17
B[0]	16

VCP			VPIC VIDEO[15:0]				
Pins\time	K	K+1	Pins\time	K	K+1		
Y[7]	G[7]	G[7]	VIDEO[15]	G[7]	x	G[7]	15
Y[6]	G[6]	G[6]	VIDEO[14]	G[6]	x	G[6]	14
Y[5]	G[5]	G[5]	VIDEO[13]	G[5]	x	G[5]	13
Y[4]	G[4]	G[4]	VIDEO[12]	G[4]	x	G[4]	12
Y[3]	G[3]	G[3]	VIDEO[11]	G[3]	x	G[3]	11
Y[2]	G[2]	G[2]	VIDEO[10]	G[2]	x	G[2]	10
Y[1]	G[1]	G[1]	VIDEO[9]	G[1]	x	G[1]	9
Y[0]	G[0]	G[0]	VIDEO[8]	G[0]	x	G[0]	8
UV[7]	R[7]	B[7]	VIDEO[7]	R[7]	B[7]	R[7]	7
UV[6]	R[6]	B[6]	VIDEO[6]	R[6]	B[6]	R[6]	6
UV[5]	R[5]	B[5]	VIDEO[5]	R[5]	B[5]	R[5]	5
UV[4]	R[4]	B[4]	VIDEO[4]	R[4]	B[4]	R[4]	4
UV[3]	R[3]	B[3]	VIDEO[3]	R[3]	B[3]	R[3]	3
UV[2]	R[2]	B[2]	VIDEO[2]	R[2]	B[2]	R[2]	2
UV[1]	R[1]	B[1]	VIDEO[1]	R[1]	B[1]	R[1]	1
UV[0]	R[0]	B[0]	VIDEO[0]	R[0]	B[0]	R[0]	0

Figure 10. Map of 24 bit to 24 bit + alpha, via VPIC

Video input 24 bit.
Video output 24 bit RGB + 8 bit alpha

VPIC[31:0]	
a[7]	31
a[6]	30
a[5]	29
a[4]	28
a[3]	27
a[2]	26
a[1]	25
a[0]	24
R[7]	23
R[6]	22
R[5]	21
R[4]	20
R[3]	19
R[2]	18
R[1]	17
R[0]	16

VCP			VPIC VIDEO[15:0]				
Pins\time	K	K+1	Pins\time	K	K+1		
Y[7]	G[7]	G[7]	VIDEO[15]	G[7]	x	G[7]	15
Y[6]	G[6]	G[6]	VIDEO[14]	G[6]	x	G[6]	14
Y[5]	G[5]	G[5]	VIDEO[13]	G[5]	x	G[5]	13
Y[4]	G[4]	G[4]	VIDEO[12]	G[4]	x	G[4]	12
Y[3]	G[3]	G[3]	VIDEO[11]	G[3]	x	G[3]	11
Y[2]	G[2]	G[2]	VIDEO[10]	G[2]	x	G[2]	10
Y[1]	G[1]	G[1]	VIDEO[9]	G[1]	x	G[1]	9
Y[0]	G[0]	G[0]	VIDEO[8]	G[0]	x	G[0]	8
UV[7]	R[7]	B[7]	VIDEO[7]	R[7]	B[7]	B[7]	7
UV[6]	R[6]	B[6]	VIDEO[6]	R[6]	B[6]	B[6]	6
UV[5]	R[5]	B[5]	VIDEO[5]	R[5]	B[5]	B[5]	5
UV[4]	R[4]	B[4]	VIDEO[4]	R[4]	B[4]	B[4]	4
UV[3]	R[3]	B[3]	VIDEO[3]	R[3]	B[3]	B[3]	3
UV[2]	R[2]	B[2]	VIDEO[2]	R[2]	B[2]	B[2]	2
UV[1]	R[1]	B[1]	VIDEO[1]	R[1]	B[1]	B[1]	1
UV[0]	R[0]	B[0]	VIDEO[0]	R[0]	B[0]	B[0]	0

Figure 11. Map of 24 bit to 24 bit + alpha,via VPIC

Figure 12 shows the color component map for 16 bit RGB input to 4x8 bit RGB. In this mode the video source supplies four 16 bit pixels which are dithered and reduced to 8 bit pixels and then packed into a single 32 bit PCI transfer.

16 bit RGB is output from the VCP as 5 bits of R, 6 of G and 5 of B. The 8 bit pixel format consists of 3 bits R, 3 bits G and 2 bits B. The LSB's are rounded/ clipped differently for odd/even pixels and lines to create a broader color range and to increase perceived video quality.

Video Input 16 bit.
Video output 4x8 bit dithered

	VCP					VPIC VIDEO[15:0]				VPICAD[31:0]	
Pins\time	K	K+1	K+2	K+3	Pins\time	K	K+1	K+2	K+3		
Y[7]	R1[7]	R2[7]	R3[7]	R4[7]	VIDEO[15]	R1[7]	R2[7]	R3[7]	R4[7]	R4[7]	31
Y[6]	R1[6]	R2[6]	R3[6]	R4[6]	VIDEO[14]	R1[6]	R2[6]	R3[6]	R4[6]	R4[6]	30
Y[5]	R1[5]	R2[5]	R3[5]	R4[5]	VIDEO[13]	R1[5]	R2[5]	R3[5]	R4[5]	R4[5]	29
Y[4]	R1[4]	R2[4]	R3[4]	R4[4]	VIDEO[12]	R1[4]	R2[4]	R3[4]	R4[4]	G4[7]	28
Y[3]	R1[3]	R2[3]	R3[3]	R4[3]	VIDEO[11]	R1[3]	R2[3]	R3[3]	R4[3]	G4[6]	27
Y[2]	G1[7]	G2[7]	G3[7]	G4[7]	VIDEO[10]	G1[7]	G2[7]	G3[7]	G4[7]	G4[5]	26
Y[1]	G1[6]	G2[6]	G3[6]	G4[6]	VIDEO[9]	G1[6]	G2[6]	G3[6]	G4[6]	B4[7]	25
Y[0]	G1[5]	G2[5]	G3[5]	G4[5]	VIDEO[8]	G1[5]	G2[5]	G3[5]	G4[5]	B4[6]	24
UV[7]	G1[4]	G2[4]	G3[4]	G4[4]	VIDEO[7]	G1[4]	G2[4]	G3[4]	G4[4]	R3[7]	23
UV[6]	G1[3]	G2[3]	G3[3]	G4[3]	VIDEO[6]	G1[3]	G2[3]	G3[3]	G4[3]	R3[6]	22
UV[5]	G1[2]	G2[2]	G3[2]	G4[2]	VIDEO[5]	G1[2]	G2[2]	G3[2]	G4[2]	R3[5]	21
UV[4]	B1[7]	B2[7]	B3[7]	B4[7]	VIDEO[4]	B1[7]	B2[7]	B3[7]	B4[7]	G3[7]	20
UV[3]	B1[6]	B2[6]	B3[6]	B4[6]	VIDEO[3]	B1[6]	B2[6]	B3[6]	B4[6]	G3[6]	19
UV[2]	B1[5]	B2[5]	B3[5]	B4[5]	VIDEO[2]	B1[5]	B2[5]	B3[5]	B4[5]	G3[5]	18
UV[1]	B1[4]	B2[4]	B3[4]	B4[4]	VIDEO[1]	B1[4]	B2[4]	B3[4]	B4[4]	B3[7]	17
UV[0]	B1[3]	B2[3]	B3[3]	B4[3]	VIDEO[0]	B1[3]	B2[3]	B3[3]	B4[3]	B3[6]	16
										R2[7]	15
										R2[6]	14
										R2[5]	13
										G2[7]	12
										G2[6]	11
										G2[5]	10
										B2[7]	9
										B2[6]	8
										R1[7]	7
										R1[6]	6
										R1[5]	5
										G1[7]	4
										G1[6]	3
										G1[5]	2
										B1[7]	1
										B1[6]	0

Figure 12. 16 bit RGB to 4 x 8 bit Dithered Video

The VPIC is also able to map 24 bit incoming video into the 8 bits per pixel format. Figure 13 shows the component map of the 4x24 bit to 4x8 bit transfer mode. As before with 24 bit mode, the VPIC samples the G component at the same time as the R component and ignores the 8 MSB's of the VIDEO bus during the B transfer cycle.

24 bit video comprises 8 bits for each of the color components. This is reduced to 3 each for R and G and to 2 bit for B. The dithering is done by rounding differently according to horizontal pixel position and line number.

Video input 24 bit RGB. Video output 4x8 bit dithered

VPIC AD[31:0]		
R1[7]	R4[7]	31
R1[6]	R4[6]	30
R1[5]	R4[5]	29
G1[7]	G4[7]	28
G1[6]	G4[6]	27
G1[5]	G4[5]	26
B1[7]	B4[7]	25
B1[6]	B4[6]	24
R2[7]	R3[7]	23
R2[6]	R3[6]	22
R2[5]	R3[5]	21
G2[7]	G3[7]	20
G2[6]	G3[6]	19
G2[5]	G3[5]	18
B2[7]	B3[7]	17
B2[6]	B3[6]	16
R3[7]	R2[7]	15
R3[6]	R2[6]	14
R3[5]	R2[5]	13
G3[7]	G2[7]	12
G3[6]	G2[6]	11
G3[5]	G2[5]	10
B3[7]	B2[7]	9
B3[6]	B2[6]	8
R4[7]	R1[7]	7
R4[6]	R1[6]	6
R4[5]	R1[5]	5
G4[7]	G1[7]	4
G4[6]	G1[6]	3
G4[5]	G1[5]	2
B4[7]	B1[7]	1
B4[6]	B1[6]	0

VCP									VPIC VIDEO[15:0]								
Pin\T	K	K+1	K+2	K+3	K+4	K+5	K+6	K+7	Pins\time	K	K+1	K+2	K+3	K+4	K+5	K+6	K+7
Y[7]	G1[7]	G1[7]	G2[7]	G2[7]	G3[7]	G3[7]	G4[7]	G4[7]	VIDEO[15]	x	G1[7]	x	G2[7]	x	G3[7]	x	G4[7]
Y[6]	G1[6]	G1[6]	G2[6]	G2[6]	G3[6]	G3[6]	G4[6]	G4[6]	VIDEO[14]	x	G1[6]	x	G2[6]	x	G3[6]	x	G4[6]
Y[5]	G1[5]	G1[5]	G2[5]	G2[5]	G3[5]	G3[5]	G4[5]	G4[5]	VIDEO[13]	x	G1[5]	x	G2[5]	x	G3[5]	x	G4[5]
Y[4]	G1[4]	G1[4]	G2[4]	G2[4]	G3[4]	G3[4]	G4[4]	G4[4]	VIDEO[12]	x	G1[4]	x	G2[4]	x	G3[4]	x	G4[4]
Y[3]	G1[3]	G1[3]	G2[3]	G2[3]	G3[3]	G3[3]	G4[3]	G4[3]	VIDEO[11]	x	G1[3]	x	G2[3]	x	G3[3]	x	G4[3]
Y[2]	G1[2]	G1[2]	G2[2]	G2[2]	G3[2]	G3[2]	G4[2]	G4[2]	VIDEO[10]	x	G1[2]	x	G2[2]	x	G3[2]	x	G4[2]
Y[1]	G1[1]	G1[1]	G2[1]	G2[1]	G3[1]	G3[1]	G4[1]	G4[1]	VIDEO[9]	x	G1[1]	x	G2[1]	x	G3[1]	x	G4[1]
Y[0]	G1[0]	G1[0]	G2[0]	G2[0]	G3[0]	G3[0]	G4[0]	G4[0]	VIDEO[8]	x	G1[0]	x	G2[0]	x	G3[0]	x	G4[0]
UV[7]	R1[7]	B1[7]	R2[7]	B2[7]	R3[7]	B3[7]	R4[7]	B4[7]	VIDEO[7]	R1[7]	B1[7]	R2[7]	B2[7]	R3[7]	B3[7]	R4[7]	B4[7]
UV[6]	R1[6]	B1[6]	R2[6]	B2[6]	R3[6]	B3[6]	R4[6]	B4[6]	VIDEO[6]	R1[6]	B1[6]	R2[6]	B2[6]	R3[6]	B3[6]	R4[6]	B4[6]
UV[5]	R1[5]	B1[5]	R2[5]	B2[5]	R3[5]	B3[5]	R4[5]	B4[5]	VIDEO[5]	R1[5]	B1[5]	R2[5]	B2[5]	R3[5]	B3[5]	R4[5]	B4[5]
UV[4]	R1[4]	B1[4]	R2[4]	B2[4]	R3[4]	B3[4]	R4[4]	B4[4]	VIDEO[4]	R1[4]	B1[4]	R2[4]	B2[4]	R3[4]	B3[4]	R4[4]	B4[4]
UV[3]	R1[3]	B1[3]	R2[3]	B2[3]	R3[3]	B3[3]	R4[3]	B4[3]	VIDEO[3]	R1[3]	B1[3]	R2[3]	B2[3]	R3[3]	B3[3]	R4[3]	B4[3]
UV[2]	R1[2]	B1[2]	R2[2]	B2[2]	R3[2]	B3[2]	R4[2]	B4[2]	VIDEO[2]	R1[2]	B1[2]	R2[2]	B2[2]	R3[2]	B3[2]	R4[2]	B4[2]
UV[1]	R1[1]	B1[1]	R2[1]	B2[1]	R3[1]	B3[1]	R4[1]	B4[1]	VIDEO[1]	R1[1]	B1[1]	R2[1]	B2[1]	R3[1]	B3[1]	R4[1]	B4[1]
UV[0]	R1[0]	B1[0]	R2[0]	B2[0]	R3[0]	B3[0]	R4[0]	B4[0]	VIDEO[0]	R1[0]	B1[0]	R2[0]	B2[0]	R3[0]	B3[0]	R4[0]	B4[0]

Figure 13. 24 bit RGB Component Map to 4x8 bit Dithered

PCI INTERFACE

The IIT VPIC supports both 32 bit and 64 bit PCI interfaces at speeds up to 33MHz. The PCI interface may be used in either DMA master mode or slave mode for each of the 4 DMA channels.

CONFIGURATION REGISTERS

Figure 14 shows the VPIC PCI configuration space registers. These registers are accessed during the initial setup of the PCI interface and allow the OS to retrieve the various IDs, to set up the DMAs to be master or slave and to configure the interrupt level and master latency of the device.

The configuration registers also hold the base address for the control I/O space and the base addresses for the DMA channels in slave mode.

Offset	Range	Type	Register	Default value
00h	31:16	RO	Device ID	0002h
	15:0	RO	Vendor ID	1061h
04h	29	RR	Master Abort Detected. A value of 1 indicates that a master abort has been detected. Writing a 1 will reset this bit.	
	28	RR	Target Abort Detected. A value of 1 indicates that a target abort has been detected. Writing a 1 will reset this bit.	
	26:25	RO	DEVSEL# timing, Medium device	01b
	2	RW	Master Enable. (1 to enable bus master).	0
	1	RW	Memory Enable (1 to enable memory space)	0
	0	RW	IO Enable (1 to enable I/O space)	0
08h	31:8	RO	Class Code. The code for "Multimedia Other Device" is returned.	048000h
	7:0	RO	Revision ID	02h
0Ch	23	RO	Header Type. Single function device.	0
	22:16	RO	Header Type	0000000b
	15:8	RW	Latency Timer. Specifies the number of PCI clocks between de-assertion of GNT# and the master releasing ownership of the PCI bus.	
10h	31:0	RW	Base Address for 256 byte IO space	
14h	31:0	RW	Base Address for 4K byte Memory space. Display FIFO.	
18h	31:0	RW	Base Address for 4K byte Memory space. Host Read.	
1Ch	31:0	RW	Base Address for 4K byte Memory space. Host write.	
20h	31:0	RW	Base Address for 4K byte Memory space. Capture FIFO.	
3Ch	15:11	RO	Interrupt Pin	00000b
	10:8	RO	Indicates which INT lines is connected.	INTA#
	7:0	RW	Interrupt Line	

RO: Read only

RW: Read write

RR: Read/Reset (Write a "1" to reset).

Figure 14. VPIC Configuration Register Map

CONTROL I/O

The control I/O map is detailed in Figure 15. The space is split between the VCP, the VPIC internal registers and the auxiliary port. To reduce the amount of I/O space used by the VPIC, an additional level of indirection is used for accessing some internal registers. The index register within the control I/O address space is set with the target register address and then the data is sent to address 0x030.

Details of the Control, Interrupt Mask and Interrupt Status registers are shown in Figures 15a, 15b and 15c.

PCI address	Name	Description
0x000	VCP DMA port	VCP DMA port, 16 bit.
0x004	VCP VCX port	VCP VCX port, 8 bit
0x008	VCP DBG port	VCP DBG port, 8 bit
0x00C	VCP hostctl	VCP Host control register, 8 bit
0x010	VCP hostmask	VCP Host irq mask register, 8 bit
0x014	VCP hostirqstat	VCP Host irq status register, 8 bit
0x020	Control Register	See Figure 15a
0x024	Interrupt Mask	See Figure 15b
0x028	Interrupt Status	See Figure 15c
0x02C	Index	Index register 8 bit
0x030	Indexed Data regs	Data register , 32 bit
0x040 - 0x07C	Auxiliary Registers	Auxiliary port

Figure 15. VPIC Control Space Map

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX[3..0] Control				AUX[3..0] Data				Reserved			Write FIFO Reset	Read FIFO Reset	Dsply FIFO Reset	VCP Reset	64-bit PCI

Figure 15a. VPIC Control Space Control Register

15-12: AUX[3..0] Control

Control signals for the AUX[3..0] pins, set to 0 for input, 1 for output.

11-8: Aux[3..0] Data

Data to be written to the AUX[3..0] pins. Only pins defined as outputs will be written. Pins defined as inputs should be read using the Status Register. Only available in 32-bit mode.

7-5: Reserved

Reserved, data written is ignored.

4: Reset DMA Write FIFO

Set to 1 to reset DMA Write FIFO.

3: Reset DMA Read FIFO

Set to 1 to reset DMA Read FIFO.

2: Reset Display FIFO

Set to 1 to reset Capture and Display FIFOs.

1: Reset VCP

Set to 1 to reset VCP.

0: 64-bit PCI

Set to 1 for 64-bit PCI bus mode.

9	8	7	6	5	4	3	2	1	0
INT[4..1]				DMA Write EOT	DMA Read EOT	Addr Cross Bndry	End of Frame	Master Abort	VCP

Figure 15b. VPIC Control Space Interrupt Mask Register

9-6: INT[4..1] Mask

Setting to 1 will cause the corresponding INT[] pin to be masked from generating a VPIC interrupt. Only available in PCI 32-bit mode.

5: DMA Write End of Transfer Mask

Masks out interrupt generated by the end of a write DMA transfer sequence.

4: DMA Read End of Transfer Mask

Masks out interrupt generated by the end of a read DMA transfer sequence.

3: Address Cross Boundary Mask

Setting prevents an interrupt being generated in the event of the address used crossing a graphics page boundary.

2: End of Frame Mask

Set to prevent End of video Frame interrupts.

1: Master Abort Mask

Set to mask out Master Abort interrupts.

0: VCP Mask

Setting prevents a VCP interrupt generating a VPIC interrupt.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX[3..0]				INT[4..1]				DMA Write EOT	DMA Read EOT	Addr Cross Bndry	End of Frame	Master Abort	VCP

Figure 15c: VPIC Control Space Interrupt Status Register

13-10: AUX[3..0] Inputs

Correspond to the state of the external AUX[] pins. Note the pins must be defined as inputs before reading in order to guarantee values read. Only available in PCI 32-bit mode.

9-6: INT[4..1] Inputs

Correspond to the state of the external INT[] pins. These pins are only defined as interrupt inputs in 32-bit PCI mode.

5: DMA Write End of Transfer Interrupt

End of write DMA transfer interrupt detected.

4: DMA Read End of Transfer Interrupt

End of read DMA transfer interrupt detected.

3: Address Cross Boundary Interrupt

Interrupt generated as address crossed graphics memory page boundary.

2: End of Frame Interrupt

End of video frame interrupt detected.

1: Master Abort Interrupt

Interrupt generated because VPIC cannot write data to target.

0: VCP Interrupt

Interrupt detected from the VCP.

INDEX REGISTERS

The internal index registers are used to control the VPIC video transfer functions, the DMA channels and the rectangular video clipping masks. The index register usage is shown in Figure 16.

Index	Name	Range	Type	Description
0x00	Screen Map Width	10:0	R W	Screen display width.
0x01	FIFO input control	0	R W	RGB mode. 0: 16-bit, 1: 24-bit
		1	R W	Color dither enable
		2	R W	Double clock
		3	R W	Pixel mode. 24-bit 0: RGB, 1: BGR 16-bit 0: 565, 1:555
		4	R W	YUV bypass mode
		31:24	R W	Upper byte data in 24bpp mode
0x02	FIFO output control	0	R W	Master enable
		1	R W	Enable 64k address checking
		2	R W	Enable 1M address checking
0x03	FIFO control	0	R W	Start operation
	Restart	1	R W	Restart from End of Frame interrupt
0x04	FIFO status	5:0	R O	Write pointer (byte)
		9:6	R O	Read pointer (longword)
0x05	PCI Master Cntl	0	R W	Restart from memory checking
		1	R W	Restart from abort
0x06	PCI Master Status	0	R O	Address cross boundary detected
		1	R O	Target abort detected
		2	R O	Master abort detected
0x07	DMA1 Y0	10:0	R W	DMA1 display Y direction begin. This value specify the offset of starting Y location.
0x08	DMA1 X0	10:0	R W	DMA1 display X direction begin. This value specify the offset of starting X location.
0x09	DMA1 W0	10:0	R W	DMA1 display width. This value indicate the display width. The sum of X0 and W0 should less or equal to Width.
0x0a	DMA1 H0	10:0	R W	DMA1 display height. This value indicate the display height. The sum of Y0 and H0 should less or equalto Height.
0x0b	DMA1 Mask1 X_left	10:0	R W	DMA1 mask1 X left pointer
0x0c	DMA1 Mask1 X_right	10:0	R W	DMA1 mask1 X right pointer
0x0d	DMA1 Mask1 Y_up	10:0	R W	DMA1 mask1 X upper pointer
0x0e	DMA1 Mask1 Y_down	10:0	R W	DMA1 mask1 X lower pointer

Figure 16. VPIC Internal Index Register

Index	Name	Range	Type	Description
0x0f	DMA1 Mask2 X_left	10:0	RW	DMA1 mask2 X left pointer
0x10	DMA1 Mask2 X_right	10:0	RW	DMA1 mask2 X right pointer
0x11	DMA1 Mask2 Y_up	10:0	RW	DMA1 mask2 X upper pointer
0x12	DMA1 Mask2 Y_down	10:0	RW	DMA1 mask2 X lower pointer
0x13	DMA1 Base Address	31:0	RW	Base address for DMA channel 1. The LSB is forced to 0. The master send data stating from this value and the width and height is specified by W0 and H0.
0x14	DMA1 Control	0	RW	DMA1 enable
		1	RW	DMA2 enable
		2	RW	DMA1 Mask1 enable
		3	RW	DMA1 Mask2 enable
		4	RW	DMA2 Mask1 enable
		5	RW	DMA2 Mask2 enable
0x15	VCP_to_HOST Add	31:0	RW	DMA VCP to Host base address
0x16	VCP_to_HOST Count	10:0	RW	DMA VCP to Host word count
0x17	HOST_to_VCP Addr	31:0	RW	DMA Host to VCP base address
0x18	HOST_to_VCP Count	10:0	RW	DMA Host to VCP word count
0x19	VCP DMA Control	0	RW	VCP DMA read master enable
		1	RW	VCP DMA read FIFO disable
		2	RW	VCP DMA write master enable
		3	RW	VCP DMA write FIFO disable
		4	RW	Enable 3 cycle Host DMA read/writes. (Default equals 1 cycle)
		6:5	RW	Host/AUX IO read/write waitstates. (Default equals 2 cycles)
		7	RW	Filter single cycle GNT# signals
		8	RW	Enable master latency timer
0x1A	CAMERA Width	10:0	RW	CAMERA input map width
0x1B	CAMERA Height	10:0	RW	CAMERA input map height
0x1C	CAMERA Control	3:0	RW	Hsync to data count 4-bit
		7:4	RW	Data to Hsync count 4-bit
		8	RW	Double Clock Output

Figure 16. Continued. VPIC Internal Index Register

Index	Name	Range	Type	Description
0x1D	DMA2 Y0	10:0	WO	DMA2 display Y direction begin. This value specifies the offset of starting Y location.
0x1E	DMA2 X0	10:0	WO	DMA2 display X direction begin. This value specifies the offset of starting X location.
0x1F	DMA2 W0	10:0	WO	DMA2 display width. This value indicate the display width. The sum of X0 and W0 should less or equal to Width.
0x20	DMA2 H0	10:0	WO	DMA2 display height. This value indicate the display height. The sum of Y0 and H0 should less or equal to Height.
0x21	DMA2 Mask1 X_left	10:0	WO	DMA2 mask1 X left pointer
0x22	DMA2 Mask1 X_right	10:0	WO	DMA2 mask1 X right pointer
0x23	DMA2 Mask1 Y_up	10:0	WO	DMA2 mask1 X upper pointer
0x24	DMA2 Mask1 Y_down	10:0	WO	DMA2 mask1 X lower pointer
0x25	DMA2 Mask2 X_left	10:0	WO	DMA2 mask2 X left pointer
0x26	DMA2 Mask2 X_right	10:0	WO	DMA2 mask2 X right pointer
0x27	DMA2 Mask2 Y_up	10:0	WO	DMA2 mask2 X upper pointer
0x28	DMA2 Mask2 Y_down	10:0	WO	DMA2 mask2 X lower pointer
0x29	DMA2 Base Address	10:0	RW	Base address for DMA channel 2. This value is specified as a standard 32-bit address, the LSB is forced to 0. The master sends data starting from this value, with the width and height specified by DMA2 W0 and H0.

Figure 16. Continued. VPIC Internal Index Register

MEMORY MAP

The VPIC memory map is shown in Figure 17. These addresses are used as targets and sources of data when the VPIC is set up in slave DMA mode. Each DMA channel is independently configured and can be a master or slave as necessary. Each DMA can be 4K works long.

Index	Name	Range	Type	Description
Config 0x14	Display FIFO data	4K	RO	DMA from the VPIC video display
Config 0x18	VCP Host data	4K	RO	DMA from VCP Host port
Config 0x1C	VCP host data	4K	WO	DMA to VCP host port
Config 0x20	Capture video data	4K	WO	DMA from PCI to video capture port

Figure 17. VPIC Slave Mode DMA Memory Map

HOST AND AUX PORT

The Host Port is used by VPIC to control the VCP and other chips on the board. In the case of the VCP it is used for initialization, program download, run-time command and control. Coded data transfer to and from the VCP can occur under some circumstances. The Host port is a generic 16-bit parallel bus which accesses six registers in the VCP. There are three ports in the Host Interface, a DMA port, a VCXI port and a Debug port, a full description of the registers and their functions are detailed in the Register Description section of the VCP datasheet. Figure 18 illustrates the timing relationships of the Host port.

The DMA port typically transfers user data to be multiplexed with the audio and video data in the video conferencing application. The DMA port is also used for MPEG bitstream transfer and for VCP executable download.

The Host port uses the HRDREQ# and HWRREQ# pins to determine the VCP's readiness to send and receive data. The HIRQ line is used by the VCP to indicate that the HOSTIRQSTAT register should be interrogated. This signal is passed to the PCI interface.

The VPIC Auxiliary port makes use of the data and address lines of the Host port and has equivalent timing and loading. The AUXREAD# and AUXWRITE# are used to read from and write data to the addressed device. Auxiliary port read and write cycles are not triggered by the HRDREQ# and HWRREQ# signals, they are the result of only programmed I/O transfers.

The Host port also controls the external device reset. This is an active low signal and is mapped into the VPIC address space.

	Description	33MHz	
		Min	Max
t10	HRREQ# and HWRREQ# strobe high time	30ns	-
t11	Read/write request to HREAD/HWRITE rising edge	30	3/5T
t12	Read/write request to stable host address delay	-	4
t13	Address hold time beyond write strobe rising edge.	4	-
t14	Write request to stable data delay	6	-
t15	Data hold time beyond write strobe rising edge	4	-
t16	Read/write request to strobe falling edge delay.	-	4
t17	Host data setup time	8	-
t18	Host data hold time	4	-

Figure 18. Host Bus Timing

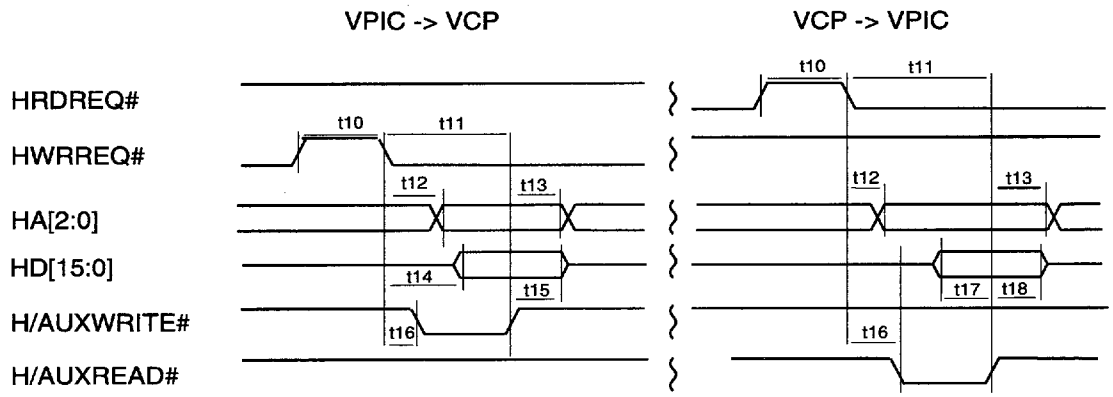

Figure 19. Host Bus Timing

PIN DESCRIPTION

Name	I/O	Definition
VIDEO[15:0]	I	Video input port from VCP to VPIC. Connect MSB to Y port and LSB to UV port.
PCLK2XSCN	O	Video input port pixel clock. Can be selected to be PCI Bus clock or half PCI bus clock.
VSYNCSCN#	I	Video input port vertical sync pulse. Is triggered on the falling edge inside VPIC.
HSYNCSCN#	I	Video input port horizontal sync pulse. Is triggered on the falling edge inside VPIC.
VSYNCCAM	O	Video output port vertical sync pulse. Is high during sync period.
HSYNCCAM	O	Video output port horizontal sync. Is high during sync period.
PCLK2XCAM	O	Video output port pixel clock. Selected to be PCI Bus clock or half PCI bus clock.
VCPRST#	O	System reset (active low). Must be low for at least 16 clock cycles to ensure chip reset.
AUXREAD#	O	Host Read. Enables data from the host interface onto the HDATA[15:0] bus.
AUXWRITE#	O	Host Write. Latches data from the HDATA[15:0] bus into the host interface registers.
HIRQ	I	Host Interrupt Request. Indicates an interrupt from the VC to the host.
HWRREQ#	I	Host DMA channel Write Request
HRDREQ#	I	Host DMA channel Read Request
HD[15:0]	I/O	Host Data Bus. Compressed data is passed to and from the VC across this bus. It is also used to pass commands and parameters from the host to the VC.
HA[3:0]	O	Host Address Bus. This bus is used by the host to address one of eight registers in the host interface.
HREAD#	O	Host Read. Enables data from the host interface onto the HDATA[15:0] bus.
HWRITE#	O	Host Write. Latches data from the HDATA[15:0] bus into the host interface registers.

Name	I/O	Definition
FRAME#	I/O	Cycle frame, indicates the beginning and duration of an access.
TRDY#	I/O	Target Ready, indicates the completeion of current data phase as a receiver.
IRDY#	I/O	Initiator ready, indicates the completion of the current data phase as a bus master.
STOP#	I/O	Indicates the current target request for transaction termination.
DEVSEL#	I/O	Device delect indicates that the driving device has decoded the address and is the target of the current transaction.
IDSEL	I	Chip select for configuration read and write cycles.
REQ32#	O	32 bit access bus request to arbiter.
GNT32#	O	32 bit access bus grant from arbiter.
AD[31:0]	I/O	Multiplexed address and data LSW.
CBE[3:0]	O	Bus command and byte enables
PAR32	O	Indicates even parity across AD[31:0] and CBE[3:0].
REQ64#/VCPCLK	O	64 bit access bus request to arbiter / VCP clock.
ACK64#/CHRDY#	I	64 bit access bus grant from arbiter / Auxiliary waitstate insertion.
AD[63:60]/AUX[3:0]	I/O	Multiplexed address and data MSW / Auxiliary IO.
AD[59:32]	I/O	Multiplexed address and data MSW.
CBE[7:4]/INT[4:1]	I/O	Bus command and byte enables / Auxiliary interrupt inputs.
PAR64	O	Indicates even parity across AD[63:32] and CBE[3:0].
PCICLK	I	PCI clock, usually 33MHz.
PCIRST#	I	PCI device reset.
PCIINT#	O	Interrupt passed from input HIRQ pin.

PINOUT 160 PIN QUAD FLAT PACK

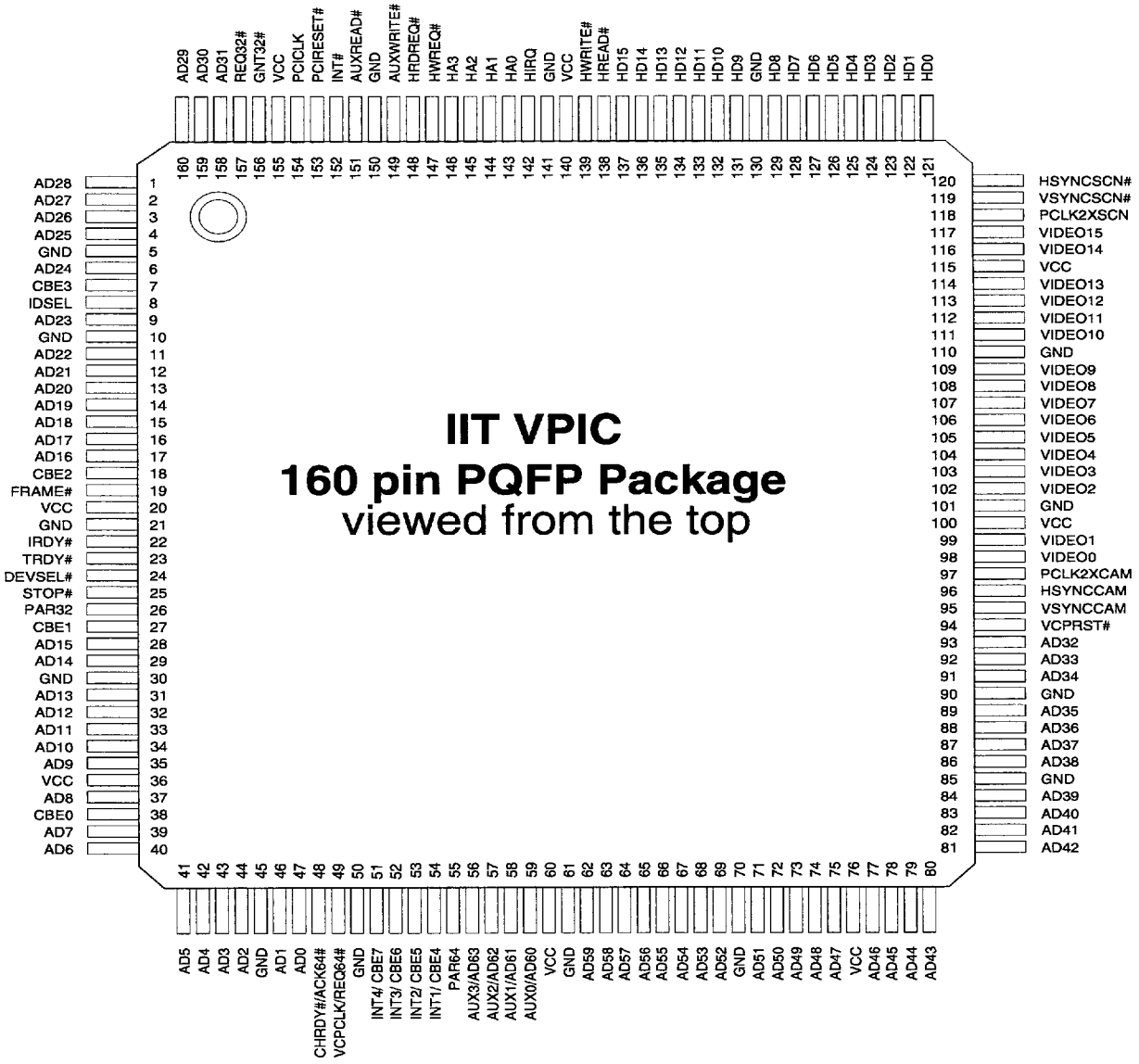

Figure 20. Pinout 160 Pin VPIC

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	-65°C to 110°C
Voltage Range on any Pin	-0.5V to (Vcc + 0.5V)
Power Dissipation	__ Watts @ 33MHz

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range	0°C to 70°C
Supply Voltage Vcc	4.75V to 5.25V

DC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Notes
Vih	High Level Input Voltage	2.0	Vcc+0.25	V	All inputs TTL levels except CLK
Vil	Low Level Input Voltage	-0.3	0.8	V	All inputs TTL levels except CLK
Vch	CLK High Level Input	3.7	Vcc+0.25	V	CMOS level input
Vcl	CLK Low Level Input	-0.3	0.8	V	CMOS level input
Voh	High Level Ouptput Voltage	3.0	-	V	IOH = 1mA
Vol	Low Level Output Voltage	-	0.45	V	IOL = 4mA
Ili	Input Leakage Current	-	±15	µA	
Ilo	Output Leakage Current	-	±15	µA	
Cin	Input Capacitance	-	10	pF	fc = 1 MHz
Co	Input/Output Capacitance	-	12	pF	fc = 1 MHz
Cclk	CLK Capacitance	-	20	pF	fc = 1 MHz

Figure 21. DC Electrical Characteristics

MECHANICAL

160-LEAD QUAD FLAT PACK

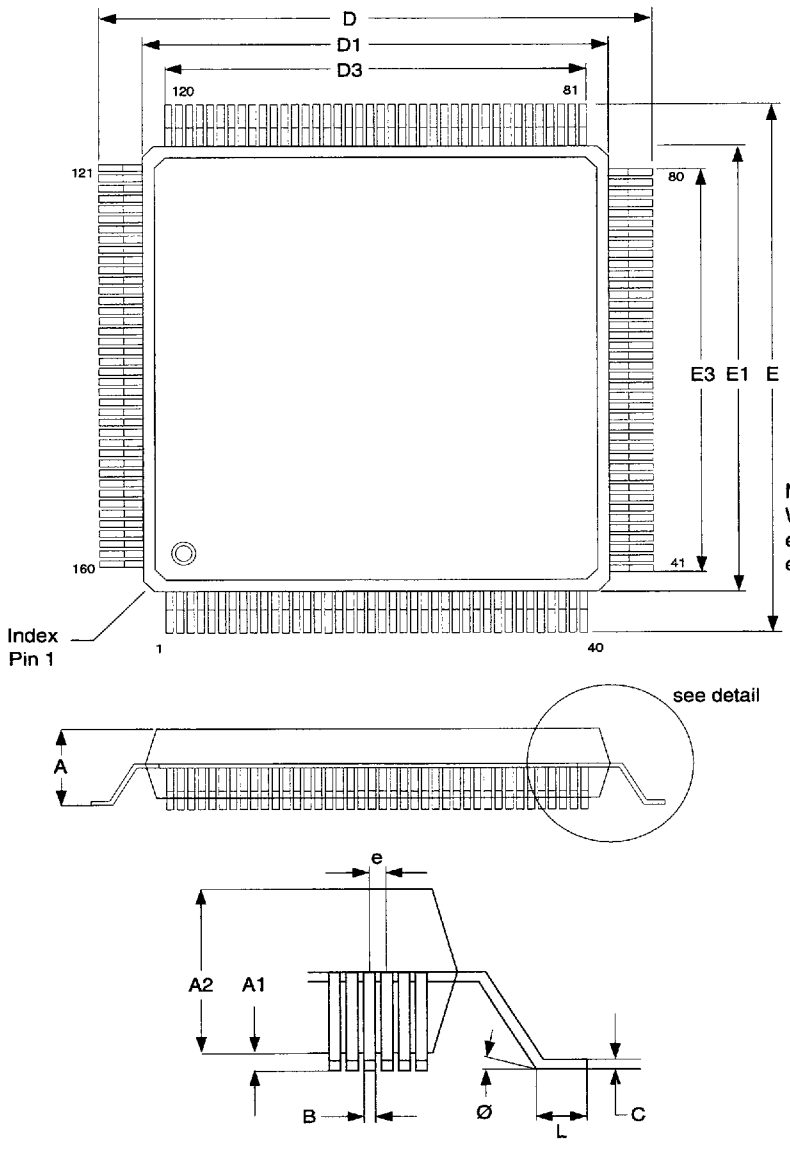

Figure 22. 160 PQFP Mechanical

Note: All dimensions are in inches (millimeters)
Warning: Multiple standard sizes for 160PQFP exist. Check layout carefully when using library elements.

Symbol	Min	Nom	Max
A	-	-	0.175 (4.45)
A1	0.017 (0.44)	0.018 (0.45)	0.019 (0.47)
A2	0.134 (3.4)	0.142 (3.6)	0.150 (3.8)
B	0.008 (0.2)	0.012 (0.3)	0.016 (0.4)
C	0.004 (0.10)	0.006 (0.15)	0.010 (0.25)
D	1.24 (31.6)	1.26 (32.0)	1.28 (32.4)
D1	1.09 (27.8)	1.10 (28.0)	1.11 (28.2)
D3	1.01 (25.6) REF		
e	0.026 (0.65) BASIC		
E	1.24 (31.6)	1.26 (32.0)	1.28 (32.4)
E1	1.09 (27.8)	1.10 (28.0)	1.11 (28.2)
E3	1.01 (25.6) REF		
L	0.02 (0.6)	0.03 (0.8)	0.04 (1.0)
θ	0	3.5	10

Figure 23. PQFP Mechanical