TQFP, QFP
Commercial Temp
Industrial Temp

64K x 32
2M Synchronous Burst SRAM

150Mhz - 66Mhz
9ns - 18ns
3.3V VDD
3.3V & 2.5V I/O

Features

- $\overline{FT}$ pin for user configurable flow through or pipelined operation.
- Single Cycle Deselect (SCD) Operation.
- High Output Drive current.
- 3.3V +10%/-5% Core power supply
- 2.5V or 3.3V I/O supply.
- $\overline{LBO}$ pin for linear or interleaved burst mode.
- Internal input resistors on mode pins allow floating mode pins.
- Default to Interleaved Pipelined Mode.
- Byte write ($\overline{BW}$) and/or global write ($\overline{GW}$) operation.
- Common data inputs and data outputs.
- Clock Control, registered, address, data, and control.
- Internal Self-Timed Write cycle.
- Automatic power-down for portable applications.
- JEDEC standard 100-lead TQFP or QFP package.

		-150	-138	-133	-117	-100	-66
Pipeline	tCycle	6.6ns	7.25ns	7.5ns	8.5ns	10ns	12.5ns
3-1-1-1	t_{KQ}	3.8ns	4ns	4ns	4.5	5ns	6ns
	I_{DD}	270mA	245mA	240mA	210mA	180mA	150mA
Flow	tCycle	10.5ns	15ns	15ns	15ns	15ns	20ns
Through	t_{KQ}	9ns	9.7ns	10ns	11ns	12ns	18ns
2-1-1-1	I_{DD}	170mA	120mA	120mA	120mA	120mA	95mA

Functional Description

Applications

The GS820H32A is a 2,097,152 bit high performance synchronous SRAM with a 2 bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPU's, the device now finds application in synchronous SRAM applications ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/O's, chip enables ($\overline{E}_1$, E_2, $\overline{E}_3$), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$) and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive edge triggered clock input (CK). Output enable ($\overline{G}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{LBO}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through / Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{FT}$ mode pin/bump (Pin 14 in the TQFP, bump 1F in the FP-BGA). Holding the $\overline{FT}$ mode pin/bump low, places the RAM in Flow through mode, causing output data to bypass the Data Output Register. Holding $\overline{FT}$ high places the RAM in Pipelined Mode, activating the rising edge triggered Data Output Register.

Pipelined Reads

The GS820H32A is an SCD (Single Cycle Deselect) pipelined synchronous SRAM. DCD (Dual Cycle Deselect) versions are also available. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers.

Byte Write and Global Write

Byte write operation is performed by using byte write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

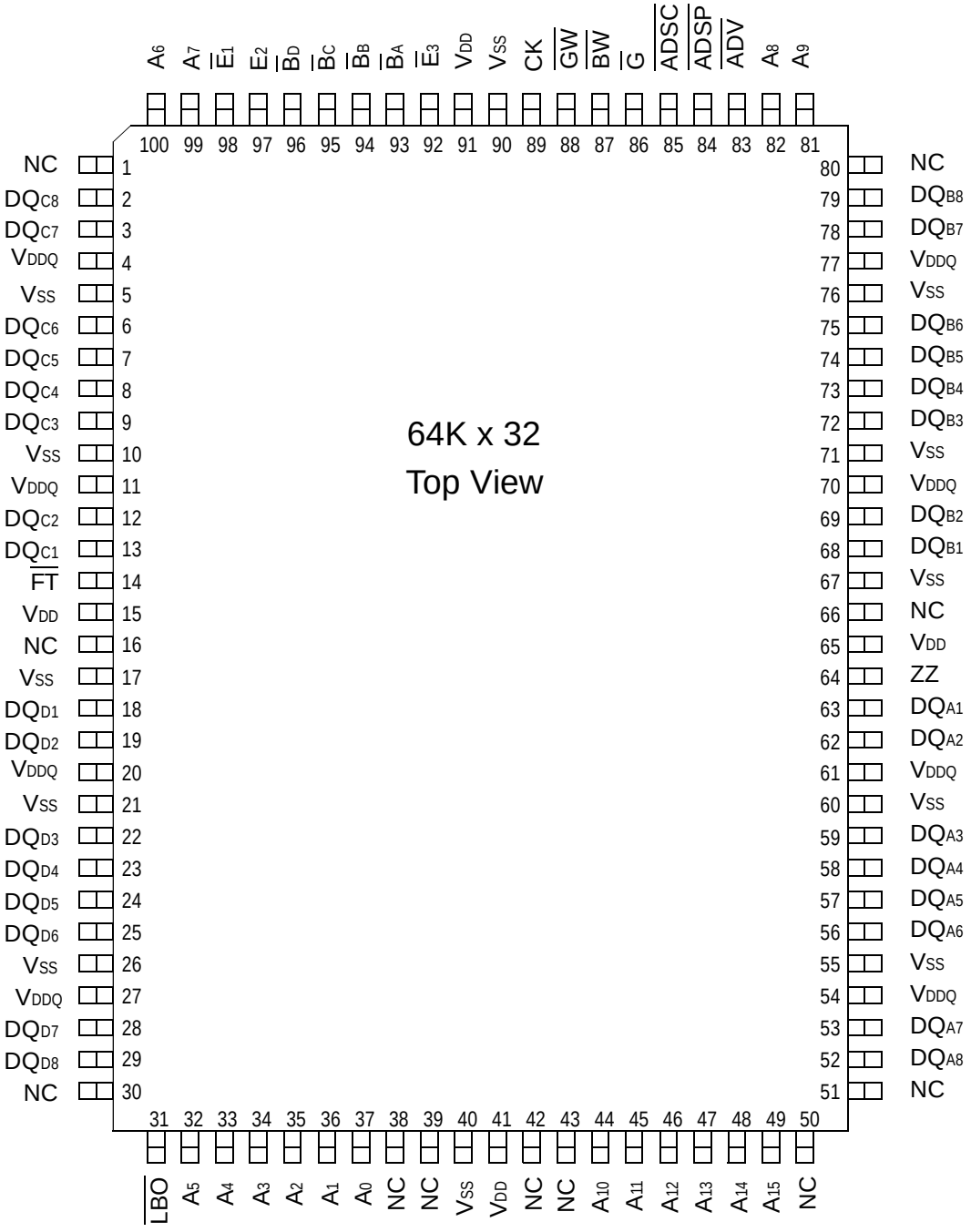
Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

Core and Interface Voltages

The GS820H32A operates on a 3.3V power supply and all inputs/outputs are 3.3V and 2.5V compatible. Separate output power (V_{DDQ}) pins are used to de-couple output noise from the internal circuit.

GS820H32A 100 Pin TQFP and QFP Pinout

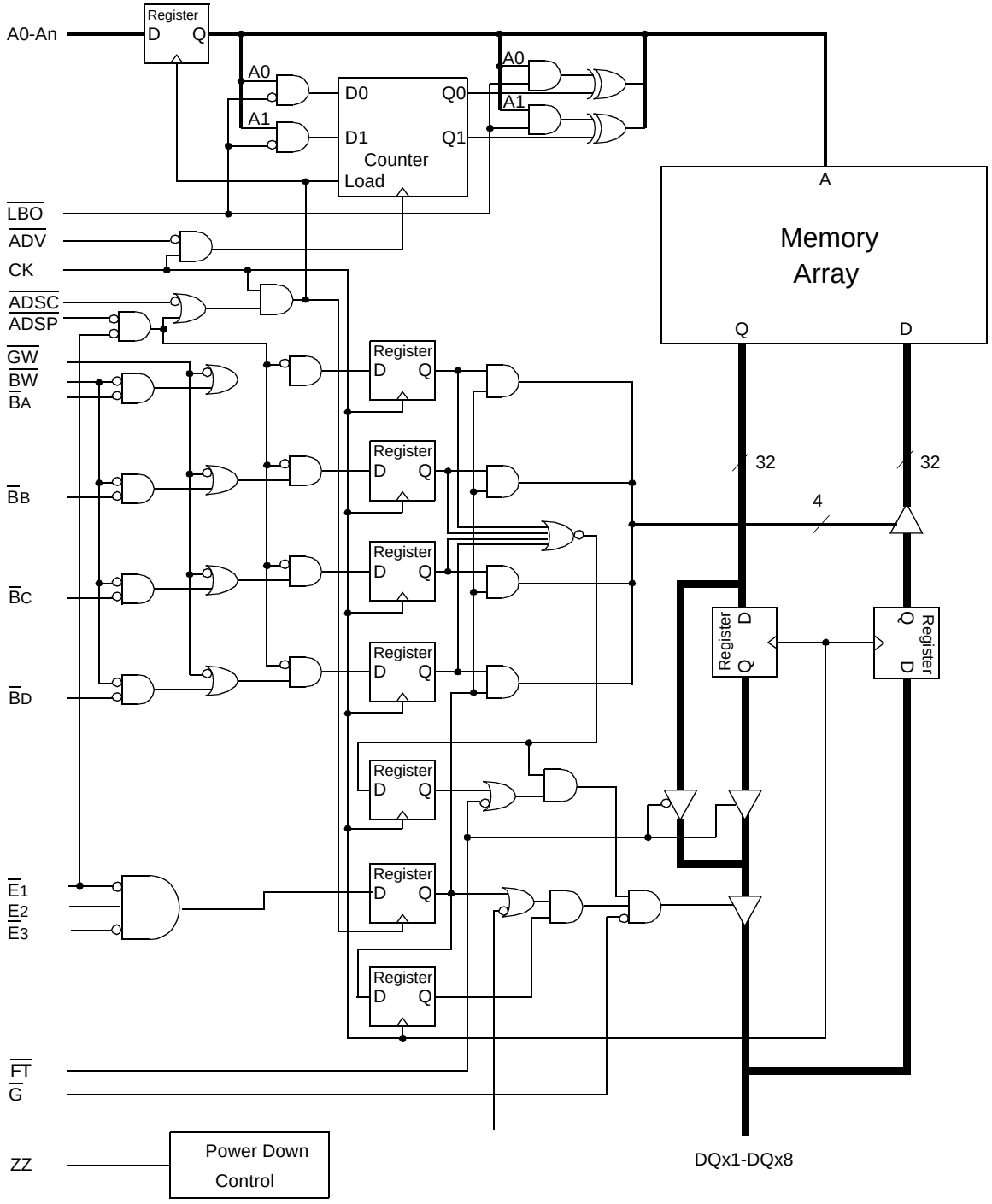


TQFP Pin Description

Pin Location	Symbol	Type	Description
37, 36	A_0, A_1	I	Address field LSB's and Address Counter preset Inputs
35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49	$A_{2\text{-}15}$	I	Address Inputs
52, 53, 56, 57, 58, 59, 62, 63 68, 69, 72, 73, 74, 75, 78, 79 2, 3, 6, 7, 8, 9, 12, 13 18, 19, 22, 23, 24, 25, 28, 29	DQ_{A1}-DQ_{A8} DQ_{B1}-DQ_{B8} DQ_{C1}-DQ_{C8} DQ_{D1}-DQ_{D8}	I/O	Data Input and Output pins.
16, 38, 39, 42, 43, 66, 50, 51, 80, 1, 30	NC		No Connect
87	$\overline{BW}$	I	Byte Write. Writes all enabled bytes. Active Low.
93, 94	$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B Data I/O's. Active Low.
95, 96	$\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_C, DQ_D Data I/O's. Active Low.
89	CK	I	Clock Input Signal. Active High.
88	$\overline{GW}$	I	Global Write Enable. Writes all bytes. Active Low.
98, 92	$\overline{E}_1$, $\overline{E}_3$	I	Chip Enable. Active Low.
97	E_2	I	Chip Enable. Active High.
86	$\overline{G}$	I	Output Enable. Active Low.
83	$\overline{ADV}$	I	Burst address counter advance enable. Active Low.
84, 85	$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller). Active Low.
64	ZZ	I	Sleep Mode control. Active High.
14	$\overline{FT}$	I	Flow Through or Pipeline mode. Active Low.
31	$\overline{LBO}$	I	Linear Burst Order mode. Active Low.
15, 41, 65, 91	V_{DD}	I	Core power supply.
5,10,17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	I	I/O and Core Ground.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	I	Output driver power supply.

H

GS820H32A Block Diagram



Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H or NC	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There are pull up devices on $\overline{LBO}$ and $\overline{FT}$ pins and a pull down device on and ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte A	H	L	L	H	H	H	2, 3
Write byte B	H	L	H	L	H	H	2, 3
Write byte C	H	L	H	H	L	H	2, 3, 4
Write byte D	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Note:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ and/or $\overline{B}_D$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/O's remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.

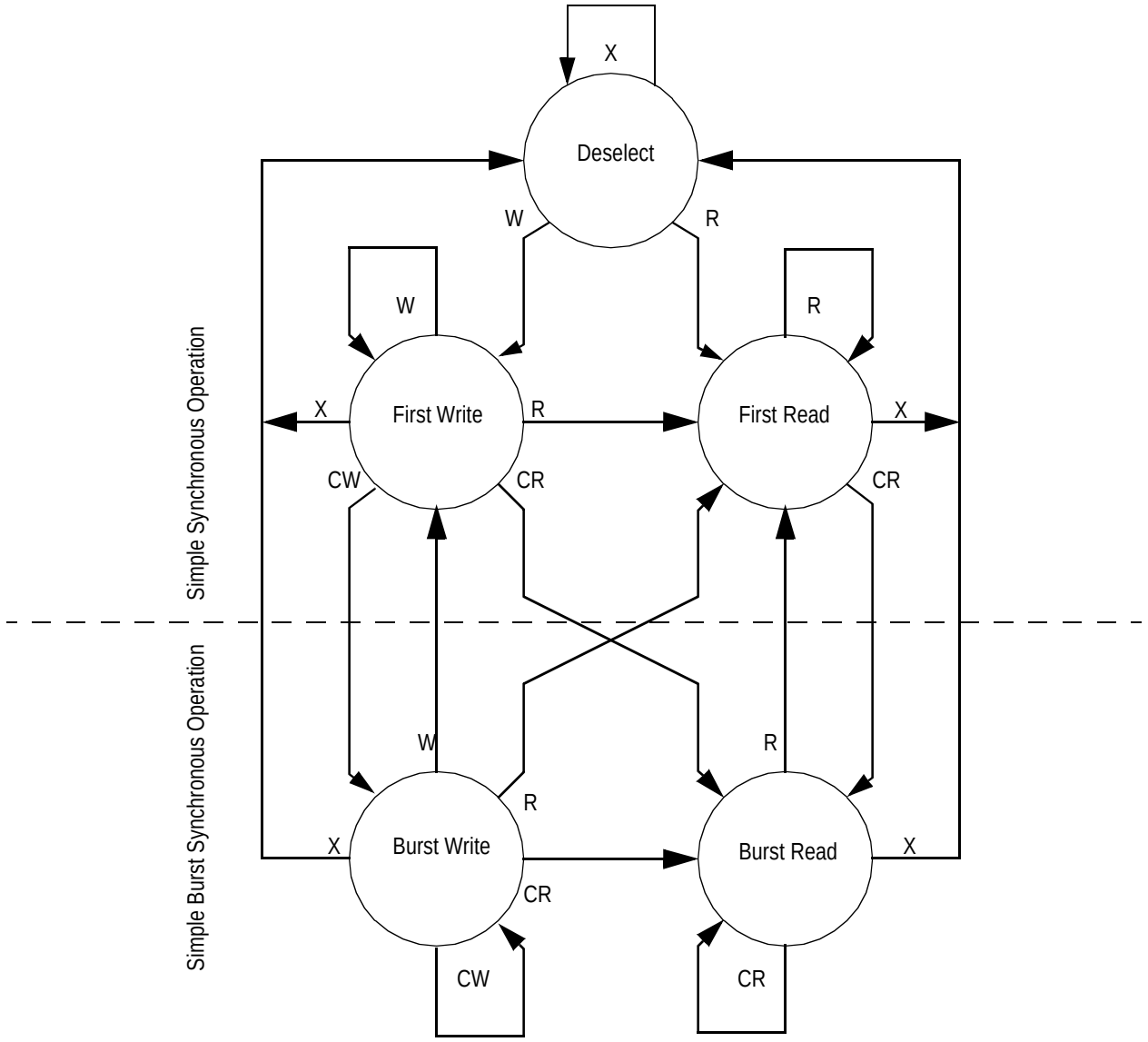
Synchronous Truth Table

Operation	Address Used	State Diagram Key[5]	$\overline{E}_1$	E^2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	W^3	DQ^4
Deselect Cycle, Power Down	**None**	**X**	**H**	**X**	**X**	**L**	**X**	**X**	**High-Z**
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	**None**	**X**	**L**	**F**	**H**	**L**	**X**	**X**	**High-Z**
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
Read Cycle, Begin Burst	**External**	**R**	**L**	**T**	**H**	**L**	**X**	**F**	**Q**
Write Cycle, Begin Burst	**External**	**W**	**L**	**T**	**H**	**L**	**X**	**T**	**D**
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

Note:

1. X = Don't Care, H = High, L = Low.
2. E = T (True) if E_2 = 1 and $\overline{E}_3$ = 0; E = F (False) if E_2 = 0 or $\overline{E}_3$ = 1.
3. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

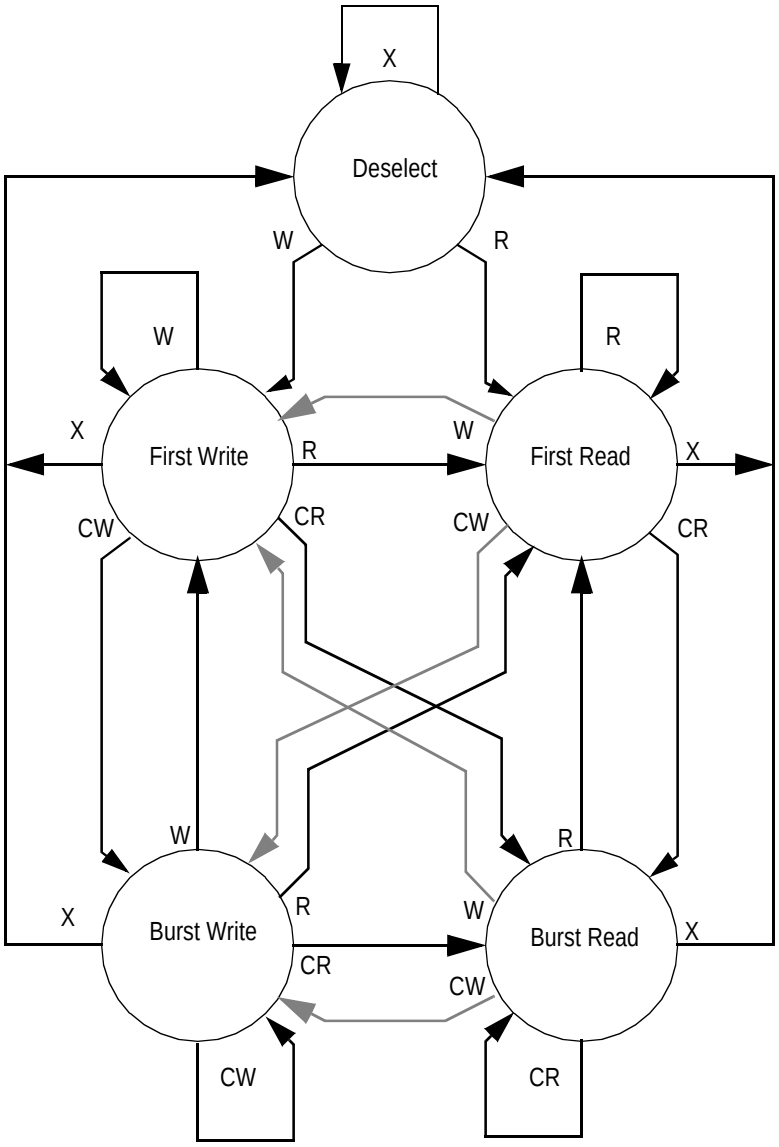
Simplified State Diagram



Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied Low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E}_1$, E_2, $\overline{E}_3$) and Write ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$, $\overline{BW}$ and $\overline{GW}$) control inputs and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write and $\overline{ADSC}$ control inputs and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

Simplified State Diagram with $\overline{G}$



Notes:
1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal Read cycles.
3. Transitions shown in grey tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	-0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	-0.5 to V_{DD}	V
V_{CK}	Voltage on Clock Input Pin	-0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to V_{DDQ}+0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	-0.5 to V_{DD}+0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/- 20	mA
I_{OUT}	Output Current on Any I/O Pin	+/- 20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	-55 to 125	°C
T_{BIAS}	Temperature Under Bias	-55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

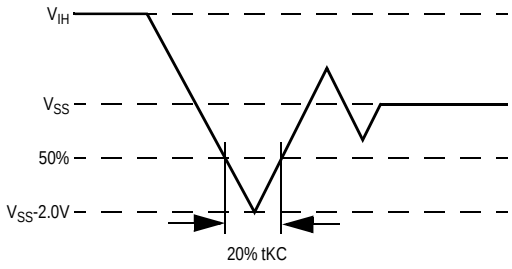
Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.6	V	
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V	1
Input High Voltage	V_{IH}	1.7	---	V_{DD}+0.3	V	2
Input Low Voltage	V_{IL}	-0.3	---	0.8	V	2
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	3
Ambient Temperature (Industrial Range Versions)	T_A	-40	25	85	°C	3

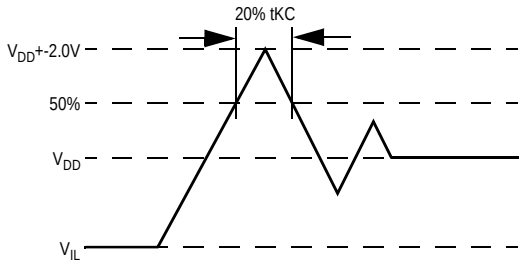
Note:

1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 2.75V ≤ VDDQ ≤ 2.375V (i.e. 2.5V I/O) and 3.6V ≤ VDDQ ≤ 3.135V (i.e. 3.3V I/O) and quoted at whichever condition is worst case.
2. This device features input buffers compatible with both 3.3V and 2.5V I/O drivers.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
4. Input Under/overshoot voltage must be -2V > Vi < V_{DD}+2V with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A=25°C, f=1MHz, V_{DD}=3.3V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Control Input Capacitance	C_I	V_{DD}=3.3V	3	4	pF
Input Capacitance	C_{IN}	V_{IN}=0V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	6	7	pF

Note: This parameter is sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	TQFP Max	QFP Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	TBD	°C/W	1,2,4
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	TBD	°C/W	1,2,4
Junction to Case (TOP)		$R_{\Theta JC}$	9	TBD	°C/W	3,4

Notes:

1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87.
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1.
4. For x18 configuration, consult factory.

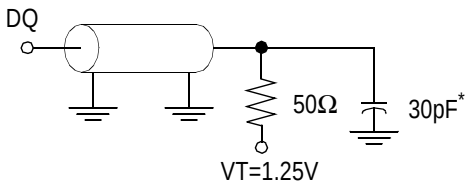
AC Test Conditions

Parameter	Conditions
Input high level	2.3V
Input low level	0.2V
Input slew rate	1V/ns
Input reference level	1.25V
Output reference level	1.25V
Output load	Fig. 1& 2

Notes:

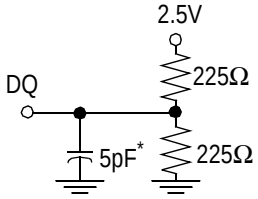
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Output Load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.
4. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

Output Load 2



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	-1uA	1uA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0V \leq V_{IN} \leq V_{IH}$	-1uA -1uA	1uA 300uA
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0V \leq V_{IN} \leq V_{IL}$	-300uA -1uA	1uA 1uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	-1uA	1uA
Output High Voltage	V_{OH}	I_{OH} = - 8mA, V_{DDQ}=2.375V	1.7V	
Output High Voltage	V_{OH}	I_{OH} = -8mA, V_{DDQ}=3.135V	2.4V	
Output Low Voltage	V_{OL}	I_{OL} = 8mA		0.4V

Operating Currents

Parameter	Test Conditions	Symbol	-150		-138		-133	
			0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C
Operating Current	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	I_{DD} Pipeline	270mA	275mA	245mA	250mA	240mA	245mA
		I_{DD} Flow-Thru	170mA	175mA	120mA	125mA	120mA	125mA
Standby Current	ZZ ≥ V_{DD} - 0.2V	I_{SB} Flow-Thru	10mA	15mA	10mA	15mA	10mA	15mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	I_{DD} Pipeline	90mA	95mA	80mA	85mA	80mA	85mA
		I_{DD} Flow-Thru	45mA	50mA	40mA	45mA	40mA	45mA

Operating Currents

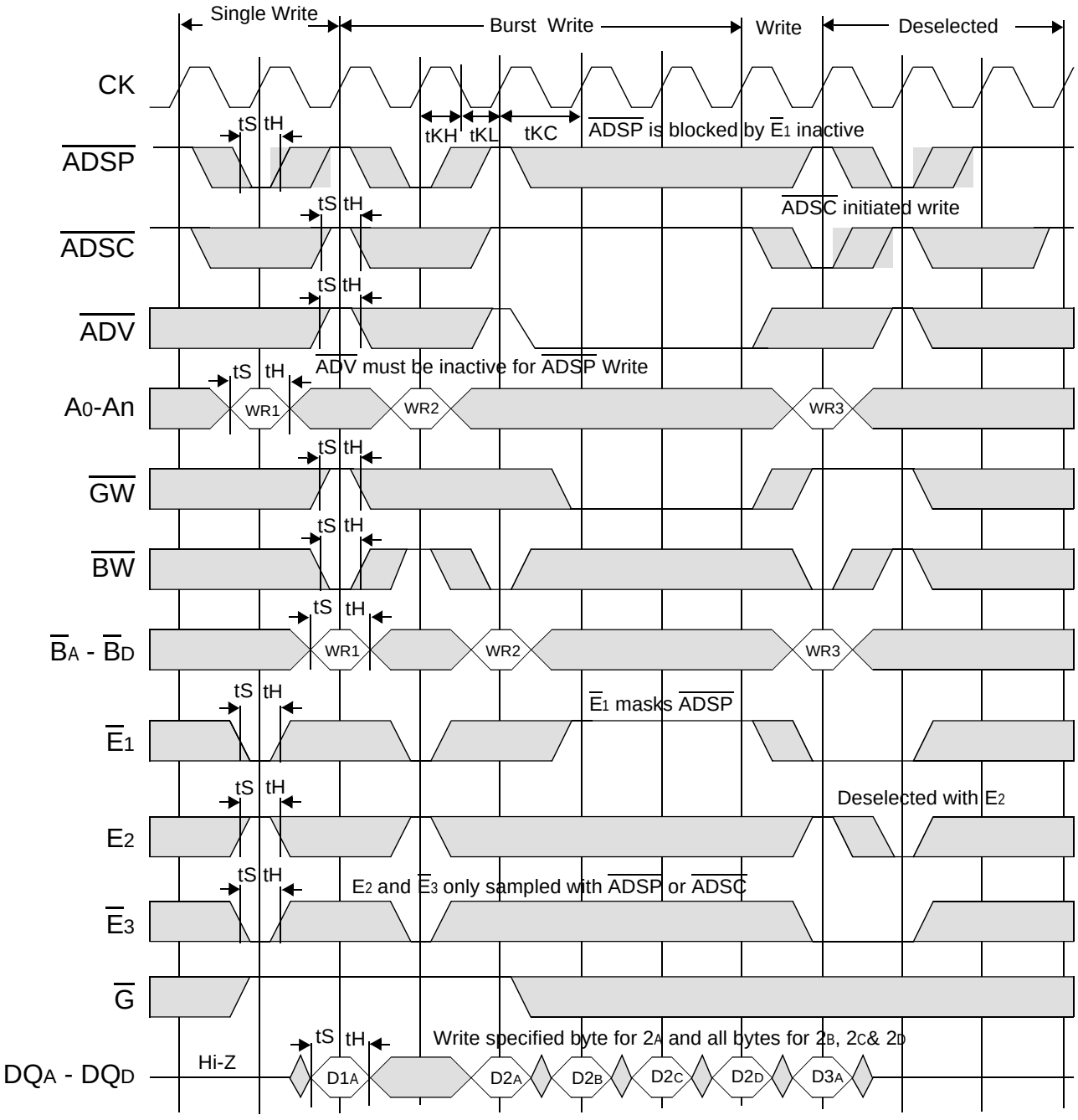
Parameter	Test Conditions	Symbol	-117		-100		-66	
			0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C
Operating Current	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	I_{DD} Pipeline	210mA	215mA	180mA	185mA	150mA	155mA
		I_{DD} Flow-Thru	120mA	125mA	120mA	125mA	95mA	100mA
Standby Current	ZZ ≥ V_{DD} - 0.2V	I_{SB} Flow-Thru	10mA	15mA	10mA	15mA	10mA	15mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	I_{DD} Pipeline	70mA	75mA	60mA	65mA	50mA	55mA
		I_{DD} Flow-Thru	40mA	45mA	40mA	45mA	40mA	45mA

AC Electrical Characteristics

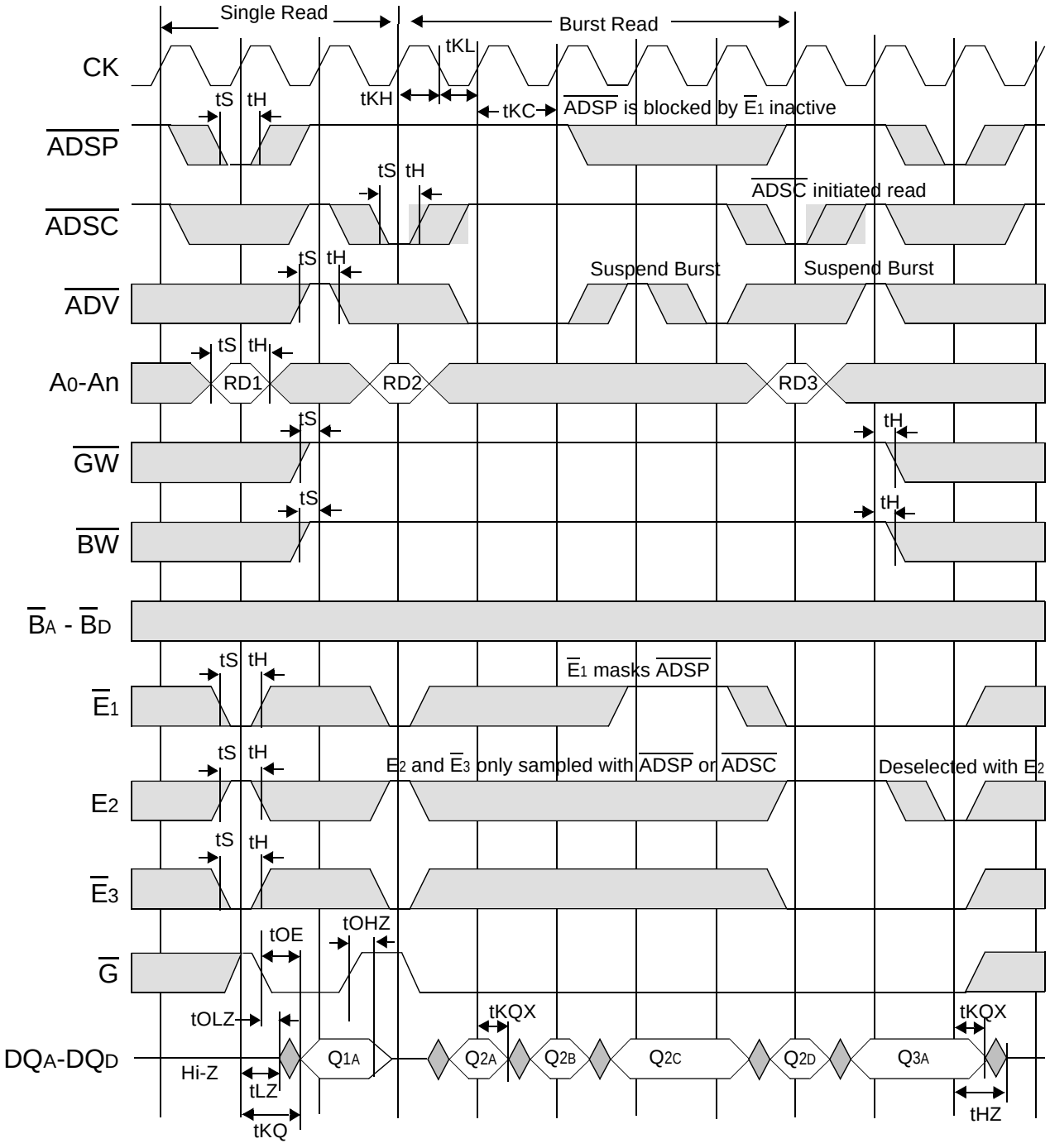
	Parameter	Symbol	-150		-138		-133		-117		-100		-66		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	6.6	---	7.25	---	7.5	---	8.5	---	10		12.5		ns
	Clock to Output Valid	tKQ	---	3.8	---	4	---	4	---	4.5		5		6	ns
	Clock to Output Invalid	tKQX	1.5	---	2	---	2	---	2	---	2		2		ns
	Clock to Output in Low-Z	tLZ[1]	1.5	---	2	---	2	---	2	---	2		2		ns
Flow-Thru	Clock Cycle Time	tKC	10.5	---	15	---	15	---	15	---	15		20		ns
	Clock to Output Valid	tKQ	---	9.0	---	9.7	---	10	---	11		12		18	ns
	Clock to Output Invalid	tKQX	3	---	3	---	3	---	3	---	3		3		ns
	Clock to Output in Low-Z	tLZ[1]	3	---	3	---	3	---	3	---	3		3		ns
	Clock HIGH Time	tKH	1.8	---	1.9	---	1.9	---	2	---	3		4		ns
	Clock LOW Time	tKL	1.8	---	1.9	---	1.9	---	2	---	3		4		ns
	Clock to Output in High-Z	tHZ[1]	1.5	3.8	1.5	4	1.5	4	1.5	4		5		6	ns
	$\overline{G}$ to Output Valid	tOE	---	3.8	---	4	---	4	---	4		5		6	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	---	0	---	0	---	0	---	0		0		ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	---	4	---	4	---	4	---	4		5		6	ns
	Setup time	tS	1.7	---	2	---	2	---	2	---	2		2		ns
	Hold time	tH	0.5	---	0.5	---	0.5	---	0.5	---	0.5		0.5		ns
	ZZ setup time	tZZS[2]	5	---	5	---	5	---	5	---	5		5		ns
	ZZ hold time	tZZH[2]	1	---	1	---	1	---	1	---	1		1		ns
	ZZ recovery	tZZR	20	---	20	---	20	---	20	---	20		20		ns

Notes:
1. These parameters are sampled and are not 100% tested
2. ZZ is an asynchronous signal. However, In order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

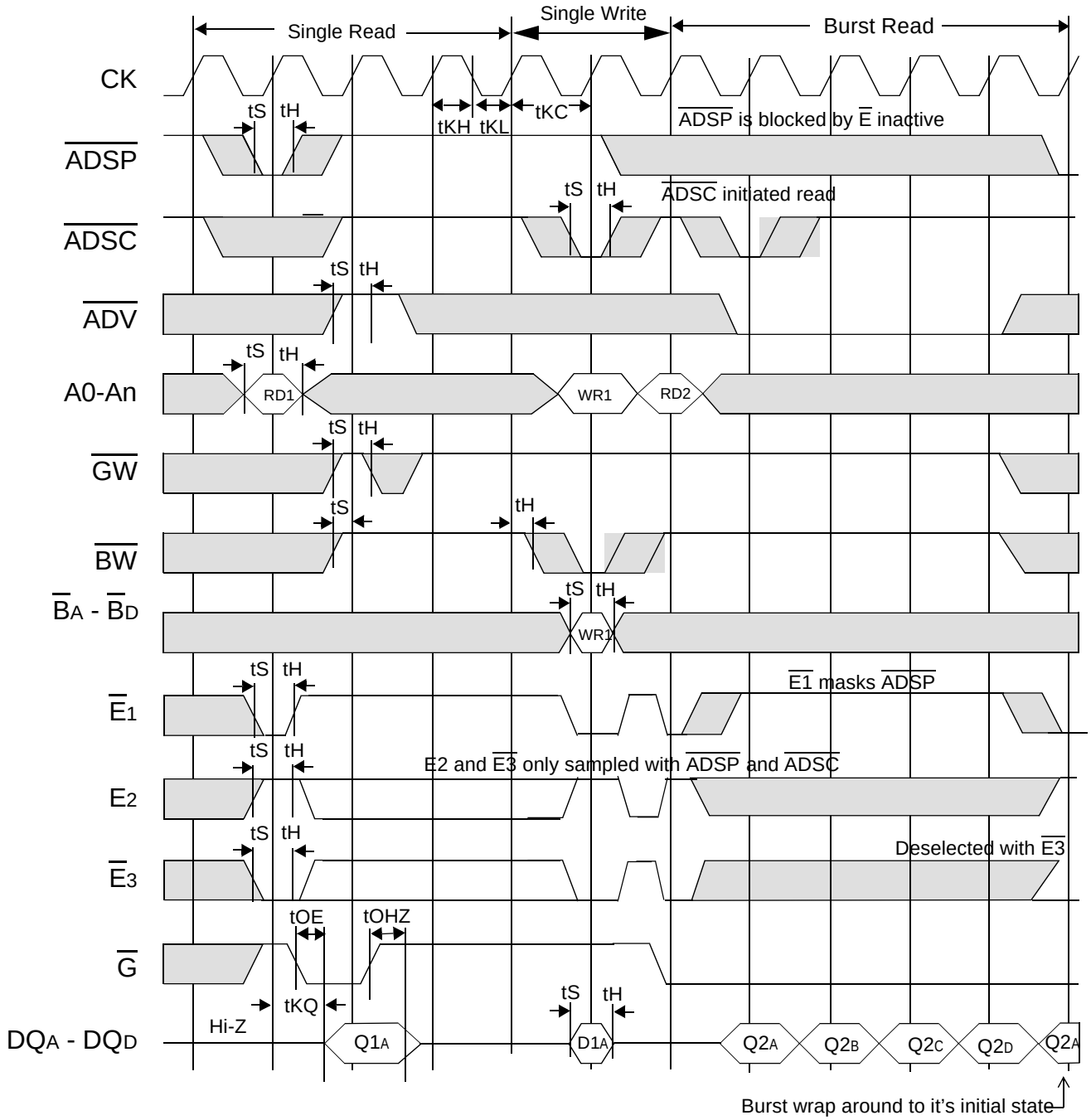
Write Cycle Timing



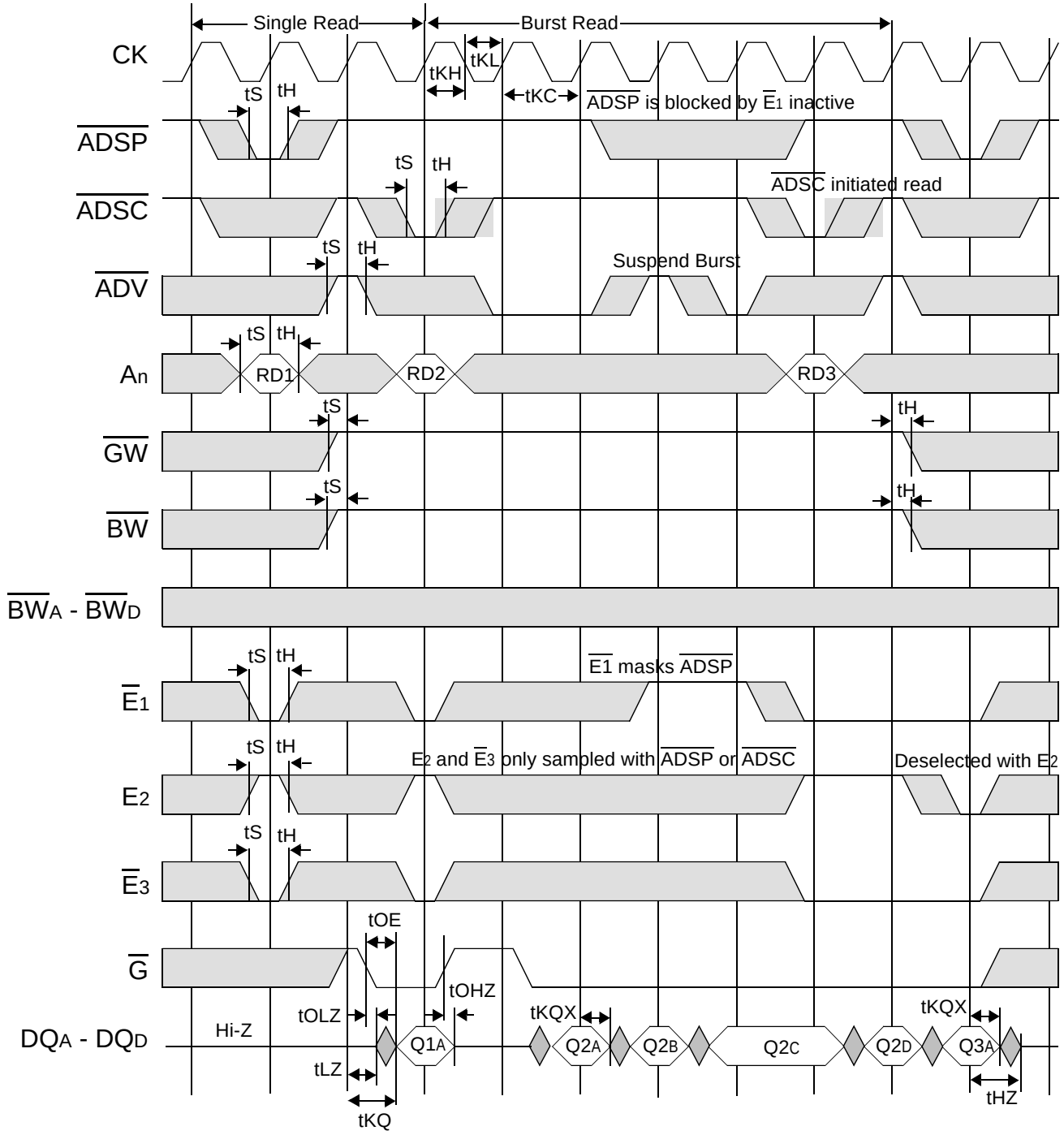
Flow Through Read Cycle Timing



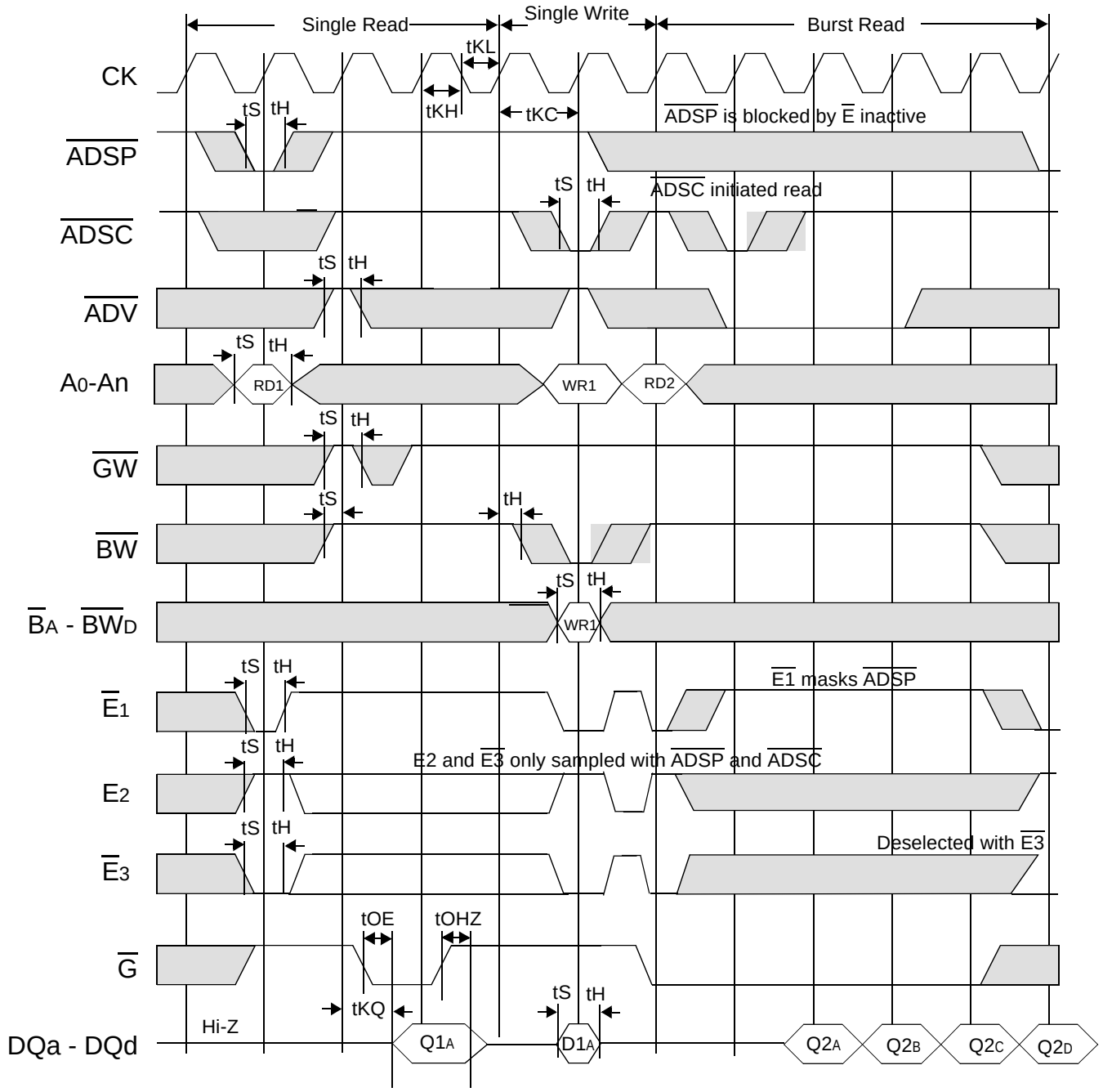
Flow Through Read-Write Cycle Timing



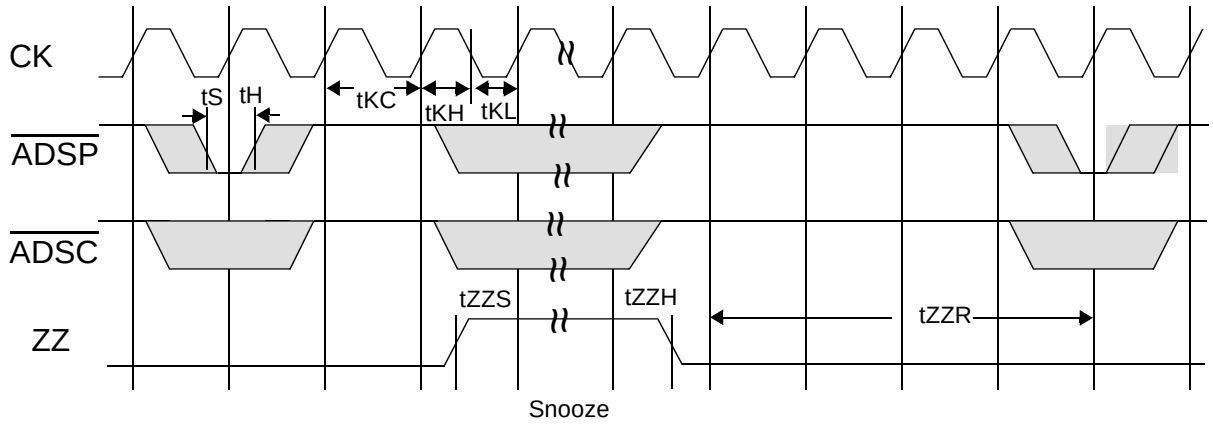
Pipelined SCD Read Cycle Timing



Pipelined SCD Read - Write Cycle Timing



Sleep Mode Timing Diagram

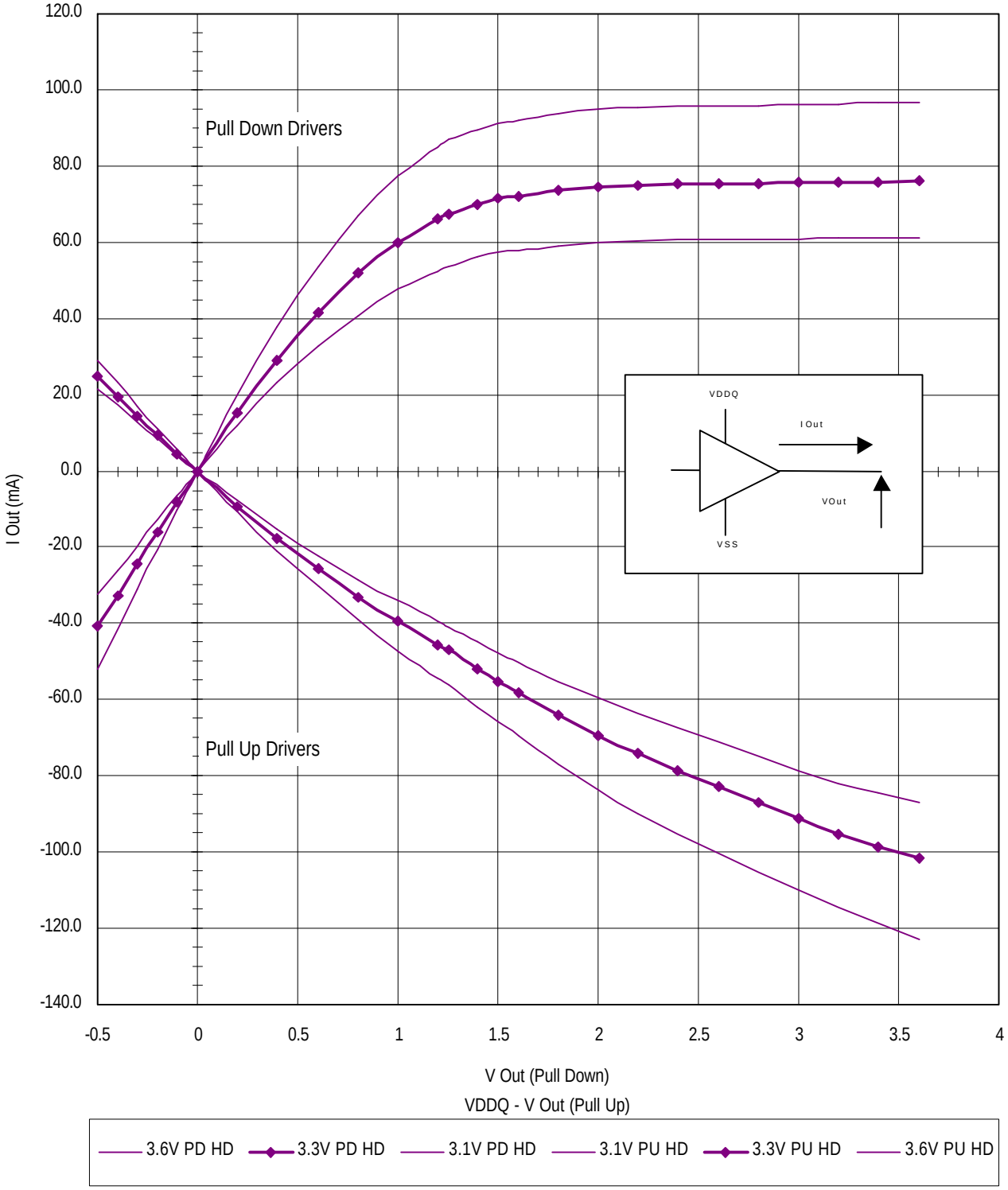


Application Tips

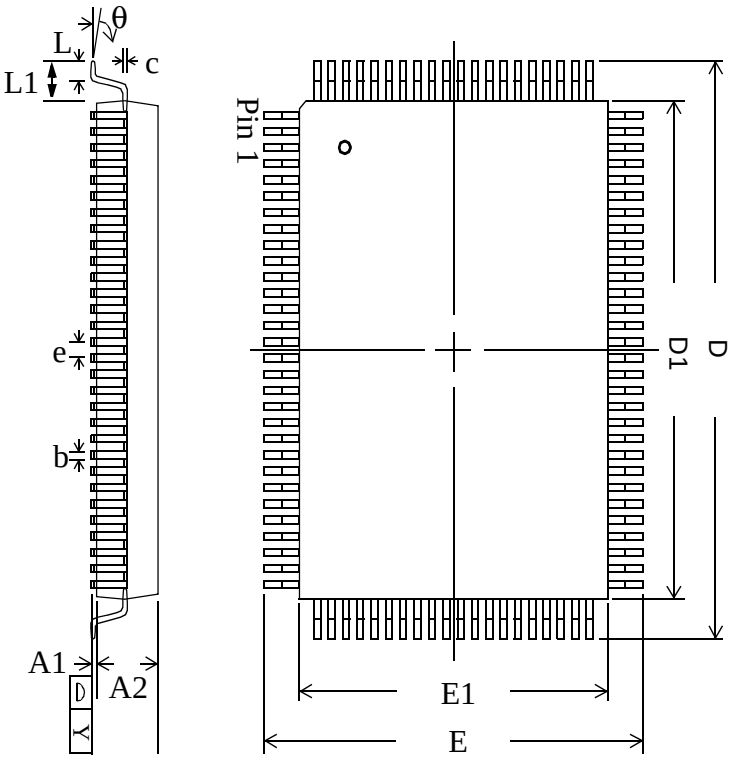
Single and Dual Cycle Deselect

SCD devices force the use of “dummy read cycles” (read cycles that are launched normally but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings) but greater care must be exercised to avoid excessive bus contention.

GS 820H32A Output Driver Characteristics



TQFP and QFP Package Drawing



		TQFP			QFP		
Symbol	Description	Min.	Nom.	Max	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15	0.25	0.35	0.45
A2	Body Thickness	1.35	1.40	1.45	2.55	2.72	2.90
b	Lead Width	0.20	0.30	0.40	0.20	0.30	0.40
c	Lead Thickness	0.09		0.20	0.10	0.15	0.20
D	Terminal Dimension	21.9	22.0	22.1	22.95	23.2	23.45
D1	Package Body	19.9	20.0	20.1	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1	17.0	17.2	17.4
E1	Package Body	13.9	14.0	14.1	13.9	14.0	14.1
e	Lead Pitch		0.65			0.65	
L	Foot Length	0.45	0.60	0.75	.60	0.80	1.00
L1	Lead Length		1.00			1.60	
Y	Coplanarity			0.10			0.10
θ	Lead Angle	0°		7°	0°		7°

Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion

Org	Part Number[1]	Type	Package	Speed[2] (Mhz/ ns)	T_A [3]	Status
64K x 32	GS820H32AT-150	Pipeline/Flow Through	TQFP	150/9	C	
64K x 32	GS820H32A2T-138	Pipeline/Flow Through	TQFP	138/9.7	C	
64K x 32	GS820H32AT-133	Pipeline/Flow Through	TQFP	133/10	C	
64K x 32	GS820H32AT-4	Pipeline/Flow Through	TQFP	117/11	C	
64K x 32	GS820H32AT-5	Pipeline/Flow Through	TQFP	100/12	C	
64K x 32	GS820H32AT-6	Pipeline/Flow Through	TQFP	66/18	C	
64K x 32	GS820H32AT-150I	Pipeline/Flow Through	TQFP	150/9	I	Not Available
64K x 32	GS820H32AT-138I	Pipeline/Flow Through	TQFP	138/9.7	I	
64K x 32	GS820H32AT-133I	Pipeline/Flow Through	TQFP	133/10	I	
64K x 32	GS820H32AT-4I	Pipeline/Flow Through	TQFP	117/11	I	
64K x 32	GS820H32AT-5I	Pipeline/Flow Through	TQFP	100/12	I	
64K x 32	GS820H32AT-6I	Pipeline/Flow Through	TQFP	66/18	I	
64K x 32	GS820H32AQ-150	Pipeline/Flow Through	QFP	150/9	C	
64K x 32	GS820H32AQ-138	Pipeline/Flow Through	QFP	138/9.7	C	
64K x 32	GS820H32AQ-133	Pipeline/Flow Through	QFP	133/10	C	
64K x 32	GS820H32AQ-4	Pipeline/Flow Through	QFP	117/11	C	
64K x 32	GS820H32AQ-5	Pipeline/Flow Through	QFP	100/12	C	
64K x 32	GS820H32AQ-6	Pipeline/Flow Through	QFP	66/18	C	
64K x 32	GS820H32AQ-150I	Pipeline/Flow Through	QFP	150/9	I	Not Available
64K x 32	GS820H32AQ-138I	Pipeline/Flow Through	QFP	138/9.7	I	
64K x 32	GS820H32AQ-133I	Pipeline/Flow Through	QFP	133/10	I	
64K x 32	GS820H32AQ-4I	Pipeline/Flow Through	QFP	117/11	I	
64K x 32	GS820H32AQ-5I	Pipeline/Flow Through	QFP	100/12	I	
64K x 32	GS820H32AQ-6I	Pipeline/Flow Through	QFP	66/18	I	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS820H32AT-100IT.
2. The speed column indicates the cycle frequency (Mhz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline / Flow through mode selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site for a complete listing of current offerings.

Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Revisions
GS82032 Rev 1.03 2/ 2000D;GS820321.04 3/2000E	Content	• First Release of A version. Added “A” Version to 82032T/Q, 820E32TQ, and 820H32TQ

