National Semiconductor

# MICROCIRCUIT DATA SHEET

## MNCLC414A-X REV 1A0

Original Creation Date: 06/24/98
Last Update Date: 04/20/01
Last Major Revision Date: 06/07/99

# QUAD, LOW-POWER MONOLITHIC OP AMP

## General Description

The CLC414 is a low-power, quad, monolithic operational amplifier designed for intermediate-gain applications where power and cost per channel are of primary concern. Benefiting from Comlinear's current feedback architecture, the CLC414 offers a gain range of ±1 to ±10 while providing stable, oscillation-free operation without external compensation, even at unity gain.

Operating from ±5V supplies, the CLC414 consumes only 25mV of power per channel, yet maintains a 90MHz small-signal bandwidth and a 1000V/uS slew rate. The CLC414 also provides wide channel isolation with its 70dB crosstalk (input referred at 5MHz). Applications requiring a high-density solution to high-speed amplification such as active filters and instumenation differential amplifiers will benefit from the CLC414's four integrated, wideband operational amplifiers in one 14-pin package.

Commercial remote-sensing applications and battery-powered radio transceivers requiring high-performance, low-power amplifiers will find the CLC414 to be an attractive, cost-effective solution. In composite video switching and distribution applications, the CLC414 offers differential gain and phase performance of 0.1%, 0.12 degrees at 3.58MHz.

The lower power CLC414 and the wideband CLC415 are quad versions of the CLC406. Both of these quads afford the designer lower power consumption and lower cost per channel with the additional benefit of requiring less board space per amplifier.

## Industry Part Number

CLC414A

## NS Part Numbers

CLC414AE-QML**
CLC414AJ-QML*

## Prime Die

UB1563A

## Controlling Document

5962-9169301MCA*, M2A**

## Processing

MIL-STD-883, Method 5004

## Quality Conformance Inspection

MIL-STD-883, Method 5005

| Subgrp | Description | Temp (°C) |
|---|---|---|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |

## Features

- 90MHz small signal bandwidth
- 2mA quiescent current per amplifier
- 70dB channel isolation @ 5MHz
- 0.1%/0.12 degrees differential gain/phase
- 16ns settling to 0.1%
- 100V/uS slew rate
- 3.3ns rise and fall time (2 Vpp)
- 70mA output current

## Applications

- Composite video distribution amplifiers
- HDTV amplifiers
- RGB-video amplifiers
- CCD signal processing
- Active filters
- Instumentation diff. amplifiers
- General purpose high density requirements

# (Absolute Maximum Ratings)
(Note 1)

| | | |
|---|---|---|
| Supply Voltage (Vs) | | ±7V dc |
| Output Current (Iout) | | 70mA |
| Common Mode Input Voltage (Vcm) | | ±Vs |
| Differential Input Voltage (Vid) | | ±10V |
| Power Dissipation (Pd) (Note 2) | | 1.2W |
| Lead Temperature (soldering, 10 seconds) | | +300 C |
| Junction Temperature (Tj) | | +175 C |
| Storage Temperature Range | | -65 C to +150 C |
| Thermal Resistance | | |
| Junction-to-ambient (ThetaJA) | | |
| Ceramic DIP | (Still Air) | 94 C/W |
| | (500 LFPM) | 57 C/W |
| LCC | (Still Air) | TBD |
| | (500 LFPM) | TBD |
| Junction-to case (ThetaJC) | | |
| Ceramic DIP | | 17 C/W |
| LCC | | TBD |
| Package Weight (typical) | | |
| Ceramic DIP | | 2190mg |
| LCC | | TBD |
| ESD Tolerance (Note 3) | | 500V |

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific perfomance limits. For guaranteed specifications and test conditions see the Electrical Characterisitics. The guaranteed specifications apply only for the test conditions listed. Some performance charateristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) /ThetaJA or the number given in the absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5k Ohms.

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage (Vs) | ±5V dc |
| Gain Range (Av) | ±1 to ±10 |
| Ambient Operating Temperature Range (Ta) | -55 C to +125 C |

# Electrical Characteristics

## AC/DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +6, load resistance (Rl) = 100 Ohms, feedback resistance (Rf) = 500 Ohms, and gain resistance (Rg) = 100 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| +Iin | Input Bias Current (noninverting) | | | | -5 | +5 | uA | 1, 2 |
| | | | | | -10 | +10 | uA | 3 |
| -Iin | Input Bias Current (inverting) | | | | -6 | +6 | uA | 1 |
| | | | | | -10 | +10 | uA | 2 |
| | | | | | -20 | +20 | uA | 3 |
| Vio | Input Offset Voltage | Rs = 50 Ohms | | | -6.0 | +6.0 | mV | 1 |
| | | | | | -14.0 | +14.0 | mV | 2 |
| | | | | | -10.5 | +10.5 | mV | 3 |
| Tc (+Iin) | Average +Input Bias Current Drift | | 1 | | -30 | +30 | nA/C | 2 |
| | | | 1 | | -75 | +75 | nA/C | 3 |
| Tc (-Iin) | Average -Input Bias Current Drift | | 1 | | -75 | +75 | nA/C | 2 |
| | | | 1 | | -175 | +175 | nA/C | 3 |
| Tc (Vio) | Average Input Offset Voltage Drift | | 1 | | -80 | +80 | uV/C | 2, 3 |
| Is | Supply Current (all channels) | No Load | | | | +11.5 | mA | 1, 2, 3 |
| +Rin | Input Resistance (noninverting) | | 1 | | 1000 | | KOhms | 1, 2 |
| | | | 1 | | 500 | | KOhms | 3 |
| Iout | Output Current | | 1 | | 50 | | mA | 1, 2 |
| | | | 1 | | 30 | | mA | 3 |
| PSRR | Power Supply Rejection Ratio | +Vs = +4.5V to +5.0V, -Vs = -4.5V to -5.0V | 2 | | 46 | | dB | 1, 3 |
| | | | 2 | | 44 | | dB | 2 |
| CMRR | Common Mode Rejection Ratio | Vcm = ±1V | 1 | | 45 | | dB | 4, 6 |
| | | | 1 | | 43 | | dB | 5 |
| SSBW | Small Signal Bandwidth | -3dB bandwidth, Vout < 2.0 Vpp | | | 60 | | MHz | 4 |
| | | | 2 | | 41 | | MHz | 5 |
| | | | 2 | | 60 | | MHz | 6 |
| LSBW | Large Signal Bandwidth | -3dB bandwidth, Vout < 5.0 Vpp | 1 | | 40 | | MHz | 4 |
| | | | 1 | | 35 | | MHz | 5, 6 |

# Electrical Characteristics

## AC/DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +6, load resistance (Rl) = 100 Ohms, feedback resistance (Rf) = 500 Ohms, and gain resistance (Rg) = 100 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| GFPL | Gain Flatness Peaking Low | At 0.1MHz to 15MHz, Vout < 2.0 Vpp | | | | 0.15 | dB | 4 |
| | | | | | | 0.15 | dB | 5, 6 |
| GFPH | Gain Flatness Peaking High | At > 15MHz, Vout < 2.0 Vpp | | | | 0.3 | dB | 4, 6 |
| | | | | | | 0.3 | dB | 5, 6 |
| GFR | Gain Flatness Rolloff | At 0.1MHz to 30MHz, Vout < 2.0 Vpp | | | | 1.0 | dB | 4 |
| | | | 2 | | | 1.6 | dB | 5 |
| | | | 2 | | | 1.0 | dB | 6 |
| HD2 | Second Harmonic Distortion | 2 Vpp at 5MHz | | | | -41 | dBc | 4 |
| | | | | | | -37 | dBc | 5 |
| | | | | | | -41 | dBc | 6 |
| HD3 | Third Harmonic Distortion | 2 Vpp at 5MHz | | | | -47 | dBc | 4 |
| | | | | | | -45 | dBc | 5 |
| | | | | | | -47 | dBc | 6 |
| SNF | Total Noise Floor | At > 1MHz | 1 | | | -153 | dBm 1Hz | 4, 6 |
| | | | 1 | | | -152 | dBm 1Hz | 5 |
| INV | Total Integrated Noise | At 1MHz to 75MHz | 1 | | | 44 | uV | 1, 3 |
| | | | 1 | | | 48 | uV | 2 |
| VN | Input Noise Non-inverting Voltage | At > 1MHz | 1 | | | 5.0 | nV/Sq RtHz | 1, 3 |
| | | | 1 | | | 5.5 | nV/Sq RtHz | 2 |
| ICN | Input Noise Inverting Current | At > 1MHz | 1 | | | 11.8 | pA/Sq RtHz | 1, 3 |
| | | | 1 | | | 13 | pA/Sq RtHz | 2 |
| INN | Input Noise Non-inverting Current | At > 1MHz | 1 | | | 1.6 | pA/Sq RtHz | 1, 3 |
| | | | 1 | | | 1.8 | pA/Sq RtHz | 2 |
| LPD | Linear Phase Deviation | At 0.1MHz to 30MHz | 1 | | | 1.2 | Degrees | 4, 6 |
| | | | 1 | | | 1.5 | Degrees | 5 |

# Electrical Characteristics

## AC/DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +6, load resistance (Rl) = 100 Ohms, feedback resistance (Rf) = 500 Ohms, and gain resistance (Rg) = 100 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| DG1 | Differential Gain | At 3.58MHz, Rl = 150Ohms, Av = +2 | 1 | | | 0.20 | % | 4 |
| | | | 1 | | | 0.25 | % | 5 |
| | | | 1 | | | 0.15 | % | 6 |
| DG2 | Differential Gain | At 4.43MHz, Rl = 150Ohms, Av = +2 | 1 | | | 0.25 | % | 4 |
| | | | 1 | | | 0.30 | % | 5 |
| | | | 1 | | | 0.20 | % | 6 |
| DP1 | Differential Phase | At 3.58MHz, Rl = 150Ohms, Av = +2 | 1 | | | 0.20 | Degrees | 4 |
| | | | 1 | | | 0.50 | Degrees | 5 |
| | | | 1 | | | 0.15 | Degrees | 6 |
| DP2 | Differential Phase | At 4.43MHz, Rl = 150Ohms, Av = +2 | 1 | | | 0.25 | Degrees | 4 |
| | | | 1 | | | 0.60 | Degrees | 5 |
| | | | 1 | | | 0.20 | Degrees | 6 |
| XT | Crosstalk | At 5MHz | 1, 4 | | | 58 | dB | 4, 6 |
| | | | 1, 4 | | | 56 | dB | 5 |
| CXT | Crosstalk | At 5MHz | 1, 5 | | | 63 | dB | 4, 6 |
| | | | 1, 5 | | | 61 | dB | 5 |
| +Vout | Output Voltage Swing | Rl = 100Ohms | 2 | | +2.6 | | V | 4 |
| | | | 2 | | +2.7 | | V | 5 |
| | | | 2 | | +2.5 | | V | 6 |
| -Vout | Output Voltage Swing | Rl = 100Ohms | 2 | | | -2.6 | V | 4 |
| | | | 2 | | | -2.7 | V | 5 |
| | | | 2 | | | -2.5 | V | 6 |
| Cin | Input Capacitance (noninverting) | | 1 | | | 2.0 | pF | 4, 5, 6 |
| Ro | Output Impedance | At DC | 1 | | | 0.3 | Ohms | 4 |
| | | | 1 | | | 0.2 | Ohms | 5 |
| | | | 1 | | | 0.6 | Ohms | 6 |

# Electrical Characteristics

## AC/DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +6, load resistance (Rl) = 100 Ohms, feedback resistance (Rf) = 500 Ohms, and gain resistance (Rg) = 100 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| CMIR | Common Input Voltage Range | | 1 | | -2.0 | +2.0 | V | 4, 5 |
| | | | 1 | | -1.4 | +1.4 | V | 6 |
| SR | Slew Rate | Measured ±1V with ±3V Step | 1 | | 650 | | V/uS | 4, 6 |
| | | | 1 | | 490 | | V/uS | 5 |
| TRS | Rise and Fall Time | 2V Step | 1 | | | 5.0 | nS | 9, 11 |
| | | | 1 | | | 6.5 | nS | 10 |
| TRL | Rise and Fall Time | 5V Step | 1 | | | 6.0 | nS | 9 |
| | | | 1 | | | 7.0 | nS | 10, 11 |
| Ts | Settling Time | 2V Step at 0.1 percent of the fixed value | 1 | | | 24 | nS | 9, 11 |
| | | | 1 | | | 30 | nS | 10 |
| | | 2V Step at 0.02 percent of the fixed value | 1 | | | 80 | nS | 9, 11 |
| | | | 1 | | | 100 | nS | 10 |
| OS | Overshoot | 2V Step | 1 | | | 10 | % | 9, 10, 11 |

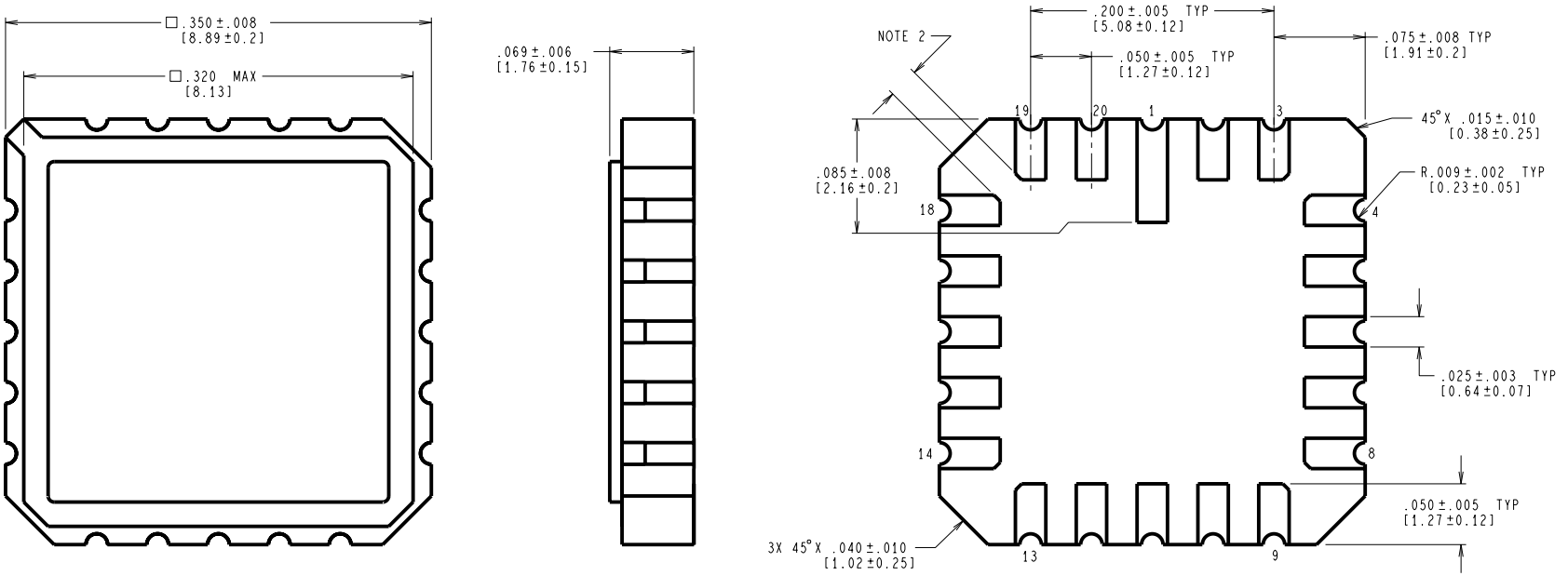
Note 1: If not tested, shall be guaranteed to the limits specified in table
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
Note 4: Three channels are driven simultaneously while observing the output of the undriven fourth channel.
Note 5: One channel is driven with a 2 Vpp pulse while the output of the most affected channel is observed.

## Graphics and Diagrams

| GRAPHICS# | DESCRIPTION |
|---|---|
| 07066HRA2 | CERDIP (J), 14 LEAD (B/I CKT) |
| 07072HRA2 | LCC (E), TYPE C, 20 TERMINAL (B/I CKT) |
| E20ARE | LCC (E), TYPE C, 20 TERMINAL(P/P DWG) |
| J14ARH | CERDIP (J), 14 LEAD (P/P DWG) |
| P000424A | CERDIP (J), 14 LEAD (PINOUT) |
| P000455A | LCC (E), TYPE C, 20 TERMINAL (PIN OUT) |

**See attached graphics following this page.**

| REVISIONS | | | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
| E | REVISE AND REDRAW. | 10005 | 02/10/94 | DEG/ |




CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

| APPROVALS | DATE |
|---|---|
| DRAWN: Dwayne Grady | 02/10/94 |
| DFTG. CHK. | |
| ENGR. CHK. | |
| APPROVAL | |

PROJECTION INCH [MM]

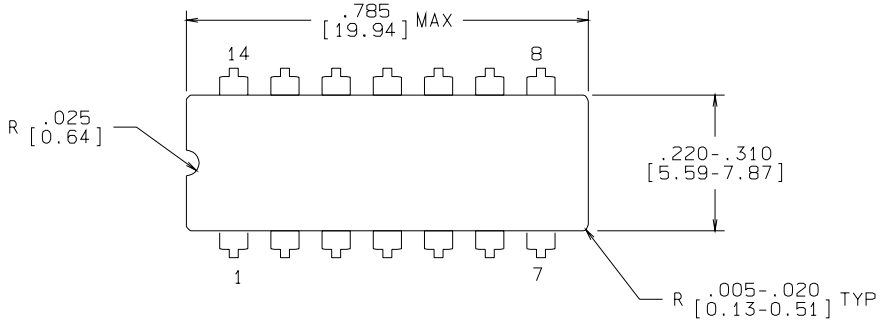
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

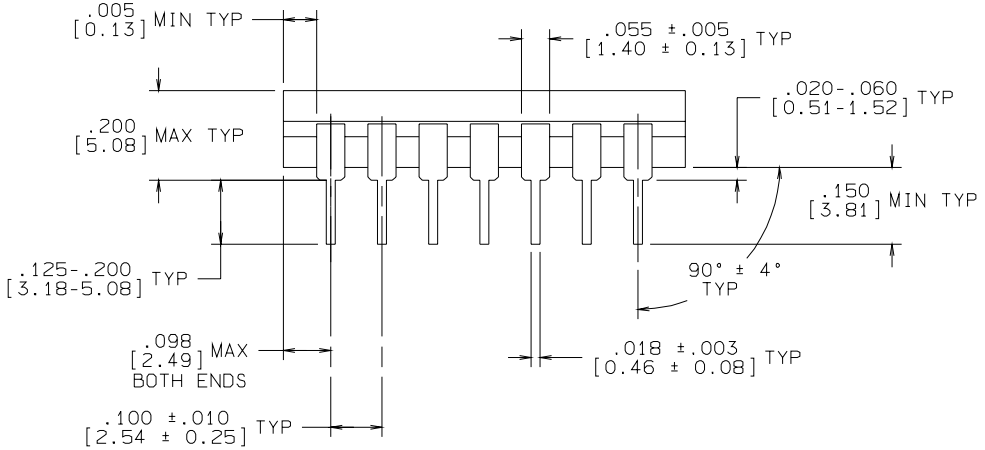
# LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

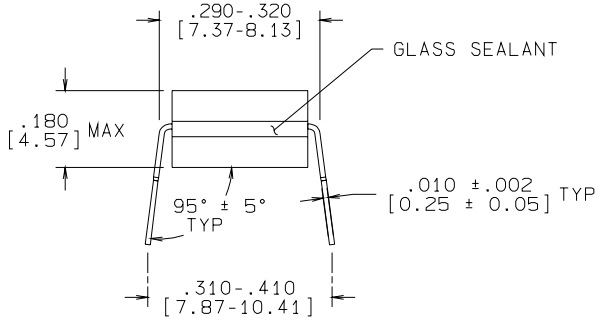
| SCALE | SIZE | DRAWING NUMBER | REV |
|---|---|---|---|
| N/A | C | MKT-E20A | E |

DO NOT SCALE DRAWING | SHEET 1 of 1

| REVISIONS | | | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
| H | REVISE PER CURRENT STD; REDRAW | 10001 | 09/15/93 | TL/ |




CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

| APPROVALS | DATE |
|---|---|
| DRAWN T. LEQUANG | 09/15/93 |
| DFTG. CHK. | |
| ENGR. CHK. | |
| APPROVAL | |

PROJECTION

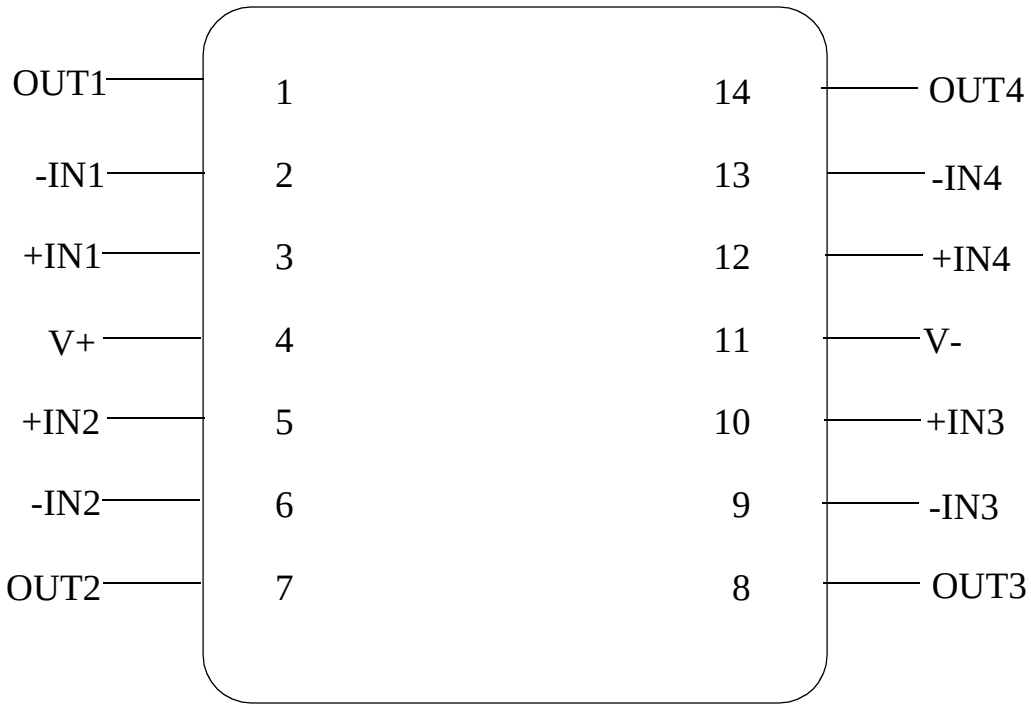
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

# CERDIP (J), 14 LEAD,

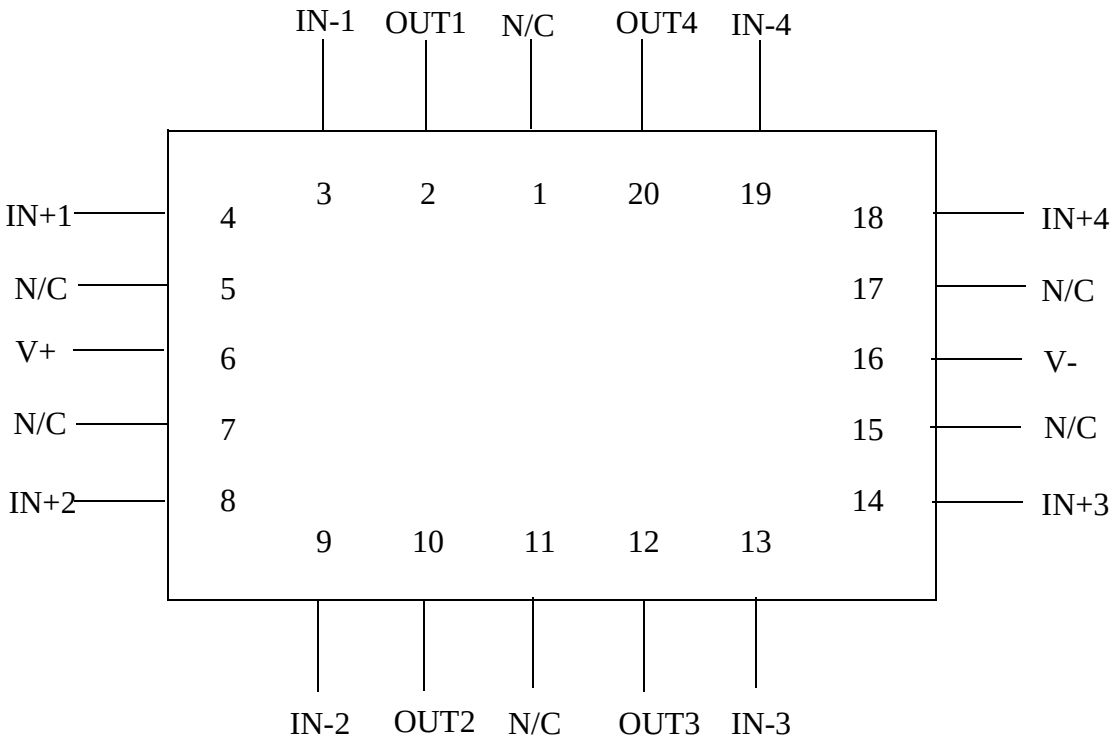
| SCALE | SIZE | DRAWING NUMBER | REV |
|---|---|---|---|
| N/A | B | MKT-J14A | H |

DO NOT SCALE DRAWING | SHEET 1 OF 1




# CLC414J
# 14 - LEAD DIP
# CONNECTION DIAGRAM
# TOP VIEW
# P000424A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050




# CLC414E
# 20 - LEAD LCC
# CONNECTION DIAGRAM
# TOP VIEW
# P000455A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

# Revision History

| Rev | ECN # | Rel Date | Originator | Changes |
|---|---|---|---|---|
| 0A0 | M0002940 | 04/20/01 | Shaw Mead | Initial MDS Release |
| 1A0 | M0003800 | 04/20/01 | Shaw Mead | Changed SSBW limit from 45MHz to 41MHz at 125'C Changed GRF limit from 1.5dB to 1.6dB at 125'C |