National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC404A-X REV 0A0

Original Creation Date: 06/05/98
Last Update Date: 08/18/99
Last Major Revision Date: 06/05/98

WIDEBAND, HIGH-SLEW RATE, MONOLITHIC OP AMP

General Description

The CLC404 is a high-speed, monolithic op amp that combines low power consumption (110mW typical, 120mW maximum) with superior large signal performance. Operating off of ±5V supplies, the CLC404 demonstrates a large-signal bandwidth (5Vpp output) of 165MHz. The bandwidth performance, along with other speed characteristics such as rise and fall time (2.1nS for a 5V step), is nearly identical to the small signal performance since slew rate is not a limiting factor in the CLC404 design.

With its 175MHz bandwidth and 10ns settling (to 0.2%), the CLC404 is ideal for driving ultra-fast flash A/D converters. The 0.5 degree deviation from linear phase, coupled with -53dBc 2nd harmonic distortion and -60dBc 3rd harmonic distortion (both at 20MHz), is well suited for many digital and analog communication applications. These same characteristics, along with 70mA output current, differential gain of 0.07%, and differential phase at 0.03 degree, make the CLC404 an appropriate high-performance solution for video distribution and line driving applications.

Constructed using an advanced, complementary bipolar process and Comlinear's proven current feedback topologies, the CLC404 provides performance far beyond that of other monolithic op amps.

Industry Part Number

CLC404A

NS Part Numbers

CLC404AJ-QML

Prime Die

UB1928B

Controlling Document

5962-9099401MPA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 165MHz large signal bandwidth (5Vpp)
- 2600V/uS slew rate
- Low power: 110mW
- Low distortion: -53dBc at 20MHz
- 10nS settling to 0.2%
- 0.07% diff. gain, 0.03% diff. phase

Applications

- Fast A/D conversion
- Line drivers
- Video distribution
- High-speed communications
- Radar, IF processors

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vs)		±7 Vdc
Output Current (Iout)		70 mA
Differential Input Voltage (Vid)		10 V
Common Mode Input Voltage (Vcm)		±5V dc
Maximum Power Dissipation (Pd) (Note 2)		1.25W
Junction Temperature (Tj)		+175 C
Storage Temperature Range		-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)		+300 C
Thermal Resistance		
Junction -to-ambient (ThetaJA)		
Ceramic DIP	(Still Air)	TBD
	(500 LFPM)	TBD
Junction -to-case (ThetaJC)		
Ceramic DIP		TBD
Package Weight (Typical)		
Ceramic DIP		TBD
ESD Tolerance (Note 3)		
ESD Rating		1000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100 pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±5 Vdc
Gain Range (Av)	+2 to +21 and -1 to -20
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5 V dc, load resistance (Rl) = 100 Ohms, Av = +6, feedback resistance (Rf) = 500 Ohms, and gain settling resistance (Rg) = 100 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (NonInverting)				-22	+22	uA	1, 2
					-44	+44	uA	3
-Iin	Input Bias Current (Inverting)				-18	+18	uA	1
					-22	+22	uA	2
					-40	+40	uA	3
Vio	Input Offset Voltage				-5.0	+5.0	mV	1
					-10.0	+10.0	mV	2
					-9.0	+9.0	mV	3
Tc (+Iin)	Average +Input Bias Current Drift		1		-200	+200	nA/C	2
			1		-275	+275	nA/C	3
Tc (-Iin)	Average -Input Bias Current Drift		1		-200	+200	nA/C	2
			1		-275	+275	nA/C	3
Tc (Vio)	Average Input Offset Voltage Drift		1		-50	+50	uV/C	2, 3
Is	Supply Current	No Load, Quiescent			-12	+12	mA	1, 2, 3
PSRR	Power Supply Rejection Ratio	+Vs = +4.5V to +5.0V, -Vs = -4.5V to -5.0V	2		48		dB	1
			2		45		dB	2, 3
CMRR	Common Mode Rejection Ratio	Vcm = ±1.0 V	1		46		dB	1
			1		44		dB	2, 3
+Iout	Output Current		1		+50		mA	1, 2
			1		+30		mA	3
-Iout	Output Current		1			-50	mA	1, 2
			1			-30	mA	3
Rout	Output Impedance at dc		1			0.2	Ohms	1, 2
			1			0.3	Ohms	3
+Rin	Input Resistance		1		500		KOhms	1
			1		1000		KOhms	2
			1		250		KOhms	3
Cin	Input Capacitance	Ta = +25 C	1			2	pF	4

Electrical Characteristics

DC PARAMETERS:(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5 V dc, load resistance (Rl) = 100 Ohms, Av = +6, feedback resistance (Rf) = 500 Ohms, and gain settling resistance (Rg) = 100 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Vout	Output Voltage Swing	Rl = 100 Ohms	2		+2.7		V	4, 5
			2		+2.3		V	6
-Vout	Output Voltage Swing		2			-2.7	V	4, 5
			2			-2.3	V	6
SSBW	Small Signal Bandwidth	-3 dB Bandwidth, Vout < 2 Vpp			150		MHz	4
			2		120		MHz	5
			2		150		MHz	6
LSBW	Large Signal Bandwidth	-3 dB bandwidth, Vout < 5 Vpp	1		140		MHz	4, 6
			1		110		MHz	5
GFPL	Gain Flatness Peaking Low	At 0.1 MHz TO 40 MHz, Vout ≤2 Vpp				0.3	dB	4
			2			0.4	dB	5, 6
GFPH	Gain Flatness Peaking High	At > 40 MHz, Vout ≤ 2 Vpp				0.5	dB	4
			2			0.7	dB	5, 6
GFR	Gain Flatness Rolloff	At 0.1 MHz to 75 MHz, Vout ≤ 2 Vpp				1	dB	4
			2			1.3	dB	5
			2			1	dB	6
LPD	Linear Phase Deviation	At ≤ 75 MHz, Vout < 2 Vpp	1			1.0	Deg.	4, 6
			1			1.2	Deg.	5
HD2	2nd Harmonic Distortion	2 Vpp at 20 MHz, Vout = 2 Vpp				-45	dBc	4
			2			-45	dBc	5
			2			-40	dBc	6
HD3	3nd Harmonic Distortion	2 Vpp at 20 MHz, Vout = 2 Vpp				-50	dBc	4
			2			-50	dBc	5, 6
SR	Slew Rate	Av = +2, Measured at ±1 V, Cl ≤10 pF, Vout = 3V	1		2000		V/uS	4, 5, 6

Electrical Characteristics

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±5 V dc, load resistance (Rl) = 100 Ohms, Av = +6, feedback resistance (Rf) = 500 Ohms, and gain settling resistance (Rg) = 100 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TRs	Rise and Fall Time	2V step, Cl ≤ 10 pF	1			2.4	nS	9, 11
			1			2.9	nS	10
TRl	Rise and Fall Time	5V step, Cl ≤ 10 pF	1			2.6	nS	9, 11
			1			3.2	nS	10
Ts	Settling Time	2V step at 0.2% of the fixed value, Cl <10 pF	1			15	nS	9, 10, 11
Os	Overshoot	2 V step, Cl ≤ 10 pF	1			12	%	9
			1			15	%	10, 11

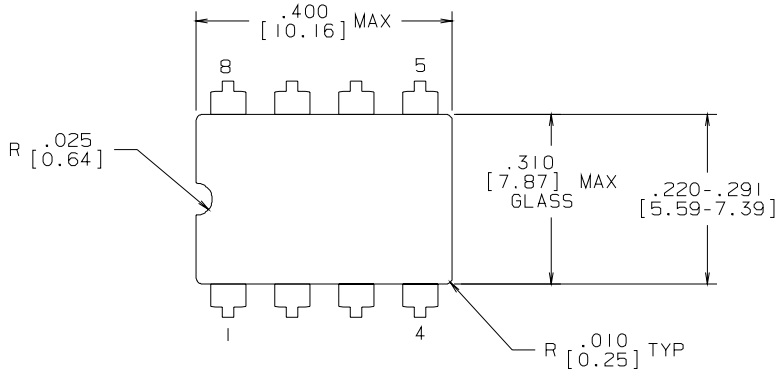
Note 1: If not tested, shall be guaranteed to the limits specified in table I herein.
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this table.

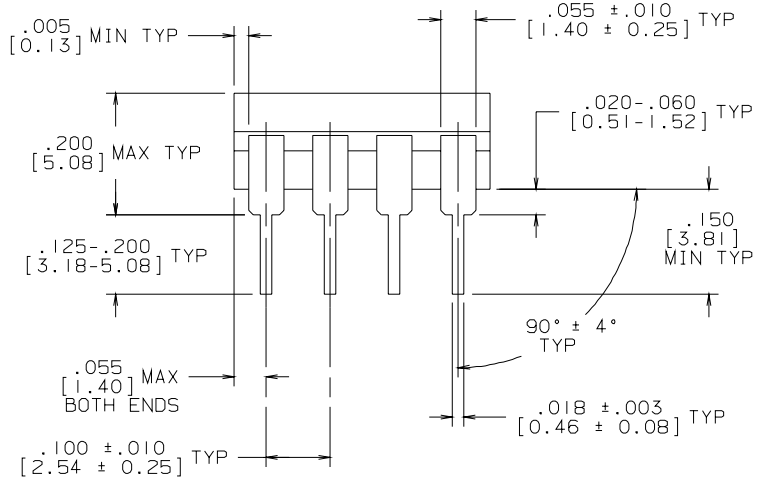
Graphics and Diagrams

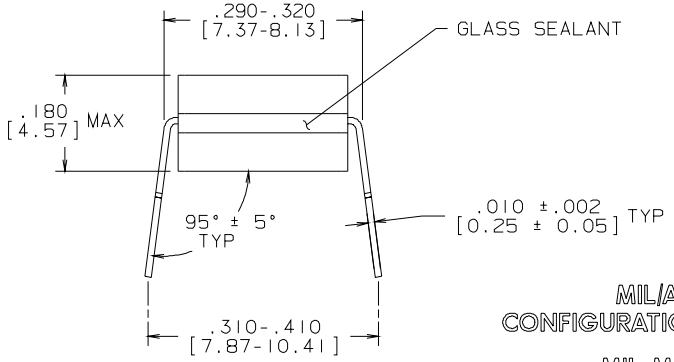
GRAPHICS#	DESCRIPTION
07076HRA2	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000396A	CERDIP (J), 14 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

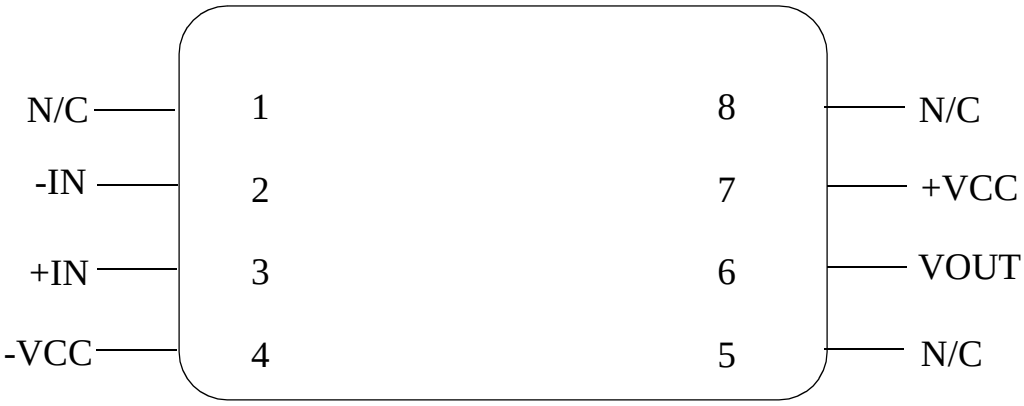
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC404J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000396A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002924	08/18/99	Shaw Mead	Initial MDS Release