Structure Silicon monolithic integrated circuits

Product Name Boost DC/DC converter LSI for Blu-ray

Model Name **BD9997FVT**

Function

(1) The output voltage can be set by external resistance.
(2) Internal Power MOS transistor with Backgate Control function
(3) Inrush current reduction
(4) Integrated Soft start
(5) Built-in Protection function
(NMOS overcurrent limit, overvoltage mute, thermal shutdown, output ground short protection)
(6) UVLO operation at low power-supply voltage
(7) Easy assembly small sized package TSSOP-B8
(8) Built-in Discharge function
(9) function of output interception(at shutdown, at overvoltage)

○Absolute maximum ratings (Ta=25℃)

Item	Symbol	Limit	Unit
Supply voltage	Vcc	−0.3～7	V
Power dissipation (※1)	Pd	0.625	W
Operating temperature range	Topt	−25～+85	℃
Storage temperature range	Tstg	−55～+150	℃
Input voltage range on SW	VINSW	−0.3～15	V
Input voltage range on VOUT	VINOUT	−0.3～15	V
Input voltage range on FB	VINFB	−0.3～VCC+ 0.3	V
AMPOUT terminal maximum input voltage	VINAMPOUT	−0.3～VCC+ 0.3	V
XSHDN terminal maximum input voltage	VINSHDN	−0.3～VCC+ 0.3	V
Junction temperature	Tjmax	+150	℃

(※1) While mounted on Glass-expoxy board(ROHM standard board:70×70×1.6[mm^3])

○Operating conditions (Ta=25℃)

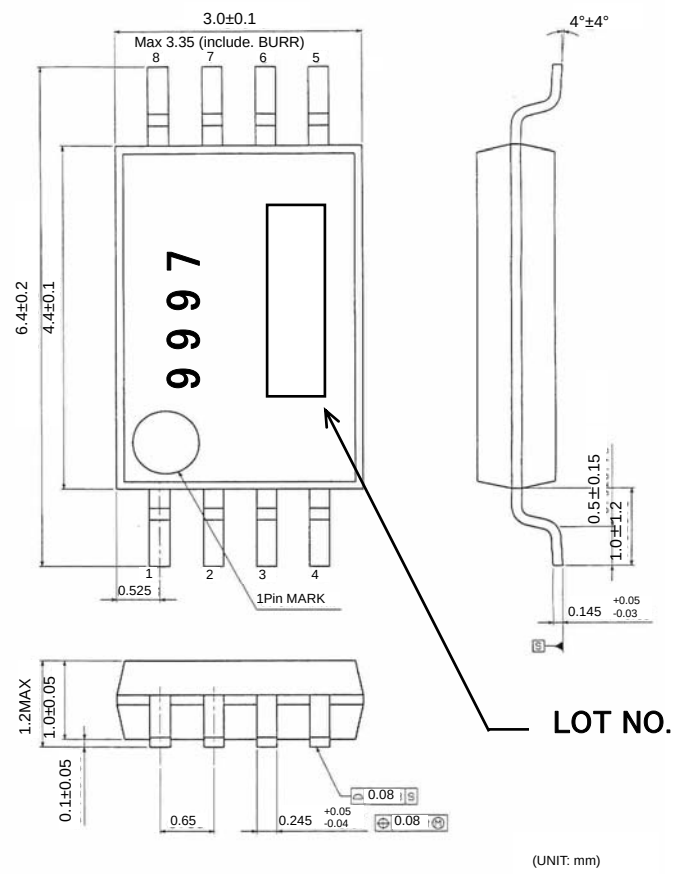
Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Output current1 (※2)(※5)	Iout1	−	−	0.15	A
Output current2 (※3)(※5)	Iout2	−	−	0.10	A
Output current3 (※4)(※5)	Iout3	−	−	0.20	A

(※2) VIN=4.5[V] → VOUT=7.5[V](L=22[uH]) (※3) VIN=4.5[V] → VOUT=11.0[V](L=22[uH])
(※4) VIN=4.5[V] → VOUT=8.1[V](L=10[uH]) (※5) Do not, however exceed Pd.

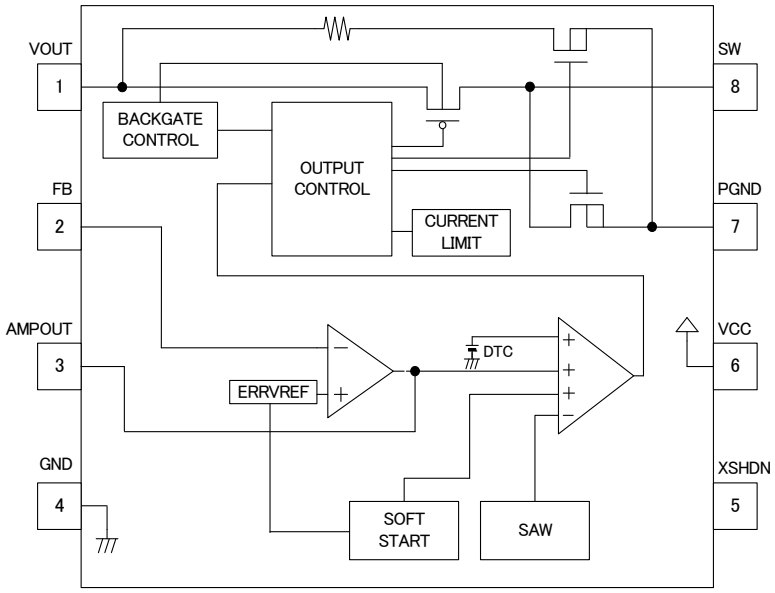
○Electric Characteristics (Unless otherwise specified, Vcc=5.0[V], VOUT=5.0[V], Ta=25[℃])

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Current consumption	ICC1	4.0	6.3	9.5	mA	VCC=5.0[V], FB=2.5[V], No load
Current consumption	ICC2	2.3	3.7	5.2	mA	VCC=5.0[V], FB=0[V], No load
Current consumption (Shutdown mode)	ICC3	—	1	10	μA	VCC=5.0[V], XSHDN=GND or Open
Output voltage range	VOUTR	Vcc	—	12.0	V	
Soft start beginning time	TSOFT	3.5	6.0	8.5	ms	VCC=5.0[V], FB=0[V]
ERRVREF voltage	ERRVREF	0.582	0.600	0.618	V	
Oscillator frequency	SAWO	400	650	900	kHz	
Maximum duty cycle	DMAX	65	80	90	%	
AMPOUT maximum output voltage	VAMPOUTH	2.00	2.30	2.60	V	
AMPOUT minimum output voltage	VAMPOUTL	—	0.03	0.20	V	
PMOS ON resistance	RONP	0.36	0.60	0.84	Ω	VOUT=9.0[V]
NMOS ON resistance	RONN	0.30	0.50	0.70	Ω	VOUT=9.0[V]
UVLO detection voltage	VUVLO1	3.35	3.55	3.75	V	VCC Falling
UVLO return voltage	VUVLO2	3.45	3.65	3.85	V	VCC Rising
XSHDN Input threshold voltage	VthXSHDN	0.92	1.53	2.14	V	
XSHDN pull down resister	RXSHDN	7.0	10.0	13.0	kΩ	

○Package outline



○Block Diagram



○Terminal No./Terminal name

Terminal No	Terminal name
1	VOUT
2	FB
3	AMPOUT
4	GND
5	XSHDN
6	VCC
7	PGND
8	SW

○Operation Notes

1. About grand potential
   Set PGND and GND to equal potential.The ground line is where the lowest potential and transient voltages are connected to the IC.

2. About starting
   Keep light Load at VOUT output while start-up.

3. About board pattern
   Use separates ground lines for small control signals and high current outputs. Because these high current outputs that flows to the wire impedance changes the GND voltage for control signal. Therefore each ground of IC must be connected at one point on the set circuit board. As for GND of external parts, it's similar to the above-mentioned. The characteristics of DC/DC converter might influenced by surrounding components and board pattern. Consider the effects from surroundings while design. Make VCC,PGND and GND impedance sufficiently low Solder RESERVE to GND on set circuit board.

4. About peripheral circuit
   Bypass capacitor between power supply and ground should be use low ESR ceramic capacitor and placed close to the IC pin as possible. External components such as L and C is necessary to be placed as near to the IC as possible with shortest distance. Monitor the output voltage at both end of capacitor connected to VOUT.PMOS over current limit must not be built into, and the over current must not flow to PMOS. please have safe countermeasure such as adding POLY SWITCH and fuse to avoid from over stressing.

5. About absolute maximum rating
   Exceeding supply voltage and operating Temp. over Absolute Maximum Ratings may cause degradation of IC and even may destroy the IC. If special mode such that exceeding Absolute Maximum Ratings is expected, please have safe countermeasure such as adding POLY SWITCH and fuse to avoid from over stressing.

6. About heat design
   Do not exceed the power dissipation (PD) of the package specification rating under actual operation.

7. About Short between terminals and the mis-installation
   While mounting IC on the board, check direction and position of the IC. If inadequately mounted, the IC may destroy. Moreover this IC might be destroyed when dust short the terminals between pins or pin and ground.

8. About operation in strong electromagnetic field
   Strong electromagnetic radiation can cause operation failures.
9. About heat interception circuit (TSD)
   The TSD is activated when the junction temperature (Tj) reaches 175℃ and the output terminal is switched to Hi-Z. The TSD circuit aims to intercept IC from high temperature. The guarantee and protection of IC are not purpose. Therefore, please do not use this IC after TSD circuit operates, nor use it for assumption that operates the TSD circuit.

10. About inspection by set substrate
    The stress might hang to IC by connecting the capacitor to the terminal with low impedance. Then, please discharge electricity in each and all process. Moreover, in the inspection process, please turn off the power before mounting the IC, and turn on after mounting the IC. In addition, please take into consideration the countermeasures for electrostatic damage, such as giving the earth in assembly process, transportation or preservation.

11. About each input terminal
    This IC is a monolithic IC, and has P^+ isolation and P substrate for the element separation. Therefore, a parasitic PN junction is firmed in this P-layer and N-layer of each element. When the GND voltage potential is greater than the voltage potential at Terminals A or B, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GND (P substrate). Please do not apply the voltage to the input terminal when the power -supply voltage is not impressed. Moreover, please impress each input terminal lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage is impressing..

Notes

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