PRELIMINARY

# Am79168/Am79169-275

## TAXIchip™ Transmitter/Receiver Transparent Asynchronous Transmitter/Receiver Interface

Advanced Micro Devices

## DISTINCTIVE CHARACTERISTICS

- **Parallel TTL interface**
  - Eight (8) Data bits, Four (4) Command bits or
  - Ten (10) Data bits, Two (2) Command bits
- **ANSI Fibre Channel X3T9.3 and FC-PH compatible in 8-bit mode**
- **IBM ESCON™ compatible in 8-bit mode**
- **Selectable encoded or unencoded (raw) serial transmission modes**
- **Dedicated TLOOP and RLOOP pins allow easy implementation of loopback test**
- **Parallel data throughput**
  - 17.5 Mbyte/sec to 27.5 Mbyte/sec in 8-bit mode, or
  - 14.6 Mbyte/sec to 22.9 Mbyte/sec in 10-bit mode
- **Serial data throughput 175 Mbaud to 275 Mbaud**
  - 140 Mbit/sec to 220 Mbit/sec in 8-bit mode, or
  - 146 Mbit/sec to 229 Mbit/sec in 10-bit mode
- **+5 V single power supply operation**
- **Serial link interface compatible with standard fiber optic components**
- **Direct interface with transmission lines, no need for extra driver/receiver components**
- **On-chip Phase-Locked-Loop (PLL) requires only an external clock reference**
- **Diagnostic feature $\overline{\text{ESEL}}$ facilitates link integrity testing.**

## GENERAL DESCRIPTION

The Am79168 TAXIchip Transmitter and Am79169 TAXIchip Receiver chipset is a general-purpose interface for very high speed point-to-point communications over coaxial or fiber optic media. TAXIchips emulate a parallel register. They load data into one side and output it on the other, except that, the two sides are separated by a long serial link.

The speed of a TAXIchip system is adjustable over a range of frequencies. The TAXIchips' flexible bus interface scheme accepts bytes that are either 8 or 10 bits wide. Byte transfers can be Data or Command signaling.

Am79168/169 are second generation TAXIchips using an 8B/10B NRZ transmission code. They offer features similar to the Am7968/69.



Publication# 15765 Rev. A Amendment/0
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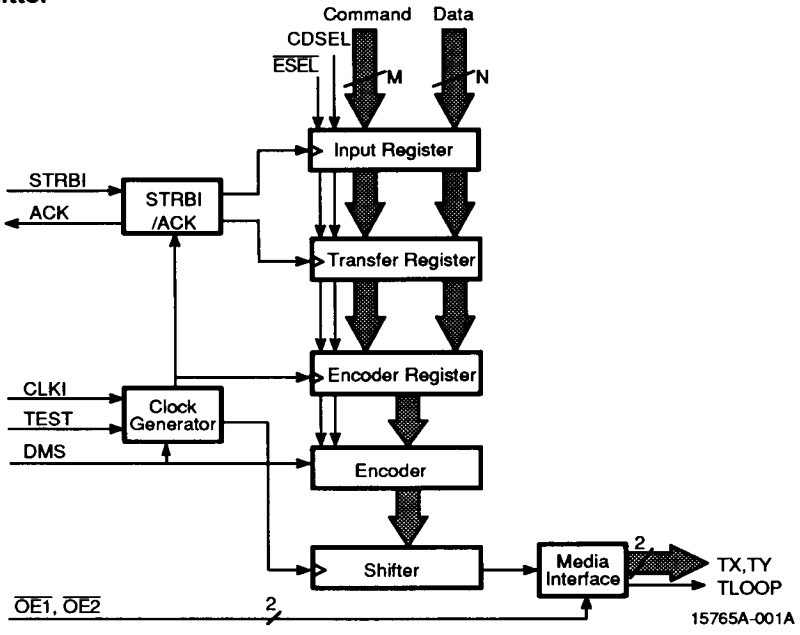
## BLOCK DIAGRAM
## Am79168 Transmitter

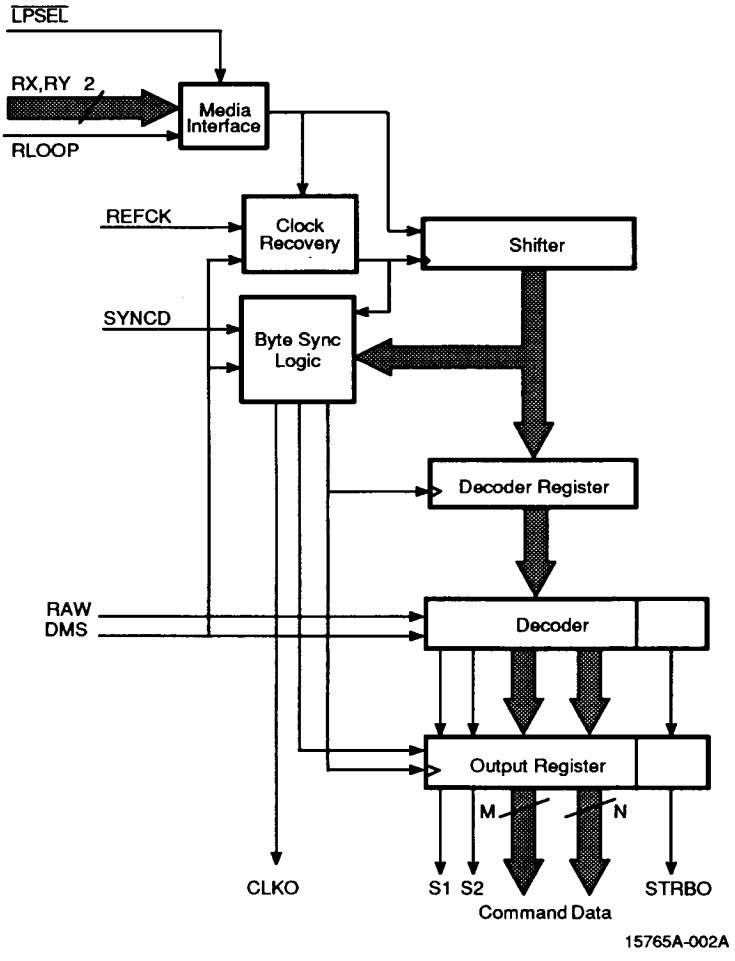



**Note:**

Encoded Data
N can be 8 or 10
M can be 4 or 2
N + M = 12
Raw Data
M = 0
N = 10 or 12

## BLOCK DIAGRAM

### Am79169 Receiver




**Note:**

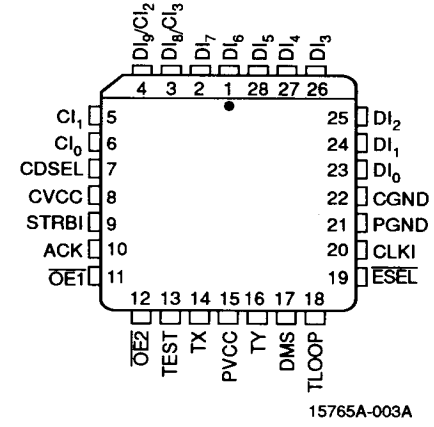
Encoded Data
- N can be 8 or 10
- M can be 4 or 2
- N + M = 12

Raw Data
- M = 0
- N = 10 or 12

## CONNECTION DIAGRAMS (Top View)

### Am79168

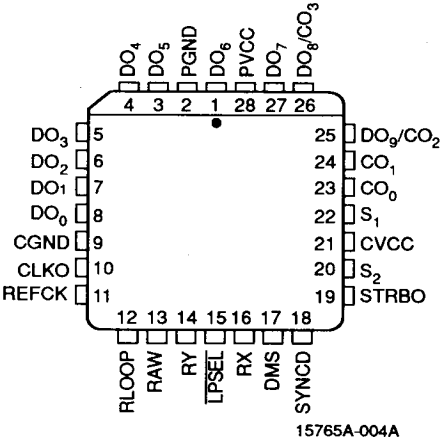
**PLCC**




15765A-003A

### Am79169

**PLCC**

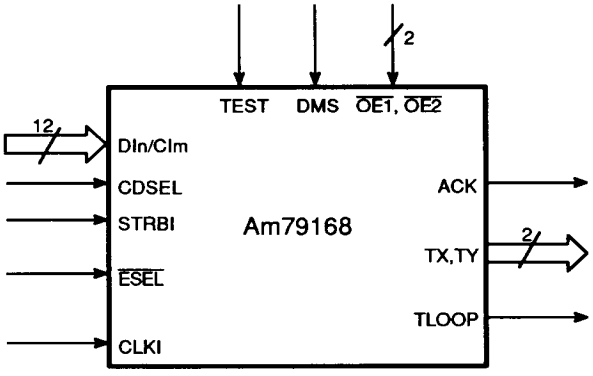



15765A-004A

**Notes:**

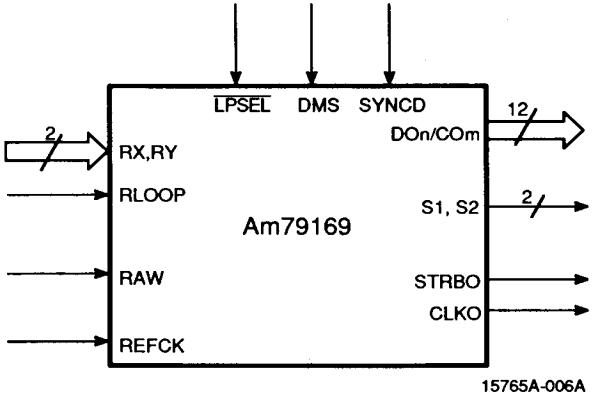
1. Pin 1 is marked for orientation.
2. 28-pin Ceramic Leadless Chip Carrier pinout identical to PLCC.

## LOGIC SYMBOLS




15765A-005A

Vcc = Power Supply (2)
GND = Ground (2)

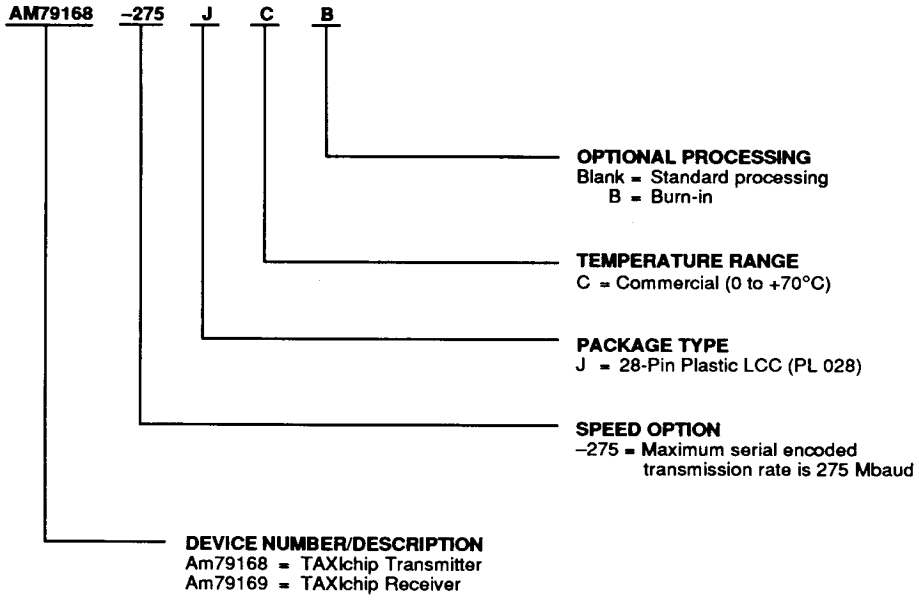



15765A-006A

Vcc = Power Supply (2)
GND = Ground (2)

## ORDERING INFORMATION
## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:




| Valid Combinations | |
|---|---|
| AM79168 | JC |
| AM79169 | JC |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

## PIN DESCRIPTION

The terms Data and Command are used to indicate the groups of pins listed below for all data-width modes.

| Mode | Data MSB ↔ LSB | Command MSB ↔ LSB |
|---|---|---|
| Encoded, 8-bit mode DMS=GND $\overline{ESEL}$=GND | Tx: $DI_7$, $DI_6$, $DI_5$, $DI_4$, $DI_3$, $DI_2$, $DI_1$, $DI_0$<br>Rx: $DO_7$, $DO_6$, $DO_5$, $DO_4$, $DO_3$, $DO_2$, $DO_1$, $DO_0$ | Tx: $CI_3$, $CI_2$, $CI_1$, $CI_0$<br>Rx: $CO_3$, $CO_2$, $CO_1$, $CO_0$ |
| Encoded, 10-bit mode DMS=Vcc $\overline{ESEL}$=GND | Tx: $DI_9$, $DI_8$, $DI_7$, $DI_6$, $DI_5$, $DI_4$, $DI_3$, $DI_2$, $DI_1$, $DI_0$<br>Rx: $DO_9$, $DO_8$, $DO_7$, $DO_6$, $DO_5$, $DO_4$, $DO_3$, $DO_2$, $DO_1$, $DO_0$ | Tx: $CI_1$, $CI_0$<br>Rx: $CO_1$, $CO_0$ |
| Unencoded, 10-bit mode DMS=GND $\overline{ESEL}$=Vcc | Tx: $DI_9$, $DI_8$, $DI_7$, $DI_6$, $DI_5$, $DI_4$, $DI_3$, $DI_2$, $DI_1$, $DI_0$<br>Rx: $DO_9$, $DO_8$, $DO_7$, $DO_6$, $DO_5$, $DO_4$, $DO_3$, $DO_2$, $DO_1$, $DO_0$ | N/A<br>N/A |
| Unencoded, 12-bit mode DMS=Vcc $\overline{ESEL}$=Vcc | Tx: $CI_0$, $CI_1$, $DI_9$, $DI_8$, $DI_7$, $DI_6$, $DI_5$, $DI_4$, $DI_3$, $DI_2$, $DI_1$, $DI_0$<br>Rx: $CO_1$, $CO_0$, $DO_9$, $DO_8$, $DO_7$, $DO_6$, $DO_5$, $DO_4$, $DO_3$, $DO_2$, $DO_1$, $DO_0$ | N/A<br>N/A |

## Am79168 TAXIchip Transmitter

### $DI_0 - DI_7$

**Data Inputs <0–7> (TTL Inputs)**

These inputs accept parallel data from the host system. The Data is latched by STRBI.

### $DI_8/CI_3$

**Data <8> or Command <3> Input (TTL Input)**

This input is either a Data ($DI_8$) or Command ($CI_3$) bit, depending upon the state of the DMS and $\overline{ESEL}$ pins. In 8-bit Encoded mode this pin is $CI_3$. Otherwise, this pin is $DI_8$. $DI_8/CI_3$ is latched by STRBI.

### $DI_9/CI_2$

**Data <9> or Command <2> Input (TTL Input)**

This input is either a Data ($DI_9$) or Command ($CI_2$) bit, depending upon the state of the DMS and $\overline{ESEL}$ pins. In 8-bit Encoded mode, this pin is $CI_2$. Otherwise, this pin is $DI_9$. $DI_9/CI_2$ is latched by STRBI.

### $CI_1, CI_0$

**Command Inputs <1> , <0> (TTL Inputs)**

These inputs accept parallel Command information from the host system. They are latched by STRBI. In the unencoded 12-bit mode, these pins are the 2 most significant bits of the 12-bit data bus.

### CDSEL

**Command or Data Select (TTL Input)**

This input is used to select between Command or Data transmission. When High, the parallel Command inputs are selected to be encoded and transmitted. When Low, the parallel Data inputs are selected to be encoded and transmitted. CDSEL is latched by STRBI. When $\overline{ESEL}$ is High, CDSEL is ignored.

### $\overline{ESEL}$

**Encoded Data Select (TTL Input)**

$\overline{ESEL}$ enables or disables the Data/Command Encoder logic. $\overline{ESEL}$ is latched by STRBI and affects the corresponding parallel data input. When High, 10-bit or 12-bit parallel words (set by DMS) are transmitted without encoding. When Low, 8-bit or 10-bit parallel words (set by DMS) are transmitted as encoded 8B/10B or 10B/12B data. Commands can only be transmitted in Encoded mode.

### DMS

**Data Mode Select (Hard-Wired TTL Select Input)**

This input selects the Data pattern width. The transmission modes for all possible combinations of DMS and $\overline{ESEL}$ are given in the table below.

| Inputs | | |
|---|---|---|
| DMS | $\overline{ESEL}$ | Transmission Mode |
| 0 | 0 | 8-bit Mode, Encoded Data |
| 0 | 1 | 10-bit Mode, Raw Data |
| 1 | 0 | 10-bit Mode, Encoded Data |
| 1 | 1 | 12-bit Mode, Raw Data |

**Note:**
For receiver replace strobed in $\overline{ESEL}$ input with hardwired Raw input.

### STRBI

**Data/Command Strobe Input (TTL Input)**

The rising edge of this input causes both the Data and Command inputs to be latched into the Am79168 Transmitter. STRBI can be tied to CLKI for synchronous operation or STRBI can be operated asynchronously. For

asynchronous operation, the STRBI/ACK protocol must be observed.

### CLKI
**Clock Input (TTL Input)**

This input supplies the reference to the internal PLL clock multiplier. It must be driven by an external crystal-controlled frequency source. The internal state machine counters are synchronized to the falling edge of this signal. In Test mode, the clock-multiplying circuit is disabled and the falling edge of this input supplies the internal bit-clock to the entire circuit .

### $\overline{OE1}$, $\overline{OE2}$
**Output Enable 1, 2 (TTL Inputs, active Low)**

These inputs control the TX/TY and TLOOP serial outputs according to the table below. $\overline{OE1}$ and $\overline{OE2}$ are synchronized internally by the falling edge of CLKI.

| $\overline{OE1}$ | $\overline{OE2}$ | TX/TY Outputs | TLOOP Output |
|---|---|---|---|
| Low | Low | Serial Data | Serial Data |
| Low | High | Serial Data | Low |
| High | Low | Low/High | Serial Data |
| High | High | Off/Off | Low |

Note: output High = $V_{OH}$, output Low = $V_{OL}$, output Off = the output emitter-follower circuit is turned off to allow Pseudo Emitter Coupled Logic (PECL) 'wired–OR.'

### ACK
**Acknowledge (TTL Output)**

ACK High indicates that the Am79168 is ready to accept a new Data and Command. The timing of ACK's response to STRBI depends on the condition of the Transfer Register.

If the Transfer Register is empty when STRBI goes High, new data immediately falls through the Input Register into the Transfer Register and ACK closely follows STRBI. If the Transfer Register contains previously stored data when STRBI is asserted, ACK is delayed until the next falling edge of CLKI. If the ACK signal needs to be observed, STRBI must remain High until the ACK signal is active. ACK is provided as a convenience to asynchronous TAXIchip systems and may be ignored in synchronous systems.

ACK goes Low in response to the falling edge of STRBI.

### TX, TY
**Transmitted Serial Data (Differential PECL Outputs)**

These outputs generate data at PECL voltage levels. When correctly biased, they are capable of driving 50-ohm lines either directly or through isolating capacitors. TX/TY is enabled or disabled by $\overline{OE1}$ and $\overline{OE2}$.

### TLOOP
**Transmitted Loopback Data (Single-Ended PECL Output)**

TLOOP generates the same PECL serial data signal as TX. When correctly biased, it is capable of driving 50-ohm lines either directly or through isolating capacitors. TLOOP can be connected to RLOOP at the Receiver to perform system diagnostic testing. TLOOP is enabled or disabled by $\overline{OE1}$ and $\overline{OE2}$.

### TEST
**Test Mode Enable (Hard-Wired 3-Level Select Input)**

This is a factory test pin and must be wired to ground during normal operation.

### PVCC, CVCC
**Peripheral $V_{CC}$, Core Logic $V_{CC}$ (Power Supply)**

PVCC powers the TTL input/output and PECL output circuits. CVCC powers all internal logic and analog circuits. They are isolated from each other to reduce internal noise coupling, but must be connected to a common external +5 V supply.

### PGND, CGND
**Peripheral GND, Core Logic GND (Ground Pins)**

PGND is used by the TTL circuits. CGND is used by all internal logic and analog circuits. They are separated from each other to reduce internal noise coupling, but must be connected to a common external ground reference.

## Am79169 TAXIchip Receiver

### REFCK
**Reference Clock (TTL Input)**

REFCK is driven by an external crystal-controlled frequency source. REFCK supplies the expected byte-rate frequency reference for the clock and data recovery PLL.

### $\overline{LPSEL}$
**Loop Select (TTL Input, Active Low)**

$\overline{LPSEL}$ Low selects the serial RLOOP data stream input as the received data. This can be used in system diagnostic test to bypass the transmission medium. $\overline{LPSEL}$ High selects the RX/RY input.

### $DO_0$–$DO_7$
**Data Outputs <0–7> (TTL Outputs)**

These outputs reflect the most recent valid Data received by the Receiver.

### $DO_8/CO_3$
**Data <8> or Command <3> Output (TTL Output)**

This output is either a Data ($DO_8$) or Command ($CO_3$) bit, depending on the state of the DMS and RAW pins. In 8-bit Encoded mode, this output is $CO_3$. Otherwise, it is $DO_8$. The output reflects the most recent valid $DO_8$ or $CO_3$ bit received by the Receiver.

### $DO_9/CO_2$
**Data <9> or Command <2> Output (TTL Output)**

This output is either a Data ($DO_9$) or Command ($CO_2$) bit, depending on the state of the DMS and RAW pins. In 8-bit Encoded mode, this output is $CO_2$. Otherwise, it is

$DO_9$. The output reflects the most recent valid $DO_9$ or $CO_2$ bit received by the Receiver.

## $CO_1$, $CO_0$
**Command Outputs <1>, <0> (TTL Outputs)**

These outputs reflect the most recent valid Command received by the Receiver. In 10-bit Raw mode, these outputs are the two most significant bits of the 12-bit data bus.

## S1, S2
**Status Indication 1, 2 (TTL Output)**

These outputs indicate the status of the parallel output data (Data received, Command received, Violation detected, or re-alignment of byte boundary) according to the table given below. The timing of the S1 and S2 outputs is the same as all Data and Command outputs.

| Pin Status | | |
|---|---|---|
| S1 | S2 | Indication |
| 0 | 0 | Data |
| 1 | 0 | Command |
| 0 | 1 | Violation (see Notes 2, 3) |
| 1 | 1 | Re-Align (see Notes 1, 3) |

**Notes:**

1. Re-Align = Byte boundary adjustment made through receipt of SYNC pattern. If a SYNC pattern is received that is aligned with the current byte alignment, no adjustment of the byte boundary is made and Re-Align is not signalled.
2. Violation = Coding violation or Disparity error.
3. In the case of Re-Align, the Data outputs remain unchanged from their previous values while a CMD (5/13) appears on the command outputs (CMD (1/3) in 10-bit mode). In the case of Violation, the Command outputs remain unchanged and the Data outputs reflect a decoded interpretation of the data that was received.

## STRBO
**Command/Data Strobe Output (TTL Output)**

The rising edge of this output signals the presence of new Command or Data at the output register. It is High after new outputs are presented and it goes Low midway through the same byte.

## SYNCD
**Byte Synchronization Disable (TTL Input)**

When High, this pin disables Byte Sync Logic and prevents the SYNC pattern from resetting the byte boundary. For most applications, the SYNCD pin should be tied to GND.

## CLKO
**Clock Output (TTL Output)**

This is a byte rate clock output from the clock-recovery PLL circuit. When data is being received, CLKO is locked to the serial signal. It falls at the time that the Parallel Outputs are updated, and rises at mid-byte. CLKO has no direct frequency relationship with REFCK. CLKO may contain feed-through jitter from the received data. It will be stretched during byte boundary realignment.

## RX, RY
**Received Data (Differential PECL Inputs)**

RX and RY receive differential serial data. They are compatible with typical PECL interfaces. RX and RY can be directly connected to +5 V referenced PECL or AC coupled to –5.2 V referenced ECL.

This input pair has wide common mode voltage range and high differential sensitivity. They can be connected directly to properly terminated transmission lines in wire interconnect systems.

## RLOOP
**Received Loopback Data (Single-Ended PECL Input)**

RLOOP accepts 100K PECL voltage swings, which are referenced to +5 V. This input can be connected to the Am79168 Transmitter TLOOP pin through a terminated line for system level diagnostic loopback test functions.

## DMS
**Data Mode Select (Hard-Wired 3-Level Select Input)**

DMS selects the Data pattern width. The transmission modes for all possible combinations of DMS and RAW are given in the table shown in the Transmitter DMS pin description.

This input also serves as a Test mode enable for factory or incoming inspection. When left open (internally terminated to 1/2 Vcc), the Am79169 is forced into an 8-bit Test mode. In this mode, the internal bit-clock is derived from the REFCK input, instead of the internal PLL.

## RAW
**RAW Data Reception Enable (TTL Input)**

RAW enables or disables the Data/Command Decoder logic. When High, the Receiver converts the incoming serial bit stream into 10-bit or 12-bit (determined by DMS) parallel words and presents these words at the parallel outputs without any decoding. When RAW is Low, the Receiver converts the incoming serial bit stream into decoded 8-bit or 10-bit parallel words.

## PVCC, CVCC
**Peripheral Vcc, Core Logic Vcc (Power Supply)**

PVCC powers the TTL output circuits. CVCC powers all input circuits, internal logic and analog circuits. They are isolated from each other to reduce internal noise coupling, but must be connected to a common external +5 V supply.

## PGND, CGND
**Peripheral GND, Core Logic GND (Ground Pins)**

PGND is used by the TTL output circuits. CGND is used by all inputs, internal logic and analog circuits. They are separated from each other to reduce internal noise coupling, but must be connected to a common external ground reference.

## FUNCTIONAL DESCRIPTION

Unless stated otherwise, all descriptions in this section assume Encoded Mode operation.

### Transmitter Operation

The inputs to the Am79168 Transmitter typically come from two different parts of the sending host system. Data comes from a data channel and represents information transfer between host systems. Command comes from a communication control section of the sending host system. The set of COMMANDs provided by the TAXIchip could be the basis of a user-defined protocol.

When a byte has been latched into the Transmitter by the STRBI input, the Data or Command (selected by CDSEL) is encoded, serialized and shifted out onto the serial link. If the Transmitter $\overline{\text{ESEL}}$ pin is strobed in HIGH, the data bypasses the encoder, is serialized and then shifted out for that byte.

The serial link speed is derived from a crystal-controlled frequency source external to the Transmitter. This source frequency is multiplied by ten (DMS = GND) or twelve (DMS = Vcc) by the internal clock-multiplying PLL. The multiplied frequency gives the baud rate on the serial link.

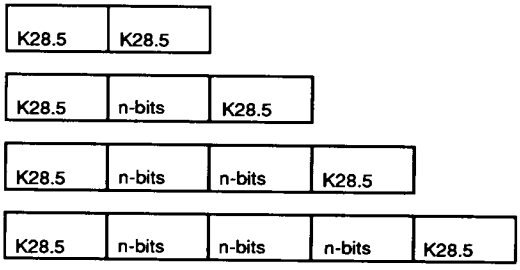
In 8-bit mode, the source frequency can be varied between 17.5 MHz and 27.5 MHz. In 10-bit mode, the source frequency can be varied between 14.6 MHz and 22.9 MHz. The frequency required to achieve the maximum speed of 275 Mbaud on the serial link is given in the table below.

| Data Width Mode | Max. Clock Freq. (MHz) | Max. Parallel Throughput (ns/Byte) | Internal Clock Multiply Ratio | Max. Serial Data Rate (Mbits/sec.) |
|---|---|---|---|---|
| 8-bit | 27.5 | 36.4 | 10 | 220 |
| 10-bit | 22.9 | 43.7 | 12 | 229 |

### TAXI System Byte Alignment

In order to maintain correct symbol boundaries between the Transmitter and Receiver, a SYNC pattern has been chosen which is uniquely recognized by the Receiver. At power-up or if byte alignment is lost through link errors, a SYNC pattern must be sent by the Transmitter to allow the Receiver to reset its byte boundaries.

The SYNC pattern is defined as a K28.5 followed by another K28.5 either immediately or after exactly 1, 2, or 3 sets of n-bits. This fulfills byte alignment requirements for ANSI Fibre Channel Standard and IBM ESCON. Data at the Receiver outputs is aligned after the second K28.5. In 10-bit mode, the K28.D13/18 symbol replaces the K28.5. The four possible SYNC patterns are illustrated in the following diagram.




**Notes:**

1. Valid Symbol can be any valid command or data symbol
2. In 10-bit mode, K28.D13/18 replaces K28.5
3. n = 10 for 8-bit mode
   n = 12 for 10-bit mode

The TAXI Transmitter automatically generates and sends K28.5 symbols (K28.D13/18 in 10-bit mode) when it is not strobed. Also, these symbols can be explicitly sent using the Command channel. Either of these means can be used to generate one of the SYNC patterns. The SYNC pattern will limit the run-length of a byte alignment error. The interval at which SYNC needs to be sent depends solely upon the environment and requirements of the application.

In addition to being part of the specially defined SYNC patterns, the K28.5 (K28.D13/18 in 10-bit mode) symbols have encoded patterns that contain the appropriate number of data transitions to aid Receiver PLL data acquisition and keep it in its optimal operating condition.

### Receiver Operation

The Am79169 Receiver accepts encoded NRZ serial data on the RX/RY or RLOOP inputs. The clock information is extracted from the encoded data using a PLL circuit. The clock-recovery PLL in the Receiver examines every transition in the arriving serial data stream and aligns its own bit-clock with these data transitions. All data transfers and decoding in the Receiver are synchronous to this bit-clock.

The data stream is continuously monitored by the Byte Sync Logic and loaded in parallel into the Decoder on byte boundaries (see block diagram on page 2). The decoded data is latched to either Data or Command outputs synchronous to STRBO. STRBO signals the arrival of new Data or Command in the respective output latches. If an invalid code is detected by the Decoder, S1 and S2 will indicate a Violation.

The Command, Data, S1 and S2 outputs are stable during STRBO pulses. The timing relationship between these outputs and STRBO is derived from the internal

bit-synchronous logic. CLKO is a buffered version of the internal byte boundary clock.

When the Receiver loses byte alignment and upon power-up, subsequent reception of a SYNC pattern causes the Byte Sync Logic to re-establish the byte boundary and signal its detection at the S1 and S2 output pins. When this occurs, CLKO will be stretched to the new byte boundary to guarantee minimum pulse width for receiving systems. When Re-Align is signaled on S1 and S2, the Data and Command outputs do not change. The fragment being processed just prior to this re-acquisition of the byte boundary will be lost.

## Am79168 Transmitter Test Mode

The TEST input pin is used to put the Transmitter into Test mode. This allows the testing of the logic in the Registers, Encoder, and Shifter without involving the PLL. The below mentioned actions must take place to put the chip into Test mode. Either 8-bit or 10-bit mode can be used.

- TEST to Vcc
- CLK the device
- TEST to float to reset to known state
- CLK the device

When the Transmitter is in Test mode, the internal bit-clock is switched out and replaced by the CLKI input, which clocks the serial output data at the CLKI rate.

An automatic test system will be able to clock the part through its functional test patterns at any rate or sequence that is convenient.

## Am79169 Receiver Test Mode

The DMS input is used to put the Receiver into Test mode. This will allow testing of the logic in the Latches, Decoder, and Shifter without involving the PLL. When in Test Mode, only the 8-bit Mode may be used.

When DMS is left open, the internal bit-clock is switched out and replaced by the REFCK input. An automatic test system will then be able to clock the part through its functional test patterns at any rate or sequence that is convenient.

## Am79168 Transmitter Raw Data

The $\overline{\text{ESEL}}$ input on the Transmitter is used to send unencoded data. When $\overline{\text{ESEL}}$ is High, the Encoder logic in the Transmitter is bypassed and the 10-bit or 12-bit (determined by DMS) parallel words that are strobed into the Transmitter are sent serially as raw bits (no encoding). Command inputs and CDSEL are ignored.

When sending raw data, as when sending encoded data, the Transmitter inserts K28.5 (K28.D13/D18 in 12-bit mode) symbols into the serial data stream when it is not strobed.

Sending raw data is useful for diagnostic purposes and for systems that implement a coding scheme other than the 8B/10B and 10B/12B schemes.

Disparity is suspended for both the Transmitter and Receiver during raw data transmission.

## Am79169 Receiver Raw Mode

The RAW input on the Receiver is used to put the Receiver into Raw mode. When in Raw mode (RAW = High), the Decoder logic in the Receiver is bypassed. Serial data is converted into parallel 10-bit or 12-bit words and presented to the receiving system without any decoding.

Function of the SYNCD input is the same in Raw mode as in Encoded mode. If SYNCD is Low, Byte Sync Logic is enabled and word alignment at the Receiver is performed when a SYNC pattern is received. If SYNCD is High, Byte Sync Logic is disabled and raw, unaligned data is presented to the receiving system.

When in Raw mode, the Receiver decodes everything as Data. Hence, the Receiver status outputs (S1 and S2) can only indicate Data and if SYNCD is Low, Re-Align can also be indicated. Several bytes of padding should be allowed before and after a transition of the RAW Pin.

When the Receiver is in Raw mode, a Resync will be output as S1, S2 = 1, with the outputs not representing any particular Data or Command. A Raw mode Resync can be generated in 8-bit mode by the reception of a Command 5 or Command 13 and in 10-bit mode by Command 1 or Command 3.

## Data Encoding/Decoding Format

The encoding/decoding scheme used by the Am79168/79169 is taken from the ANSI Fibre Channel standard. In the 8-bit encoded mode, the code is exactly the 8B/10B code used in Fibre Channel. In this code, 8 data bits are converted into a 10-bit code word (symbol). This is done in two parts. The least significant 5 bits are coded into a 6-bit sub-block using the 5B/6B coding table given and the 3 remaining bits are coded into a 4-bit sub-block using the 3B/4B coding table. The 6-bit sub-block is transmitted serially in the NRZ format in the order a, b, c, d, e, i followed by the 4-bit sub-block in the order f,g,h,j.

In the 10-bit encoded mode, a 10B/12B code is used which is a derivative of the 8B/10B code. In this mode, the 10-bit word is divided into two 5-bit words, which are each encoded into a 6-bit sub-block using the 5B/6B coding table given. Serial transmission is then done identically to 8-bit mode.

The 8B/10B and 10B/12B codes guarantee DC balance by insuring the same average amount of "High" time as "Low" time. By insuring DC balance, the data-induced

noise effects due to DC shifts in an AC-coupled system are minimized.

The DC balance of a code can be characterized by its "Running Disparity". The "Disparity" of a sub-block of code bits is the difference between the number of ones and zeroes in the sub-block. For example, the Disparity of the sub-block 011000 is –2 and the Disparity of the sub-block 110110 is +2. Running Disparity is defined as the cumulative Disparity of all previous sub-blocks. In the 8B/10B and 10B/12B codes, all sub-blocks defined in the 5B/6B and 3B/4B coding tables have a Disparity of –2, 0, or +2. Those sub-blocks with non-zero Disparity have two versions: one with –2 Disparity and one with +2 Disparity. These two versions are complements of each other. Sub-blocks with 0 Disparity have only one version. Two exceptions to this are the encoding D7 and Dx.3 in the 5B/6B and 3B/4B coding tables, respectively. These sub-blocks are balanced (0 Disparity) but have two versions. The decoder always changes the Disparity to + when 000111 is received and to – when 111000 is received. This is done to reduce the maximum run length of the code.

The Running Disparity at the end of any sub-block is always –1 or +1. When a sub-block is sent that has non-zero Disparity, the +2 Disparity version is chosen if the Running Disparity is –1 and the –2 Disparity version is chosen if the Running Disparity is +1. When a 0 Disparity sub-block is sent, the Running Disparity is not changed. Hence, the Running Disparity at sub-block boundaries is always –1 or +1 and the code maintains DC balance. In addition to maintaining DC balance, the sub-blocks defined by the code provide sufficient transition density for clock recovery circuits by limiting run-length to a maximum of 5 bits.

Illustrated in Table 1 below is the naming convention for symbols obtained through a combination of sub-block names from the 5B/6B and 3B/4B tables.

In addition to the 5B/6B and 3B/4B coding tables used for data, special symbols are defined which are used for TAXI Command transmission. These special symbols have names that begin with K instead of the D for data symbols. In the 8-bit mode, Commands D21.5/4 (1110) and D10.5/4 (1111) are special cases in which data sub-blocks are sent. When Command 14 is sent, the TAXI Transmitter chooses to send either D21.4 or D21.5 to guarantee that the Running Disparity after this symbol will be –1. Similarly, when Command 15 is sent, the choice is made between D10.4 or D10.5. These special cases are available to ease implementation of End-of-Frame functions in Fibre Channel compliant systems.

**Table 1. Example of Naming Convention**

| 8-Bit Parallel Data D7 D0 | 5B Encoder Input D4 D0 | 3B Encoder Input D7 D5 | Symbol Name | Encoded Version Current RD – | Encoded Version Current RD + |
|---|---|---|---|---|---|
| 10110010 | 10010 | 101 | D18.5 | 010011 1010 | 010011 1010 |
| 01101101 | 01101 | 011 | D13.3 | 101100 1100 | 101100 0011 |

**Table 2. TAXIchip Data/Command Symbols 5B/6B-Bit Encoder/Decoder**

| Data | 5-Bit Binary | * | 6-Bit Encoded NRZ Sub-Block | ** | * | Alternate Encoded NRZ Sub-Block | ** |
|---|---|---|---|---|---|---|---|
| | $D_4D_3D_2D_1D_0$ | | abcdei | | | abcdei | |
| D0 | 00000 | + | 011000 | – | – | 100111 | + |
| D1 | 00001 | + | 100010 | – | – | 011101 | + |
| D2 | 00010 | + | 010010 | – | – | 101101 | + |
| D3 | 00011 | d | 110001 | d | | | |
| D4 | 00100 | + | 001010 | – | – | 110101 | + |
| D5 | 00101 | d | 101001 | d | | | |
| D6 | 00110 | d | 011001 | d | | | |
| D7 | 00111 | + | 000111 | + | – | 111000 | – |
| D8 | 01000 | + | 000110 | – | – | 111001 | + |
| D9 | 01001 | d | 100101 | d | | | |
| D10 | 01010 | d | 010101 | d | | | |
| D11 | 01011 | d | 110100 | d | | | |
| D12 | 01100 | d | 001101 | d | | | |
| D13 | 01101 | d | 101100 | d | | | |
| D14 | 01110 | d | 011100 | d | | | |
| D15 | 01111 | + | 101000 | – | – | 010111 | + |
| D16 | 10000 | + | 100100 | – | – | 011011 | + |
| D17 | 10001 | d | 100011 | d | | | |
| D18 | 10010 | d | 010011 | d | | | |
| D19 | 10011 | d | 110010 | d | | | |
| D20 | 10100 | d | 001011 | d | | | |
| D21 | 10101 | d | 101010 | d | | | |
| D22 | 10110 | d | 011010 | d | | | |
| D23 | 10111 | + | 000101 | – | – | 111010 | + |
| D24 | 11000 | + | 001100 | – | – | 110011 | + |
| D25 | 11001 | d | 100110 | d | | | |
| D26 | 11010 | d | 010110 | d | | | |
| D27 | 11011 | + | 001001 | – | – | 110110 | + |
| D28 | 11100 | d | 001110 | d | | | |
| D29 | 11101 | + | 010001 | – | – | 101110 | + |
| D30 | 11110 | + | 100001 | – | – | 011110 | + |
| D31 | 11111 | + | 010100 | – | – | 101011 | + |

**Notes:**

*Initial Running Disparity

**Final Running Disparity

d: Running Disparity = either + or –

Serialization order: a is transmitted first, i is transmitted last

**Table 3. TAXIchip Data/Command Symbols 3B/4B-Bit Encoder/Decoder**

| Data | 3-bit Binary | * | 4-bit Encoded NRZ Sub-Block | ** | * | Alternate Encoded NRZ Sub-Block | ** |
|---|---|---|---|---|---|---|---|
| | $D_7D_6D_5$ | | fghj | | | fghj | |
| Dx.0 | 000 | + | 0100 | – | – | 1011 | + |
| Dx.1 | 001 | d | 1001 | d | | | |
| Dx.2 | 010 | d | 0101 | d | | | |
| Dx.3 | 011 | + | 0011 | + | – | 1100 | – |
| Dx.4 | 100 | + | 0010 | – | – | 1101 | + |
| Dx.5 | 101 | d | 1010 | d | | | |
| Dx.6 | 110 | d | 0110 | d | | | |
| Dx.7 | 111 | + | 0001 | – | – | 1110 | + |
| | OR | + | 1000 | – | – | 0111 | + |

**Notes:**

d: Running Disparity = either + or –
Serialization order: f is transmitted first, j is transmitted last

The second 111 code is used when the previously encoded 6B sub-block is 110100, 101100, or 011100 (use 1000) or 100011, 010011, or 001011 (use 0111) to avoid a possible alias K28.5 special character.

**Table 4. TAXIchip Data/Command Symbols 8-Bit Encoder/Decoder**

| Decimal Value | TX Command Input | TX Command Input 4-Bit Binary | * | Encoded NRZ Sub-Block | | ** | * | Alternate NRZ Sub-Block | | ** | RX Command Output 4-Bit Binary |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $C_3C_2C_1C_0$ | | abcdei | fghj | | | abcdei | fghj | | |
| 0 | K28.0 | 0000 | – | 001111 | 0100 | – | + | 110000 | 1011 | + | 0000 |
| 1 | K28.1 | 0001 | – | 001111 | 1001 | + | + | 110000 | 0110 | – | 0001 |
| 2 | K28.2 | 0010 | – | 001111 | 0101 | + | + | 110000 | 1010 | – | 0010 |
| 3 | K28.3 | 0011 | – | 001111 | 0011 | + | + | 110000 | 1100 | – | 0011 |
| 4 | K28.4 | 0100 | – | 001111 | 0010 | – | + | 110000 | 1101 | + | 0100 |
| 5 | K28.5 | 0101 | – | 001111 | 1010 | + | + | 110000 | 0101 | – | 1101/0101 |
| 6 | K28.6 | 0110 | – | 001111 | 0110 | + | + | 110000 | 1001 | – | 0110 |
| 7 | K28.7 | 0111 | – | 001111 | 1000 | – | + | 110000 | 0111 | + | 0111 |
| 8 | K23.7 | 1000 | – | 111010 | 1000 | – | + | 000101 | 0111 | + | 1000 |
| 9 | K27.7 | 1001 | – | 110110 | 1000 | – | + | 001001 | 0111 | + | 1001 |
| 10 | K29.7 | 1010 | – | 101110 | 1000 | – | + | 010001 | 0111 | + | 1010 |
| 11 | K30.7 | 1011 | – | 011110 | 1000 | – | + | 100001 | 0111 | + | 1011 |
| 12 | Reserved | 1100 | d | 001111 | 1010 | + | | No Alternate | | | 1101 |
| 13 | K28.5+ | 1101 | d | 001111 | 1010 | + | | No Alternate | | | 1101 |
| 14 | D21.5/4 | 1110 | – | 101010 | 1010 | – | + | 101010 | 0010 | – | *** |
| 15 | D10.5/4 | 1111 | – | 010101 | 1010 | – | + | 010101 | 0010 | – | *** |

**Notes:**

*Initial Running Disparity

**Final Running Disparity

***Received as Data

d: Running Disparity = either + or –
Serialization order: a is transmitted first, j is transmitted last

Command 13 (K28.5+) can be used to reset the Running Disparity in the Transmitter to +1 so that systems that keep track of Disparity externally can reset the Disparity to a known value. When the Transmitter sends a K28.5, the Receiver will output a K28.5 (Command 5) if the Running Disparity is +1, and a K28.5+ (Command 13) if the Running Disparity is –1.

The 8-bit mode Commands 14 and 15 send D21.4 or D21.5, or D10.4 or D10.5, respectively, depending on the initial Running Disparity. These Commands can be used in sending Fibre Channel End-of-Frame delimiters (see ANSI X3T9.3 Fibre Channel Specification for details).

**Table 5. TAXIchip Data/Command Symbols10-Bit Encoder/Decoder**

| Decimal Value | TX Command Input | TX Command Input 4-Bit Binary | * | Encoded NRZ Sub-Block | | ** | * | Alternate NRZ Sub-Block | | ** | RX Command Output 4-Bit Binary |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $C_1C_0$ | | abcdei | fghjkl | | | abcdei | fghjkl | | |
| 0 | K28.D16 | 00 | – | 001111 | 100100 | – | + | 110000 | 011011 | + | 00 |
| 1 | K28.D13/D18 | 01 | – | 001111 | 101100 | + | + | 110000 | 010011 | – | 11/01 |
| 2 | K28.D14/D17 | 10 | – | 001111 | 011100 | + | + | 110000 | 100011 | – | 10 |
| 3 | K28.D13+ | 11 | d | 001111 | 101100 | + | No Alternate | | | | 11 |

**Notes:**

*Initial Running Disparity

**Final Running Disparity

Serialization order: a is transmitted first, I is transmitted last

When the Transmitter sends a Command 1 (K28.D13 or K28.D18), the Receiver will output a Command 1 if the Running Disparity is –1 (D18 received) and a Command 3 if the Running Disparity is +1 (D13 received).

## Am79168 Transmitter Functional Block Description

Unless stated otherwise, all descriptions in this section assume Encoded Mode operation.

### Clock Generator

Depending upon the state of the DMS pin, the internal PLL multiplies the CLKI reference frequency by ten (8-bit mode) or twelve (10-bit mode) to derive the serial link baud rate.

### Input Register

Data, Command, $\overline{ESEL}$ and CDSEL inputs are clocked into the Input Register by the rising edge of STRBI.

### STRBI/ACK Logic and Transfer Register

If the Transfer Register is empty, data is immediately transferred from the Input Register to the Transfer Register and ACK goes High. If the Transfer Register is full, the data transfer and assertion of ACK will be delayed until the Transfer Register is cleared. ACK indicates a successful transfer into the Transfer Register and a free Input Register.

### Encoder Register

Data is transferred from the Transfer Register to the Encoder Register at each byte boundary by an internal signal which is synchronous with CLKI.

### Encoder

When the corresponding CDSEL bit is Low, the encoder encodes 8 or 10 bits of Data into 10 or 12 code-bits. When the CDSEL bit is High, the 4 or 2 bits of Command are encoded into 10 or 12 code-bits. If $\overline{ESEL}$ is High, the encoder is bypassed.

### Shifter

Parallel encoded data is transferred from the Encoder to the Shifter at each byte boundary, and is then serially shifted to the outputs. The shifter is also responsible for generating K28.5 (K28.13/18 in 10-bit Mode) patterns when the Transmitter is not strobed.

### Media Interface

TX and TY outputs are differential PECL signals. The serial outputs carry the encoded or raw NRZ bit stream. TLOOP is a single-ended PECL serial data output. These outputs are controlled by the $\overline{OE1}$ and $\overline{OE2}$ pins.

## Am79169 Receiver Functional Block Description

Unless stated otherwise, all descriptions in this section assume Encoded Mode operation.

### Media Interface

RX and RY inputs are differential PECL line Receiver inputs. RLOOP is a single-ended PECL serial data input. Selection between RX/RY and RLOOP is done with $\overline{LPSEL}$.

### Clock-Recovery

The Clock-Recovery circuit generates an internal bit-clock synchronized to the incoming serial data stream. When serial data is absent, REFCK provides a frequency reference for the Clock-Recovery circuit.

### Shifter

Serial data is loaded into the Shifter from the Media Interface using the recovered bit-clock.

### Byte Sync Logic

The Byte Sync Logic monitors the contents of the Shifter and resets the byte boundary upon detection of one of the SYNC sequences defined in the Functional Description. If the byte boundary is adjusted, the Byte Sync Logic indicates re-align at the S1 and S2 outputs.

### Decoder Register

Data is transferred from the Shifter to the Decoder Register on the byte boundary.

### Decoder

Content of the Decoder Register is decoded into Command, Data, or a code Violation (invalid code or Disparity error) by the Decoder. In eight-bit mode, 10 input

code bits are decoded into either an 8-bit Data byte or a 4-bit Command. In ten-bit mode, 12 input code bits are decoded into either a 10-bit Data word or a 2-bit Command. If RAW is High, the decoder is bypassed.

The Decoder classifies each symbol as Data, Command or a code Violation and sets S1 and S2 accordingly.

## Output Register

The most recently received and decoded data is loaded from the decoder into the Output Register on the byte boundary. Any Data will be latched to the Data outputs and will not affect the state of the Command outputs. Likewise, any Command will be latched to the Command outputs without affecting the state of the Data outputs. S1 and S2 are similarly transferred from the Decoder into the Output Register on the byte boundary.

When Violation is detected, the Command outputs remain unchanged and the Data outputs reflect a decoded interpretation of the data that was received.

## TAXIchip APPLICATION ISSUES

### Reference Clocks

One master frequency reference source is required for the Am79168 Transmitter, and one is required for the Am79169 Receiver. The CLKI frequency reference for the Transmitter is used to generate the serial link baud rate. The Receiver uses REFCK as a frequency reference for its clock-recovery PLL circuits. The maximum frequency offset of REFCK to the received data frequency is less than 0.2%. In a subsystem with multiple Transmitters and/or Receivers, all CLKI and REFCK inputs can share a common clock reference.

The external clock source must be crystal controlled and continuous. It must not contain 'clock-stretchers' or other similar logic, since this would cause the PLL circuits to behave in unpredictable ways. It is not recommended to use the CLKO of the Receiver directly as a reference clock.

All of the internal logic of the Transmitter runs on an internal clock that is PLL-multiplied from the reference. All of the internal logic of the Receiver runs on the PLL-recovered clock.

### STRBI/ACK Protocol

Inputs to the Am79168 Transmitter are latched into the Input Register by the rising edge of STRBI and later transferred into the Transfer Register when the Transfer Register is empty. The data transfer from the Transfer Register to the Encoder Register occurs at the byte boundary synchronous to CLKI.

In systems where the Transmitter inputs are strobed asynchronously with respect to CLKI, the ACK signal must be used to determine the minimum STRBI spacing. After inputs are latched into the Transfer Register, ACK goes High and STRBI can go Low. The next data pattern can then be presented and strobed into the Transmitter immediately. However, ACK will not rise again until the next transfer between the Input Register and the Transfer Register has been completed. Data can be entered at a rate which is less than the maximum transfer rate without regard to actual byte boundaries. If the STRBI/ACK protocol is observed, individual data bytes can also be strobed into the Transmitter at less than the byte transfer time.

If the STRBI/ACK protocol is not observed, the following will guarantee no loss of data:

- No more than 2 STRBIs within any one byte interval
- No more than 1 STRBI within any subsequent byte interval following a byte interval which had 2 STRBIs, without having an intervening byte interval having no STRBIs (the third STRBI must not occur within 3 bit times of the falling edge of CLKI), and
- The overall STRBI rate should not exceed the CLKI rate.

Note that inputs are latched into the Input Register by the rising edge of STRBI. It is not necessary to hold STRBI High longer than a minimum pulse width for a data transfer. However, if STRBI is not held High until ACK goes High, ACK may not go High. (Refer to STRBI hold time).

Data inputs strobed into the Transmitter may be synchronous with CLKI. In these systems, the ACK output can be ignored and the highest sustained data throughput is reached. Note that if the rising edge of STRBI occurs near the internal byte boundary (within the $t_6$ limits), the Transmitter may process the data within the present or subsequent byte time (see Switching Waveforms, $t_6$).

### Link Error and VIOLATION Status

When the Receiver receives a pattern that cannot be intentionally sent by a Transmitter, Violation status is indicated by the S1 and S2 outputs.

Examples of Violation include:

- Illegal symbol according to the Encode/Decode Table, or
- Mixed Data and Command sub-blocks in the same byte, or
- Any combination of Command sub-block pairs which are not listed in the Command Encode/Decode Table or,
- Valid sub-block pairs which result in a Running Disparity error.

Detection of a Violation does not necessarily indicate that the symbol in which the violation was detected was in error. Violations may result from a prior error which altered the Running Disparity of the bit stream but which did not result in a detectable error at the symbol in which the error occurred. Table 6 illustrates this behavior:

**Table 6. Delayed Violation Detection**

| | RD | Character | RD | Character | RD | Character | RD |
|---|---|---|---|---|---|---|---|
| Transmitted character stream | – | D21.1 | – | D10.2 | – | D23.5 | + |
| Transmitted bit stream | – | 101010 1001 | – | 010101 0101 | – | 111010 1010 | + |
| Bit Stream after error | – | 101010 1011 | + | 010101 0101 | + | 111010 1010 | + |
| Decoded character stream | – | D21.0 | + | D10.2 | + | Code Violation | + |

## Transmitter Serial Output Control

The Transmitter TX/TY outputs can be forced to a Low/High state ($\overline{OE1}$ = High, $\overline{OE2}$ = Low).

The Transmitter TX/TY outputs can also be forced to the OFF/OFF state ($\overline{OE1}$ = High, $\overline{OE2}$ = High). In the OFF/OFF state, these outputs can be "wired-OR" connected. This allows several Transmitters to be multiplexed directly onto a single transmission medium as long as only one of the Transmitters is enabled at any given time.

The $\overline{OE}$ control signals are sampled at the CLKI falling edge by the Transmitter. (The output enable latency to the serial outputs is the same as that of the strobed data.) However, when changing output states in a multiplexed TAXI Transmitter system, several bytes of K28.5 (K28.D13/18 in 10-bit Mode) should precede and follow the $\overline{OE}$ switching so that no user data are lost. The Receiver which is receiving this multiplexed data can use the K28.5 (K28.D13/18 in 10-bit Mode) bytes for synchronization. Violation status should be expected at the Receiver during the transition period.

## Typical Serial Link Timing Parameters

Am79168 Transmitter Output Jitter (for frequency components greater than 1 MHz):

250 ps peak-to-peak at 3.64 ns/bit

Am79168 Transmitter Parallel-in to Serial-out Latency:

Typical delay from the falling edge of CLKI after parallel data are accepted to the first bit out at the serial outputs: approximately 1 byte time

Am79169 Receiver Input Jitter tolerance characteristics (at 3.64 ns/bit, better than $10^{-12}$ bit-error-rate (BER)) :

Peak-to-peak Duty-Cycle Distortion (DCD) tolerance: 1.5 ns

Peak-to-peak Data-Dependent Jitter (DDJ) tolerance: 1.5 ns

Peak-to-peak Random Jitter tolerance: 2.0 ns

Total Peak-to-peak Combined Jitter tolerance: TBD ns

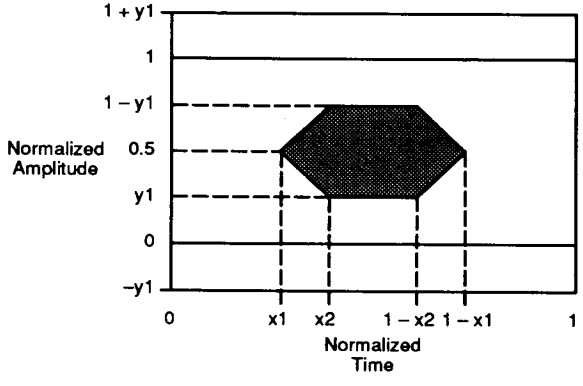
Am79169 Receiver PLL characteristics:

Acquisition Time (from QUIET to valid data): typically less than 2,500 baud intervals

CLKO Range (no input data): REFCK frequency ± 0.7%

Am79169 Receiver Serial-in to Parallel-out Latency:

Typical delay from the first bit of an encoded byte presented at the serial inputs to the falling edge of CLKO associated with that byte: approximately 2.5 byte times




| Rate | x1 | x2 | y1 | Cable Length |
|---|---|---|---|---|
| 266 MBit/s<br>200 MBit/s | TBD | TBD | TBD | TBD |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | –65 to +150°C |
| Ambient Temperature Under Bias | –55 to +125°C |
| Supply Voltage to Ground Potential Continuous | –0.5 V to +7.0 V |
| DC Voltage Applied to Outputs | –0.5 V to $V_{CC}$ Max. |
| DC Input Voltage | –0.5 V to +5.5 V |
| DC Output Current | ±100 mA |
| DC Input Current | –30 to +5.0 mA |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

**Commercial (C) Devices**

| | |
|---|---|
| Temperature ($T_A$) | 0 to +70°C |
| Supply Voltage ($V_{CC}$) | +4.75 V to +5.25 V |

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

### Am79168 TAXIchip Transmitter

| Parameter Symbol | Parameter Description | Test Conditions (Note 1) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **TTL Inputs: DIi, CIi, CDSEL, $\overline{OE1}$, $\overline{OE2}$, STRBI, CLKI, $\overline{ESEL}$, DMS** | | | | | |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = Max. (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = Max. (Note 3) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min., $I_{IN}$ = −18 mA | | −1.5 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = 2.7 V | | 50 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = 0.4 V | | −400 | µA |
| $I_I$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = 5.5 V | | 50 | µA |
| **TTL Output: ACK** | | | | | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = −1 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 4 mA | | 0.45 | V |
| $I_{SC}$ | Output Short Circuit Current | (Note 4) | −15 | −85 | mA |
| **PECL Outputs: TX, TY, TLOOP** | | | | | |
| $V_{OH}$ | Output HIGH Voltage | PECL load | $V_{CC}$ −1.025 | $V_{CC}$ −0.88 | V |
| $V_{OL}$ | Output LOW Voltage | PECL load | $V_{CC}$ −1.81 | $V_{CC}$ −1.62 | V |
| **Power Supplies** | | | | | |
| $I_{CC1}$ | PVCC Supply Current (Note 5) | PVCC = CVCC = Max. | | TBD | mA |
| $I_{CC2}$ | CVCC Supply Current | PVCC = CVCC = Max. | | TBD | mA |

## DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

### Am79169 TAXIchip Receiver

| Parameter Symbol | Parameter Description | Test Conditions (Note 1) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **TTL Inputs: REFCK, $\overline{\text{LPSEL}}$, RAW, SYNCD** | | | | | |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = Max. (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = Max. (Note 3) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min. $I_{IN}$ = –18 mA | | –1.5 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = 2.7 V | | 50 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = 0.4 V | | –400 | µA |
| $I_I$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = 5.5 V | | 50 | µA |
| **TTL Outputs: $DO_i$, $CO_i$, S1, S2, STRBO, CLKO** | | | | | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –1 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 4 mA | | 0.45 | V |
| $I_{SC1}$ | Output Short Circuit Current (STRBO, CLKO) | (Note 4) | –15 | –85 | mA |
| $I_{SC2}$ | Output Short Circuit Current ($DO_i$, $CO_i$, S1, S2) | (Note 4) | –10 | –50 | mA |
| **PECL Differential Inputs: RX, RY** | | | | | |
| $V_{CM}$ | Input Common Mode Voltage | (Note 3) (Note 15) | 3.05 | $V_{CC}$ –1/2 $V_{dif}$ | |
| $V_{dif}$ † | Input Differential Voltage | (Note 3) | .050 | 1.1 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = $V_{CC}$ – 0.88 V | | 220 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = $V_{CC}$ – 1.81 V | 0.5 | | µA |
| **PECL Single-ended Input: RLOOP** | | | | | |
| $V_{IHS}$ | Single-ended input HIGH Voltage | (Notes 3, 6) | $V_{CC}$ –1.165 | $V_{CC}$ –0.88 | V |
| $V_{ILS}$ | Single-ended input LOW Voltage | (Notes 3, 6) | $V_{CC}$ –1.81 | $V_{CC}$ –1.475 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = $V_{CC}$ – 0.88 V | | 220 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = $V_{CC}$ – 1.81 V | 0.5 | | µA |
| **Power Supplies** | | | | | |
| $I_{CC1}$ | PVCC Supply Current | PVCC = CVCC = Max. | | TBD | mA |
| $I_{CC2}$ | CVCC Supply Current | PVCC = CVCC = Max. | | TBD | mA |

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products Group A, Subgroups 9, 10, and 11 are tested unless otherwise noted)(Note 7)

### Am79168 Transmitter

| No. | Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Am79168 Transmitter Parallel Interface (Note 8)** | | | | | | |
| 0 | $t_{T0}$† | Internal Bit Clock Period | (Definition only) | 3.64 | 5.71 | ns |
| 1 | $t_P$ | CLKI Period (Note 9) | | $nt_{T0}$ (Min) | $nt_{T0}$ (Max) | ns |
| 2 | $t_{PW}$ | CLKI Pulse Width HIGH | | 10 | | ns |
| 3 | $t_{PW}$ | CLKI Pulse Width LOW | | 10 | | ns |
| 4 | $t_{PW}$ | STRBI Pulse Width HIGH (Note 10) | | 10 | | ns |
| 5 | $t_{PW}$ | STRBI Pulse Width LOW | | 10 | | ns |
| 6 | $t_{BB}$ | STRBI rise to CLKI fall internal byte boundary. (Note 11) | | 0 | 10 | ns |
| 7 | $t_S$ | $\overline{OE1}$, $\overline{OE2}$ to CLKI Fall Setup Time | | 10 | | ns |
| 8 | $t_H$ | $\overline{OE1}$, $\overline{OE2}$ to CLKI Fall Hold Time | | 0 | | ns |
| 9 | $t_S$ | Data to STRBI Rise Setup Time | | 8 | | ns |
| 10 | $t_H$ | Data to STRBI Rise Hold Time | | 2 | | ns |
| 11 | $t_H$ | ACK rise to STRBI Fall Hold (Note 12) | TTL Output Load | 0 | | ns |
| 12 | $t_H$ | ACK fall to STRBI Rise Hold (Note 12) | TTL Output Load | 0 | | ns |
| 13 | $t_{PD}$ | STRBI rise to ACK rise Delay (Note 13) | TTL Output Load | | 20 | ns |
| 14 | $t_{PD}$ | STRBI fall to ACK fall Delay | TTL Output Load | | 14 | ns |
| 15 | $t_{PD}$ | CLKI fall to ACK rise (Busy-ACK) (Note 13) | TTL Output Load | | $3t_{T0}$+16 | ns |
| **Transmitter SERIAL Data Outputs** | | | | | | |
| 19 | $t_{SK}$† | TX, TY Skew | PECL Output Load | | 50 | ps |
| 20 | $t_R$† | TX, TY, TLOOP Rise Time | PECL Output Load | 0.3 | 1.2 | ns |
| 21 | $t_F$† | TX, TY, TLOOP Fall Time | PECL Output Load | 0.3 | 1.2 | ns |
| 22 | $t_{PAD}$† | TX, TY, TLOOP Phase Angle Distortion (Note 14) | PECL Output Load | –7.5 | +7.5 | deg |

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products Group A, Subgroups 9, 10, and 11 are tested unless otherwise noted)(Note 7)

### Am79169 Receiver

| No. | Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Am79169 Receiver Parallel Interface (Notes 8, 9)** | | | | | | |
| 31 | $t_{R0}$† | Internal Bit Clock Period | (Definition only) | 3.64 | 5.71 | ns |
| 32 | $t_P$ | REFCLK Period (Note 9)<br>Data Frequency Offset | | n3.64 | n5.71 | ns |
| 33 | $t_{PW}$ | REFCK Pulse Width HIGH | | 10 | | ns |
| 34 | $t_{PW}$ | REFCK Pulse Width LOW | | 10 | | ns |
| 35 | $t_S$ | Data to STRBO rise Setup | TTL Output Load | $2t_{R0}$–2 | | ns |
| 36 | $t_{PD}$ | STRBO rise to CLKO rise | TTL Output Load | $At_{R0}$–2 | | ns |
| 37 | $t_{PD}$ | CLKO rise to STRBO fall | TTL Output Load | $t_{R0}$–2 | $t_{R0}$+5 | ns |
| 38 | $t_{PD}$ | CLKO fall to Data Invalid | TTL Output Load | –4 | | ns |
| 39 | $t_{PD}$ | CLKO fall to Data valid | TTL Output Load | | 4 | ns |
| 40 | $t_{PW}$ | STRBO Pulse Width HIGH | TTL Output Load | $Bt_{R0}$–5 | | ns |
| 41 | $t_{PW}$ | CLKO Pulse Width HIGH | TTL Output Load | $Ct_{R0}$–5 | | ns |
| 42 | $t_{PW}$ | CLKO Pulse Width LOW | TTL Output Load | $Dt_{R0}$–5 | | ns |

**Notes:** *

† Not included in group A tests.

1. For conditions shown as Min or Max, use the appropriate values specified under operating range.
3. Measured with device in Test mode while monitoring output logic states.
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. The Transmitter $I_{CC1}$ is tested with all PECL outputs terminated to $V_{CC}$ (unloaded). The PECL outputs (TX/TY and TLOOP) contribute 25 mA (when TLOOP is LOW) or 45 mA (when TLOOP is HIGH) nominally to $I_{CC1}$ when they are loaded with PECL loads, 50 ohms to ($V_{CC}$–2). In calculating the chip power dissipation, the contribution by the output loads shall be multiplied by 1 V instead of by $V_{CC}$.
6. Device thresholds on the RLOOP pin are verified during production test by ensuring that the input threshold is less than $V_{IHS}$ (min) and greater than $V_{ILS}$ (max). The figure below shows the acceptable range (shaded area) for the transition voltage.

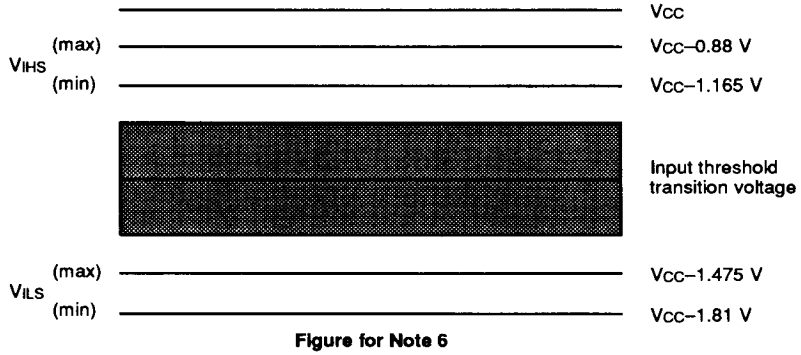



**Figure for Note 6**

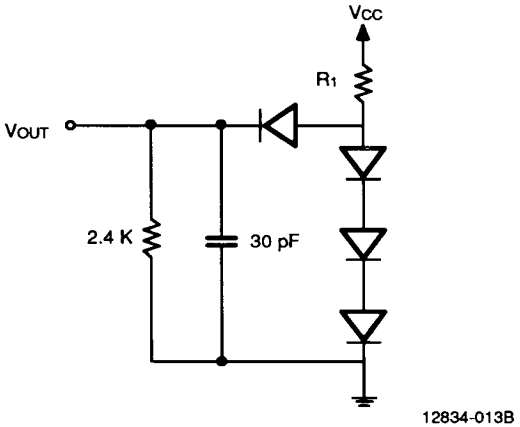
**Notes:**

7. All timing references are made with respect to + 1.5 V for TTL-level signals or to the 50% point between $V_{OH}$ and $V_{OL}$ for PECL signals. PECL input rise and fall times must be 2 ns ± 0.2 ns between 20% and 80% points. TTL input rise and fall times must be 2 ns ± 0.2 ns between 1 V and 2 V.
8. For the Am79168 Transmitter, "Data" includes $DI_{7-0}$, $DI_8/CI_3$, $DI_9/CI_2$, $CI_1$, $CI_0$, $\overline{ESEL}$, and CDSEL. For the Am79169 Receiver, "Data" includes $DO_{7-0}$, $DO_8/CO_3$, $DO_9/CO_2$, $CO_1$, $CO_0$, $S_1$ and $S_2$.
9. $t_{R0} = t_{T0}$ of the Transmitter to which the Receiver PLL is locked.

| | 8-Bit Mode | 10-Bit Mode |
|---|---|---|
| n= | 10 | 12 |
| A= | 3 | 4 |
| B= | 4 | 5 |
| C= | 5 | 6 |
| D= | 5 | 6 |

10. $t_4$ guarantees that data is latched. $t_{11}$ timing may not be valid.
11. $t_5$ (Internal Byte Boundary to CLK fall) is created by the variation of internal STRBI propagation delays relative to internal byte boundaries over temperatures and $V_{CC}$ ranges .The internal byte boundary determines the byte in which data will be transmitted at the serial outputs (TX/TY and TLOOP). If STRBI occurs before the byte boundary, then the data will be sent out in the next byte. If STRBI occurs after the byte boundary, then the output data will be delayed by one additional byte.
12. If $t_{11}$ is not met, ACK response and timing are not guaranteed, but data will still be latched on STRBI rising edge.
13. ACK delay is determined by $t_{13}$ when the Transfer Register is empty or by $t_{15}$ when the Transfer Register is full (Busy mode). "Busy ACK" occurs any time a second STRBI is applied prior to the clearing of the Transfer Register. When this occurs, active ACK does not depend on STRBI. Instead, ACK will be synchronous to the data transfer from the Transfer Register into the Encoder Register, thus $t_{15}$ is defined with respect to CLKI.
14. $t_{22}$ defines the maximum deviation of a given TX/TY transition from its ideal location relative to the previous transition. Where 1 bit-time is 360°, this deviation is expressed as ±x° phase deviation.
15. Voltages applied to either of the differential input pins should not be above $V_{CC}$ or below +2.5 V to assure proper operation.

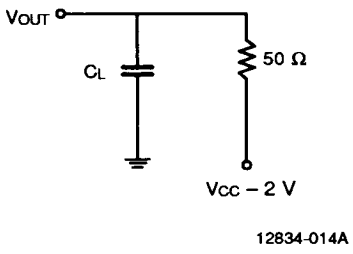
## SWITCHING TEST CIRCUITS




**TTL Output Load**

**Notes:**

1. $R_1$ = 1K Ω for the $I_{OL}$ = 4 mA
2. All diodes IN916 or IN3064, or equivalent
3. $C_L$ = 30 pF includes scope probe, wiring and stray capacitances without device in test fixture.
4. AMD uses constant current (A.T.E.) load configurations and forcing functions. This figure is for reference only.

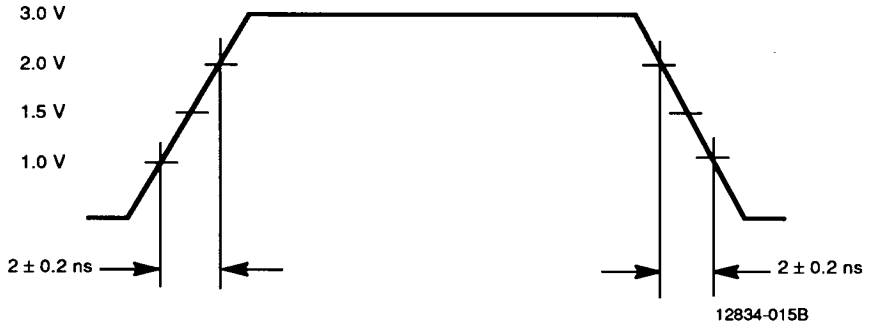



**ECL Output Load**

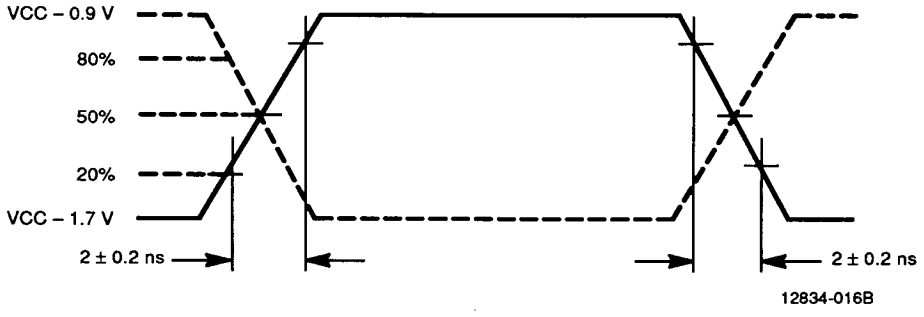
**Notes:**

1. $C_L \leq 3$ pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. AMD uses Automatic test equipment load configurations and forcing functions. This figure is for reference only.

## SWITCHING TEST WAVEFORMS




**TTL Input Waveform**




**ECL Input Waveform**

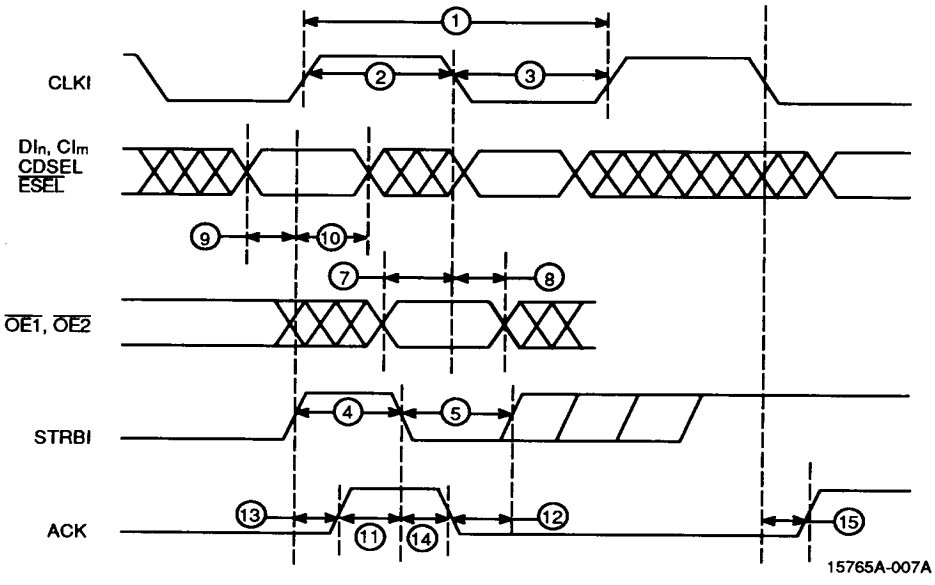
## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be Steady | Will be Steady |
| | May Change from H to L | Will be Changing from H to L |
| | May Change from L to H | Will be Changing from L to H |
| | Don't Care, Any Change Permitted | Changing, State Unknown |
| | Does Not Apply | Center Line is High-Impedance "Off" State |

KS000010

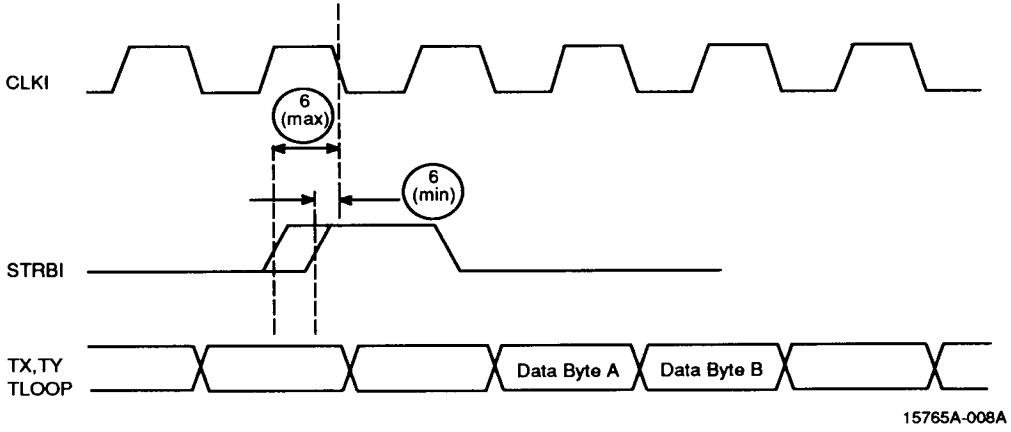
## SWITCHING WAVEFORMS

### Am79168 Transmitter



## SWITCHING WAVEFORMS

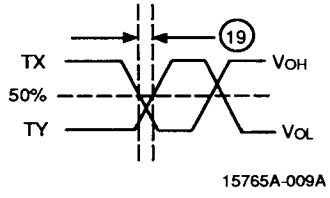
### Am79168 Transmitter

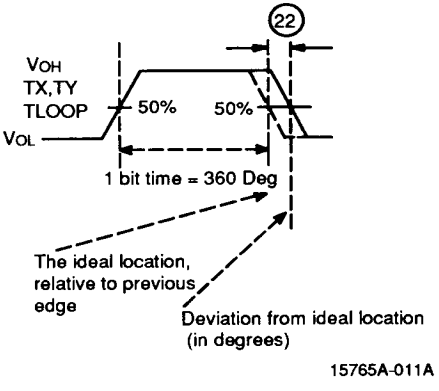


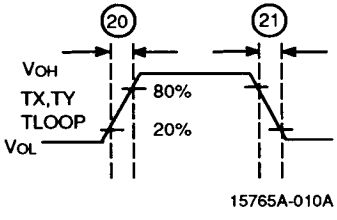

When STRBI occurs before $t_6$ (max), the strobed data will appear at "Data Byte A" position at the serial outputs.

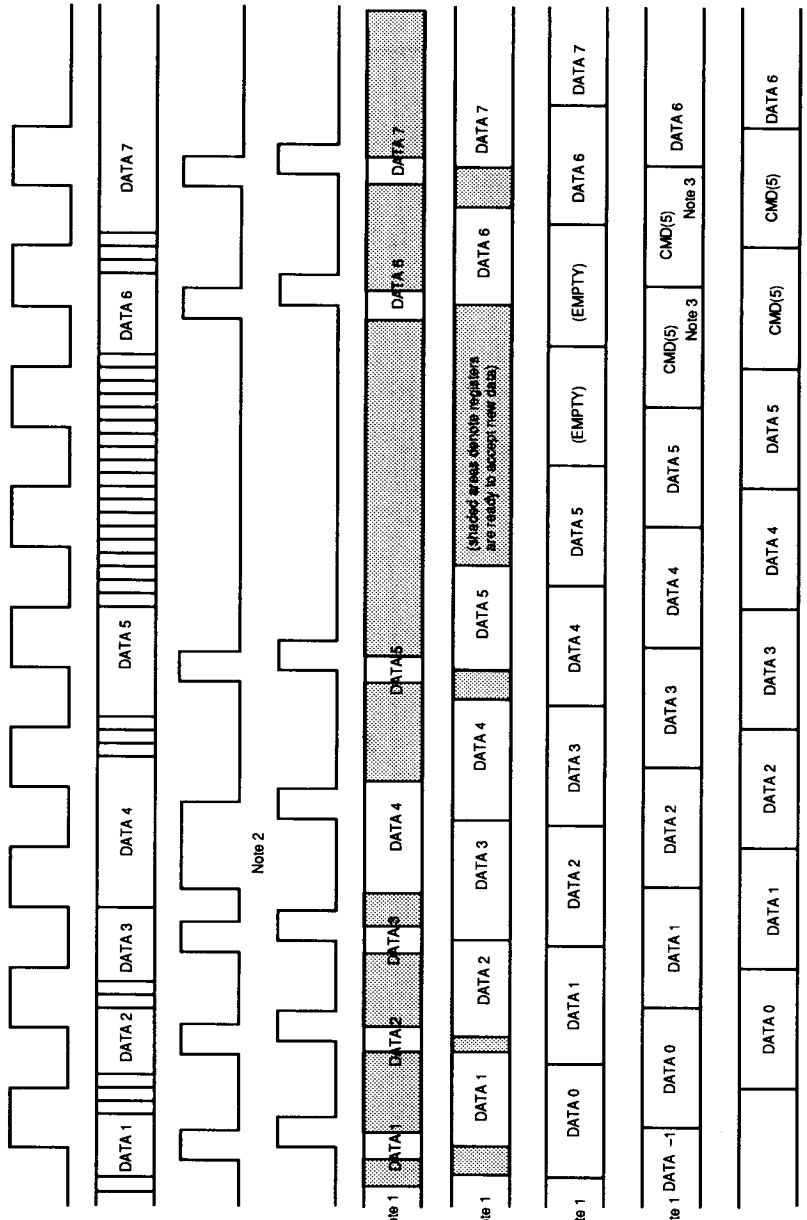
When STRBI occurs after $t_6$ (min), the strobed data will appear at "Data Byte B" position at the serial outputs.

When STRBI occurs within the $t_6$ (min) to $t_6$ (max) window, the strobed data may appear at either position at the serial outputs.






15765A-012A

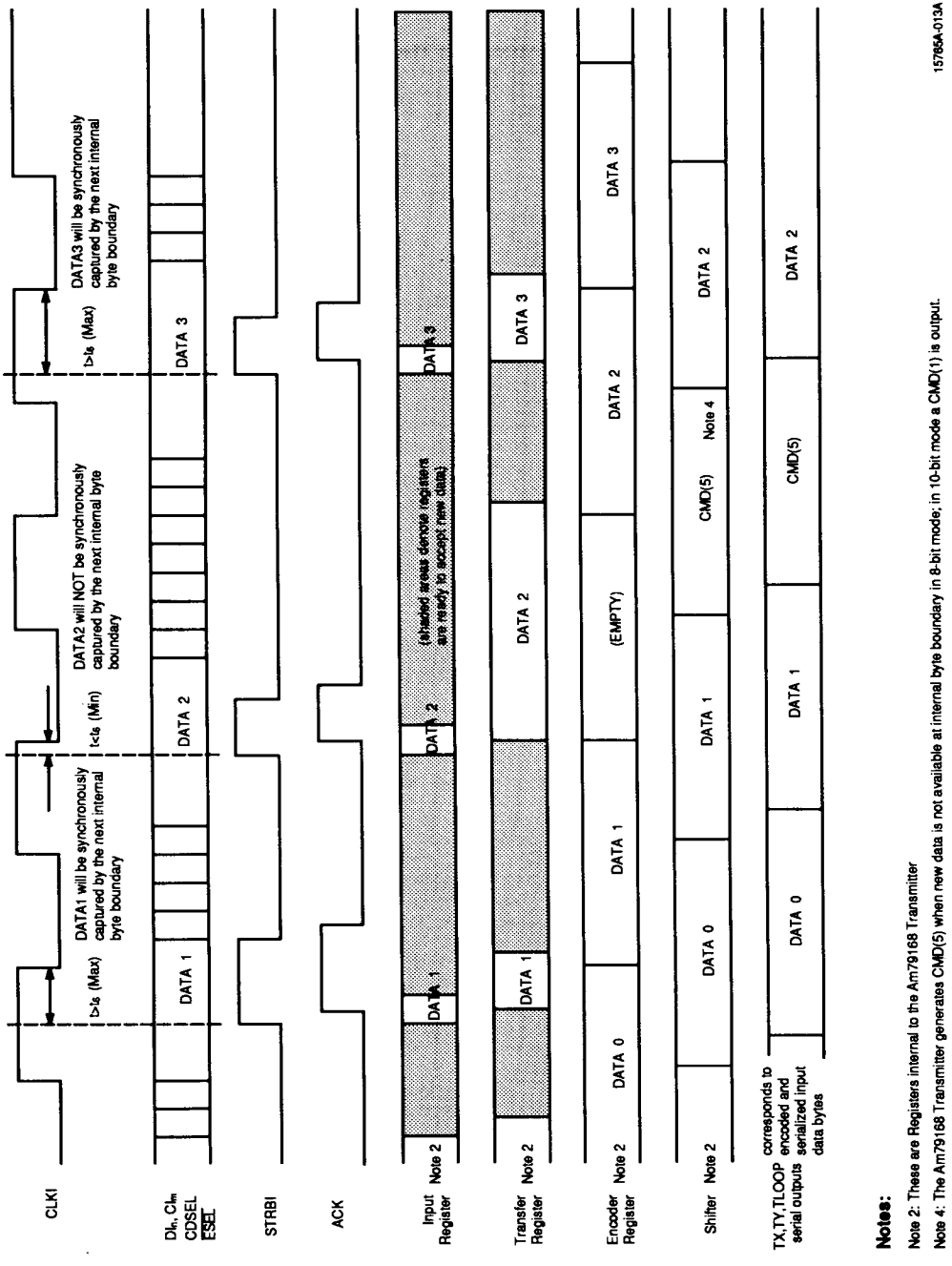
**Notes:**

Note 1: These are Registers internal to the Am79168 Transmitter

Note 2: When two STRBIs occur within the same 'byte', ACK is delayed until the Transfer Register is loaded

Note 3: The Transmitter generates a CMD(5) when new data is not available at the byte boundary in 8-bit mode; in 10-bit mode a CMD(1) is output.

## SWITCHING WAVEFORMS
### Am79168 Transmitter (STRBI-Byte Boundary)




15765A-013A

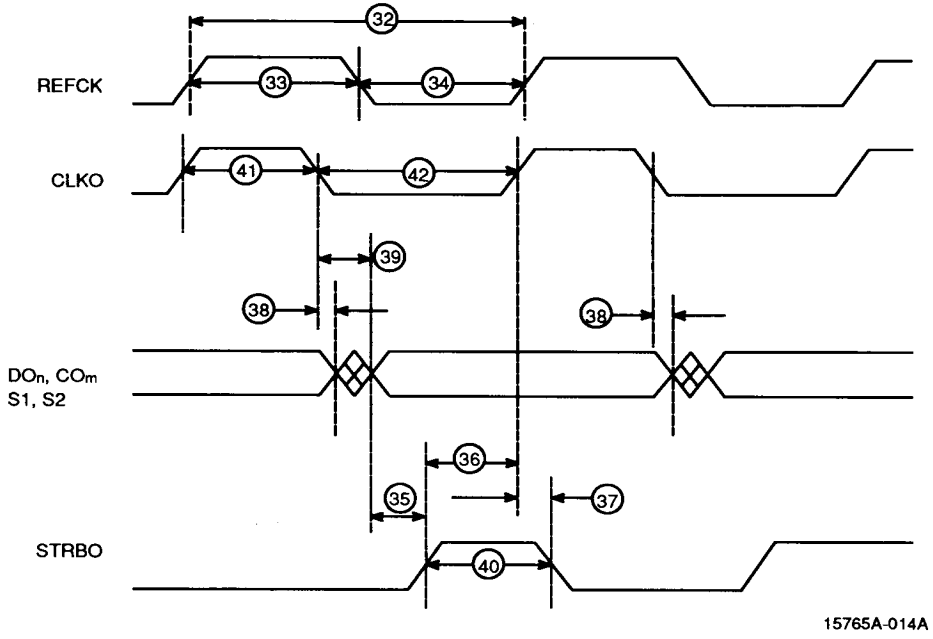
**Notes:**

Note 2: These are Registers internal to the Am79168 Transmitter

Note 4: The Am79168 Transmitter generates CMD(5) when new data is not available at internal byte boundary in 8-bit mode; in 10-bit mode a CMD(1) is output.

## SWITCHING WAVEFORMS

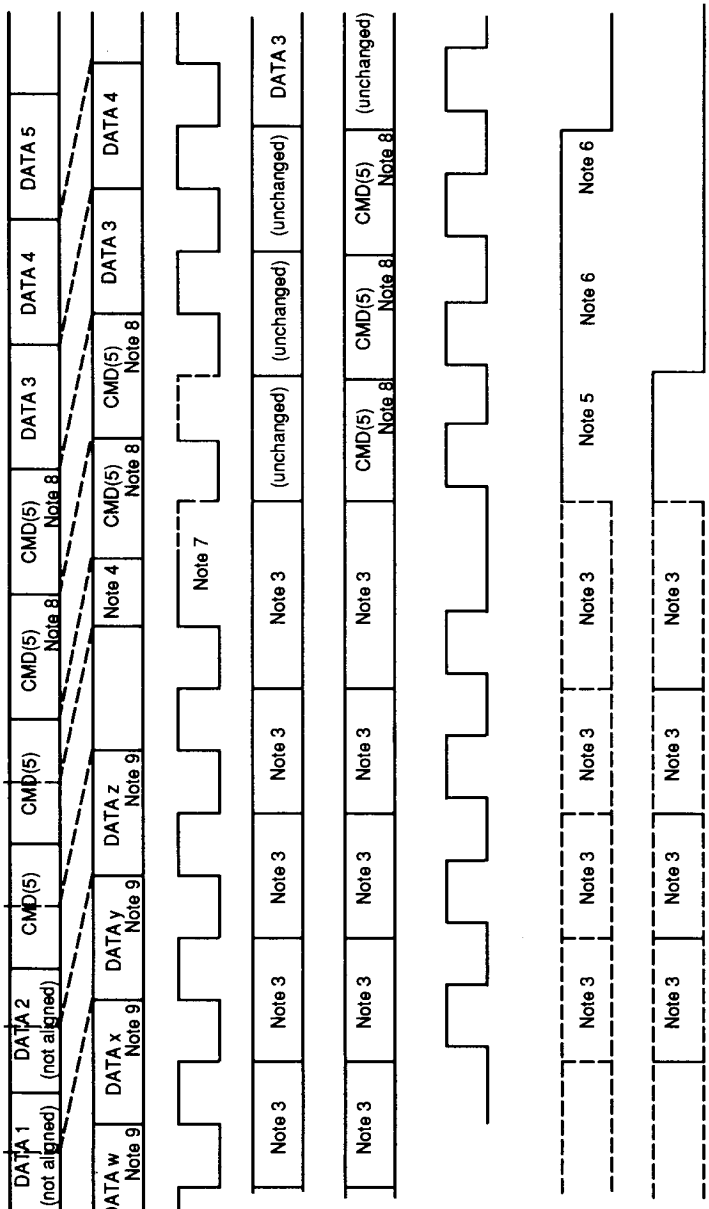
### Am79169 Receiver



## SWITCHING WAVEFORMS

### Am79169 Receiver (Byte Re-alignment) (Note 8)

### RX/RY or RLOOP Serial Inputs




**Notes:**

Note 1: The CMD(5) may occur exactly 1, 2, 3, or 4 bytes after the first and will generate a Re-Align

Note 2: Register internal to the Am79169 Receiver

Note 3: The Receiver may or may not indicate VIOLATION (it is possible for a mis-aligned byte to be decoded into a valid DATA or COMMAND)

Note 4: The Receiver resets internal byte boundary and indicates RE-SYNC condition upon serial detection of the second CMD(5)
The Decoder content and the fragmented byte is lost, due to byte boundary adjustment.

Note 5: The Receiver indicates Re-Align is done after the second CMD(5) is recognized

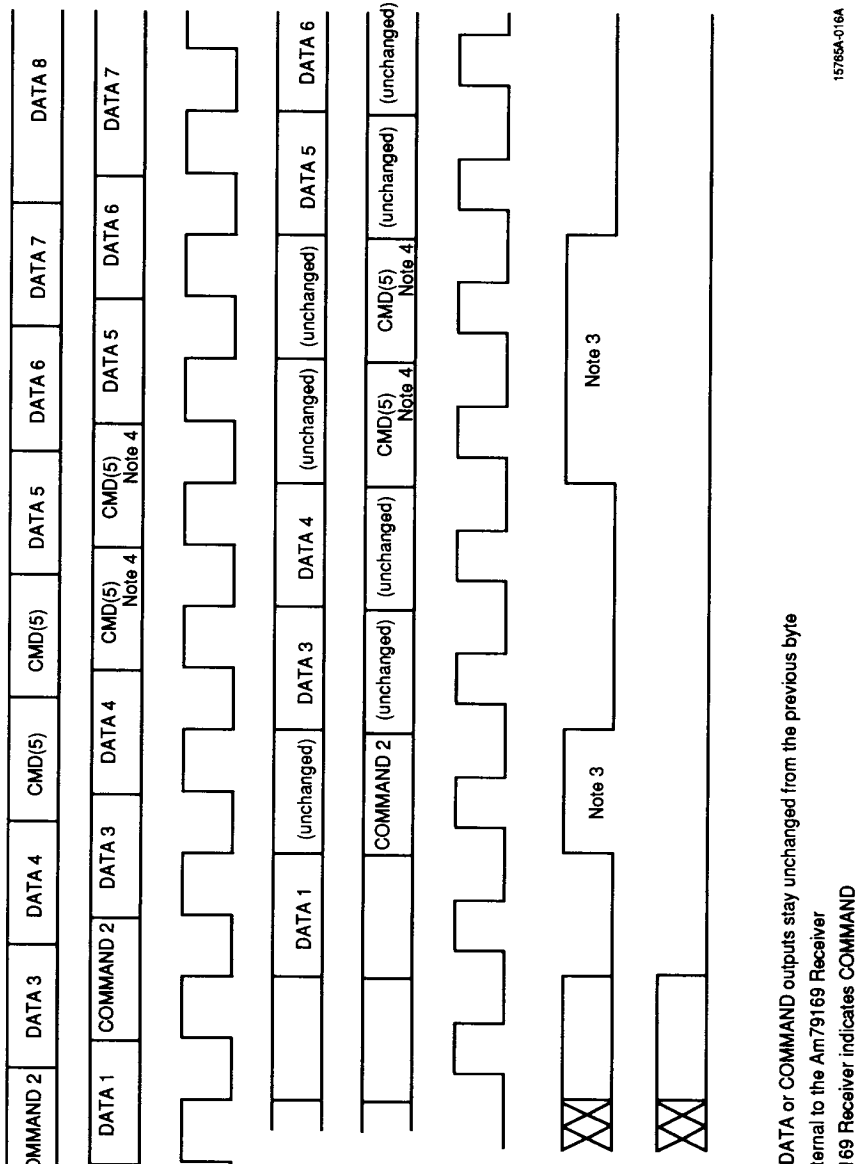
Note 6: The Receiver indicates subsequent CMD(5) after Re-Align is completed

Note 7: The Receiver will stretch CLKO and STRBO (may stretch either the HIGH or LOW portion) and align to the new byte boundary.

Note 8: In 10 bit mode CMD(1) or CMD(3) is output depending upon Running Disparity.
In 8 bit mode CMD(5) or CMD(13) is output. See Table 1.

Note 9: Misaligned data byte.

## SWITCHING WAVEFORMS
### Am79169 Receiver (Normal Receive)
### RX/RY or RLOOP Serial Inputs




**Notes:**

(unchanged) = the DATA or COMMAND outputs stay unchanged from the previous byte

Note 2: Register internal to the Am79169 Receiver

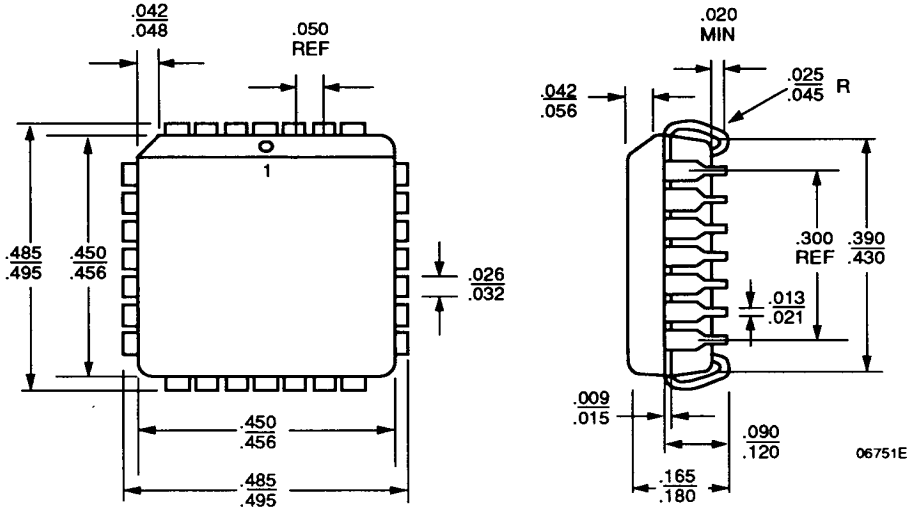
Note 3: The Am79169 Receiver indicates COMMAND

Note 4: The CMD(5) could be transmitted explicitly as COMMANDS or implicitly due to lack of STRBI at the Transmitter; for 10-bit mode it would be CMD(1). For the Receiver, if the Running Disparity is –1 a CMD(13) would be output CMD(13); if the Running Disparity is +1 a CMD(5) would be output. For 10-bit mode it would be CMD(3) or CMD(1) respectively.

## PHYSICAL DIMENSIONS*

### PL 028

### 28-Pin Plastic Leaded Chip Carrier




* For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.

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