1.1 Scope.

This specification covers the detail requirements for a hybrid, 12-bit analog-to-digital converter including quad sample-and-hold, multiplexer, reference, timing circuitry and FIFO memory.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD1334TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-40A.

1.3 Absolute Maximum Ratings.

Positive Analog Supply Voltage to Power/Signal Ground . . . . . +18 V
Negative Analog Supply Voltage to Power/Signal Ground . . . . . −18 V
Digital Supply Voltage to Digital Ground . . . . . +7 V
Power/Signal Ground to Digital Ground . . . . . −0.3 V to +0.3 V
Analog Input to Power/Signal Ground . . . . . $-V_S$ to $+V_S$
Digital Input to Digital Ground . . . . . −0.3 V to V_{DD} +0.3 V
Analog Output Short Circuit Duration . . . . . Indefinite
Digital Output Short Circuit Duration . . . . . 1 Output for 1 sec
Junction Temperature . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 8°C/W
θ_{JA} = 25°C/W

AD1334—SPECIFICATIONS

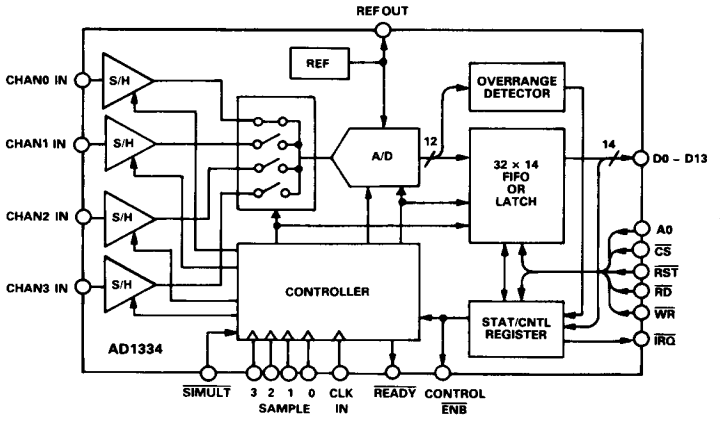
Table 1.

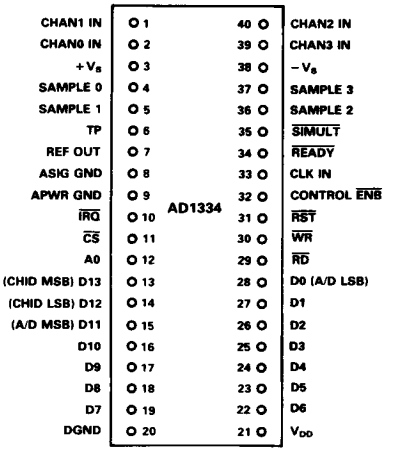
Test	Symbol	Device	Design Limit @+25°C	Sub Group 1	Sub Group 2, 3	Sub Group 7	Test Condition[1, 2]	Units
SAMPLE-AND-HOLD								
Acquisition Time to 0.01%	SH_{TACQ}	−1	7.5					μs max
Droop Rate	SH_{DRP}	−1	1					mV/ms max
Droop Rate, over Temperature	SH_{TCDRP}	−1	Doubles					/10°C
Aperture Delay	SH_{AD}	−1	15				Note 3	ns max
Effective Aperture Delay	SH_{EAD}	−1	−700				Note 4	ns min
		−1	−850					ns max
S/H, MUX & A/D CONVERTER								
Input Impedance	AD_{ZIN}	−1	2					kΩ min
Input Voltage Range	AD_{VIN}	−1	±5					V
CLK IN Frequency	f_{CLK}	−1	1.0					MHz min
				2.5	2.5			MHz max
CLK Duty Cycle	AD_{DC}	−1	45					% min
			55					% max
Sampling Rate Per Channel								
Simultaneous Mode								
($\overline{SIMULT}$ = LOW)								
1 Channel	f_{SS1}	−1	67					kHz max
2 Channels	f_{SS2}	−1	46					kHz max
3 Channels	f_{SS3}	−1	35					kHz max
4 Channels	f_{SS4}	−1		28	28			kHz max
Independent Mode								
($\overline{SIMULT}$ = HIGH)								
1 Channel	f_{SI1}	−1	67					kHz max
2 Channels	f_{SI2}	−1	67					kHz max
3 Channels	f_{SI3}	−1	44					kHz max
4 Channels	f_{SI4}	−1	33					kHz max
Resolution	AD_{RES}	−1		12	12			Bits
Integral Nonlinearity	AD_{INL}	−1		±1	±1 1/2			LSB max
Differential Nonlinearity	AD_{DNL}	−1		±1	±2			LSB max
−Full-Scale Error	AD_{FSE-}	−1		±4	±13			LSB max
+Full-Scale Error	AD_{FSE+}	−1		±4	±13			LSB max
−Full-Scale PSRR	PSRR−	−1		±1.5	±1.5			LSB/V max
+Full-Scale PSRR	PSRR+	−1		±1.5	±1.5			LSB/V max
Signal-to-Noise Ratio[5]	SNR	−1				70	f_{IN} = 13.6 kHz	dB min
Total Harmonic Distortion[5]	THD	−1				−76	f_{IN} = 13.6 kHz	dB max
Intermodulation Distortion	IMD	−1				−76	f_{IN} = 13.1 kHz and 13.6 kHz	dB max
Channel-to-Channel Isolation[6]	CCI_L	−1						
$\overline{SIMULT}$ = LOW						70	f_{IN} = 8.0 kHz	dB min
REFERENCE								
Reference Voltage	V_{REF}	−1				−5.05	I_{REF} = 1 mA	V min
						−4.95	I_{REF} = 1 mA	V max
Reference Current	I_{REF}	−1		±1				mA min
DIGITAL INPUTS & OUTPUTS								
Input Voltage, Logic Low	V_{IL}	−1		0.8	0.8			V max
Input Voltage, Logic High	V_{IH}	−1		2.0	2.25			V min
Input Current	I_I	−1		±250	±250			μA max
Output Voltage, Logic Low	V_{OL1}	−1		0.4			I_{OL} = 4 mA	V max
	V_{OL2}	−1			0.4		I_{OL} = 3.2 mA	V max
Output Voltage, Logic High	V_{OH1}	−1		2.4			I_{OH} = −4 mA	V min
	V_{OH2}	−1			2.4		I_{OH} = −3.2 mA	V min
High Impedance Leak Current, D0–D13	I_{OZ}	−1		±250	±250			μA max
$\overline{IRQ}$ Off-State Leakage	I_{OZ}	−1		±10	±20			μA max
$\overline{RST}$ Pulse Width	t_{RPW}	−1	10					ns min

Test	Symbol	Device	Design Limit @+25°C	Sub Group 1	Sub Group 2, 3	Sub Group 7	Test Condition[1, 2]	Units
DIGITAL INPUTS & OUTPUTS (Cont.)								
FIFO Fall-Thru Time	t_{FT}	−1	800					ns max
$\overline{IRQ}$ LOW to D0–D13 Valid	t_{DVAL}	−1	0				Note 7	ns max
POWER SUPPLY								
+ Analog Supply	$+V_S$	−1	+11.4					V min
			+15.75					V max
− Analog Supply	$-V_S$	−1	−11.4					V max
			−15.75					V min
Digital Supply	V_{DD}	−1	+4.75					V min
			+5.25					V max
+ Analog Supply Current	I_{S+}	−1				60		mA max
− Analog Supply Current	I_{S-}	−1				50		mA max
Logic Supply Current	I_{DD}	−1				15		mA max
Power Consumption	P_{D1}	−1				1.2	V_S = ±12 V	W max
	P_{D2}	−1				1.5	V_S = ±15 V	W max
READ CYCLE							Note 8	
Read Cycle Time	t_{RC}	−1	25				C_{OUT} = 30 pF	ns min
			35				C_{OUT} = 100 pF	ns min
Data Access Time	t_A	−1	15				C_{OUT} = 30 pF	ns max
			25				C_{OUT} = 100 pF	ns max
				35	35		C_{OUT} = 150 pF	ns max
Out Low Impedance Time	t_{LZ}	−1	2					ns min
Out High Impedance Time	t_{HZ}	−1	15				C_{OUT} = 30 pF	ns max
			25				C_{OUT} = 100 pF	ns max
Output Hold Time	t_{OH}	−1	2					ns min
A0 Valid to $\overline{RD}$ Low	t_{A0RD}	−1	3					ns min
$\overline{RD}$ High to A0 Invalid	t_{RDA0}	−1	3					ns min
A0 Valid to $\overline{CS}$ Low	t_{A0CS}	−1	3					ns min
$\overline{CS}$ High to A0 Invalid	t_{CSA0}	−1	3					ns min
WRITE CYCLE								
Write Cycle Time	t_{WC}	−1	15					ns min
Write Pulse Width	t_{WP}	−1	5					ns min
Data Setup Time	t_{SU}	−1	2					ns min
Input Hold Time	t_{IH}	−1	4					ns min
A0 Valid to $\overline{WR}$ Low	t_{A0WR}	−1	3					ns min
$\overline{WR}$ High to A0 Invalid	t_{WRA0}	−1	3					ns min
A0 Valid to $\overline{CS}$ Low	t_{A0CS}	−1	3					ns min
$\overline{CS}$ High to A0 Invalid	t_{CSA0}	−1	3					ns min

NOTES
[1]Specifications are per channel in 4-channel simultaneous mode SAMPLE 0–3 connected together and $\overline{SIMULT}$ = LOW, at F_S = 28 kHz, and with SAMPLE 0–3 having an 88% duty cycle unless noted.
[2]All specifications with $+V_S$ = 15 V, $-V_S$ = −15 V, V_{DD} = +5 V, f_{CLK} = 2.5 MHz, CONTROL $\overline{ENB}$ = Logic Low unless otherwise noted.
[3]Aperture delay is the time delay from the SAMPLE input to S/H switch opening and is a measure of digital time delay through the S/H.
[4]Effective aperture delay is the difference between analog and digital time delays described in (2) and (3).
[5]THD of harmonics 2–7 of the fundamental. SNR of fundamental less harmonics 2–7.
[6]Isolation of anyone channel from remaining three channels which have near maximum amplitude ac signals at their inputs.
[7]$\overline{RD}$, $\overline{CS}$, A0 = LOW; $\overline{WR}$, $\overline{RST}$ = HIGH.
[8]C_{OUT} = 30 pF or 100 pF except as noted.

3.2.1 Functional Block Diagram and Terminal Assignments.





3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life/Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in per MIL-STD-883 Method 1015 test condition (B).