



T-46-07-12

843A • 843B

74FCT843A • 74FCT843B

9-Bit Transparent Latch

General Description

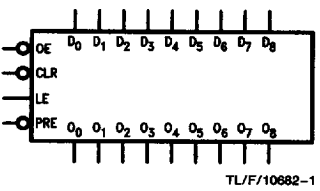
The 74FCT843A/B bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths. FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance. FACT FCTA features GTOT™ output control and undershoot corrector in addition to a split ground bus for superior performance. FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

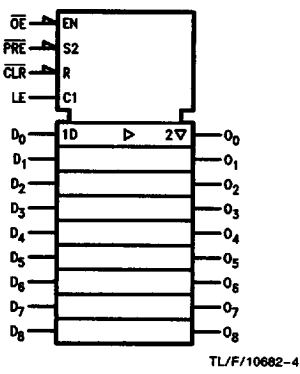
- NSC 74FCT843A/B is pin and functionally equivalent to IDT 74FCT843A/B
- High Speed parallel latches
- Buffered common latch enable, clear and preset inputs
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA
- CMOS power levels
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

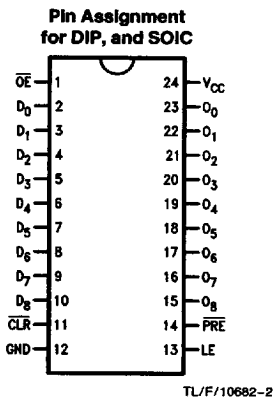
Logic Symbols



Pin Names	Description
D ₀ -D ₈	Data Inputs
Q ₀ -Q ₈	Data Outputs
OE	Output Enable
LE	Latch Enable
CLR	Clear
PRE	Preset



Connection Diagram



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Functional Description

The FCT843A/B consists of nine D-type latches with TRI-STATE® outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

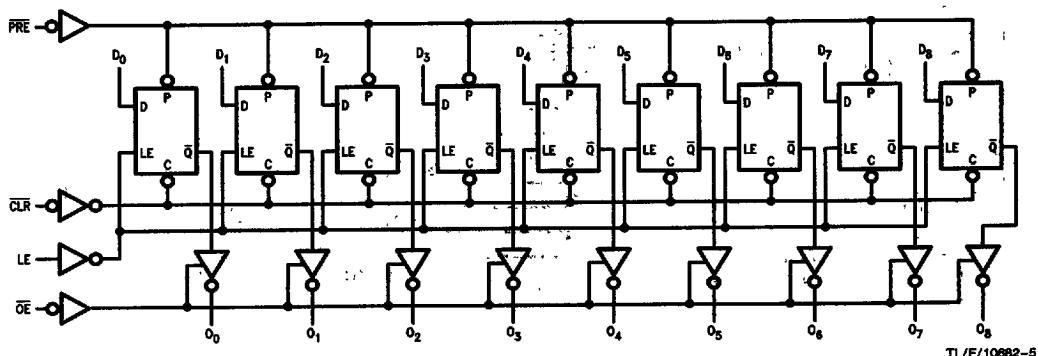
In addition to the LE and OE pins, the FCT843A/B has a Clear (CLR) pin and a Preset (PRE) pin. These pins are ideal for parity bus interfacing in high performance systems. When CLR is LOW, the outputs are LOW if OE is LOW. When CLR is HIGH, data can be entered into the latch. When PRE is LOW, the outputs are HIGH if OE is LOW. Preset overrides Clear.

Function Tables

Inputs					Internal	Outputs	Function
CLR	PRE	OE	LE	D	Q	O	
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Clear/High Z
H	L	H	L	X	H	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/10682-5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
74FCTA/B $-0.5V$ to $+7.0V$

Temperature under Bias (T_{BIAS})
74FCTA/B $-55^{\circ}C$ to $+125^{\circ}C$

Storage Temperature (T_{STG})
74FCTA/B $-55^{\circ}C$ to $+125^{\circ}C$

DC Output Current (I_{OUT}) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
74FCTA/B $4.75V$ to $5.25V$

Input Voltage $0V$ to V_{CC}

Output Voltage $0V$ to V_{CC}

Operating Temperature (T_A)
74FCTA/B $-0^{\circ}C$ to $+70^{\circ}C$

Junction Temperature (T_J)
PDIP $140^{\circ}C$

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from $-40^{\circ}C$ to $+125^{\circ}C$.

DC Characteristics for 'FCTA/B Family Devices

Typical values are at $V_{CC} = 5.0V$, $25^{\circ}C$ ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	74FCTA/B			Units	Conditions	
		Min	Typ	Max			
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	$V_{CC} = \text{Max}$	$V_I = V_{CC}$ $V_I = 2.7V$ (Note 2)
I_{IL}	Input Low Current			-5.0 -5.0	μA	$V_{CC} = \text{Max}$	$V_I = 0.5V$ (Note 2) $V_I = \text{GND}$
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 -10.0 -10.0	μA	$V_{CC} = \text{Max}$	$V_O = V_{CC}$ $V_O = 2.7V$ (Note 2) $V_O = 0.5V$ (Note 2) $V_O = \text{GND}$
V_{IK}	Clamp Diode Voltage	-0.7	-1.2		V	$V_{CC} = \text{Min}$; $I_{IN} = -18 \text{ mA}$	
I_{OS}	Short Circuit Current	-75	-120		mA	$V_{CC} = \text{Max}$ (Note 1); $V_O = \text{GND}$	
V_{OH}	Minimum Low Level Output Voltage	2.8 V_{HC} 2.4	3.0 V_{CC} 4.3		V	$V_{CC} = 3V$; $V_{IN} = 0.2V$ or V_{HC} ; $I_{OH} = -32 \mu A$ $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300 \mu A$ $I_{OL} = -24 \text{ mA}$
V_{OL}	Maximum Low Level Output Voltage		GND 0.3	0.2 0.5	V	$V_{CC} = 3V$; $V_{IN} = 0.2V$ or V_{HC} ; $I_{OH} = 300 \mu A$ $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300 \mu A$ $I_{OL} = 48 \text{ mA}$
I_{CC}	Maximum Quiescent Supply Current		0.2	1.5	mA	$V_{CC} = \text{Max}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq 0.2V$ $f_I = 0$	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	$V_{CC} = \text{Max}$ $V_{IN} = 3.4V$ (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.50	mA/MHz	$V_{CC} = \text{Max}$ Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$

DC Characteristics for 'FCTA/B Family Devices (Continued)

Typical values are at $V_{CC} = 5.0V$, $25^{\circ}C$ ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	74FCTA/B			Units	Conditions	
		Min	Typ	Max			
I_C	Total Power Supply Current (Note 6)			7.5	mA	$V_{CC} = \text{Max}$ Outputs Open $LE = V_{CC}$ $OE = GND$ $f_i = 10 \text{ MHz}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				8.0			$V_{IN} = 3.4V$ $V_{IN} = GND$
				11.0		(Note 5) $V_{CC} = \text{Max}$ Outputs Open $OE = GND$ $LE = V_{CC}$ $f_i = 2.5 \text{ MHz}$ Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				14.5			$V_{IN} = 3.4V$ $V_{IN} = GND$

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (I_{CP}/2 + f_i N_i)$

$I_{CC} = \text{Quiescent Current}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$f_i = \text{Input Frequency}$

$N_i = \text{Number of Inputs at } f_i$

All currents are in milliamperes and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	Test Conditions	74FCTA		74FCTB		Units	Fig. No.
			$T_A, V_{CC} = \text{Com}$		$T_A, V_{CC} = \text{Com}$			
			Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n (LE = High)	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$	9.0		6.5		ns	2-9
		$C_L = 300 \text{ pF}$ (Note 1) $R_L = 500\Omega$	13.0		13.0		ns	2-9
t_{SU}	Data to LE Setup Time	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$	2.5		2.5		ns	2-10
t_H	Data to LE Hold Time	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$	2.5		2.5		ns	2-10
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$	12.0		8.0		ns	2-9
		$C_L = 300 \text{ pF}$ (Note 1) $R_L = 500\Omega$	16.0		15.5		ns	2-9

AC Electrical Characteristics: See Section 2 for Waveforms (Continued)

Symbol	Parameter	Test Conditions	74FCTA		74FCTB		Units	Fig. No.
			T _A , V _{CC} = Com		T _A , V _{CC} = Com			
			Min	Max	Min	Max		
t _{PLH}	Propagation Delay PRE to O _n	C _L = 50 pF R _L = 500Ω	12.0		8.0		ns	2-9
t _{REC}	Recovery Time PRE to O _n		14.0		10.0		ns	
t _{PHL}	Propagation Delay CLR to O _n		13.0		10.0		ns	2-9
t _{REC}	Recovery Time CLR to O _n		14.0		10.0		ns	
t _W	LE Pulse Width High (Note 1)	C _L = 50 pF R _L = 500Ω	4.0		4.0		ns	
t _W	PRE Pulse Width Low (Note 1)	C _L = 50 pF R _L = 500Ω	5.0		4.0		ns	
t _W	CLR Pulse Width Low (Note 1)	C _L = 50 pF R _L = 500Ω	4.0		4.0		ns	
t _{PZH} t _{PZL}	Output Enable Time (OE to O _n)	C _L = 50 pF R _L = 500Ω	11.5		8.0		ns	2-11
		C _L = 300 pF (Note 1) R _L = 500Ω	23.0		14.0		ns	
t _{PHZ} t _{PLZ}	Output Disable Time (OE to O _n)	C _L = 5 pF (Note 1) R _L = 500Ω	7.0		6.0		ns	
		C _L = 50 pF R _L = 500Ω	8.0		7.0		ns	

Note 1: These parameters are guaranteed but not tested.

Capacitance $T_A = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$

Symbol	Parameter (Note 1)	Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	8	12	pF

Note 1: This parameter is measured at characterization but not tested.