Data Sheet

AT&T Microelectronics

41LK, 41LL, and 41LM Dual Differential Line Transceivers

Features

Driver Features:

- Two line drivers per package
- Logic converts TTL input logic levels to differential, pseudo-ECL output logic levels
- No line loading when Vcc = 0 V
- High output drive for 50 Ω lines
- 200 mA short-circuit current (typical)
- 4.5 ns maximum propagation delay
- <0.2 ns output skew (typical)

Receiver Features:

- Two line receivers per package
- High input impedance ≈ 8 kΩ*
- Logic which converts differential input logic levels to TTL output logic levels
- 7 ns maximum propagation delay
- <0.20 V input sensitivity (typical)
- −1.2 to +7.2 V common-mode range

Common Device Features:

- Common enable for each driver pair and receiver pair
- 0 °C to 85 °C ambient operating temperature (See Section 9.)
- Single 5 V supply
- 200 Mbits/s maximum data rates when used with the 41L*x* and 41M*x* devices
- Meets ESDI standards

Description

The 41LK, 41LL, and 41LM devices are dual differential transceiver circuits that transmit and receive digital data over balanced transmission lines and are compatible with 41 Series drivers and receivers. The dual drivers translate input TTL logic levels to differential, pseudo-ECL output levels. The dual receivers convert differential input logic levels to TTL output levels. Each driver pair and receiver pair has its own common enable control allowing serial data and a control clock to be transmitted and received on a single integrated circuit.

The 41LK transceiver requires the customer to supply termination resistors on the circuit board. The 41LL transceiver has an internal 220 Ω termination resistor connected to ground on each driver output and is equivalent to the 8923A device. The 41LM transceiver has an internal resistor termination for both the driver outputs (220 Ω) and receiver inputs (110 Ω), eliminating the need for external resistors on the circuit board when used with 100 Ω impedance, twisted-pair (or flat) cable.

The packaging options that are available for the dual differential transceivers include a 16-pin DIP (41LK, 41LL, 41LM), a 16-pin J-lead SOJ (1041LK, 1041LL, 1041LM), a 16-pin gull-wing SOIC (1141LK, 1141LL, 1141LM), and a 16-pin narrow-body gull-wing SOIC (1241LK, 1241LL, 1241LM).

* Except 41LM which has built-in resistors

Pin Information

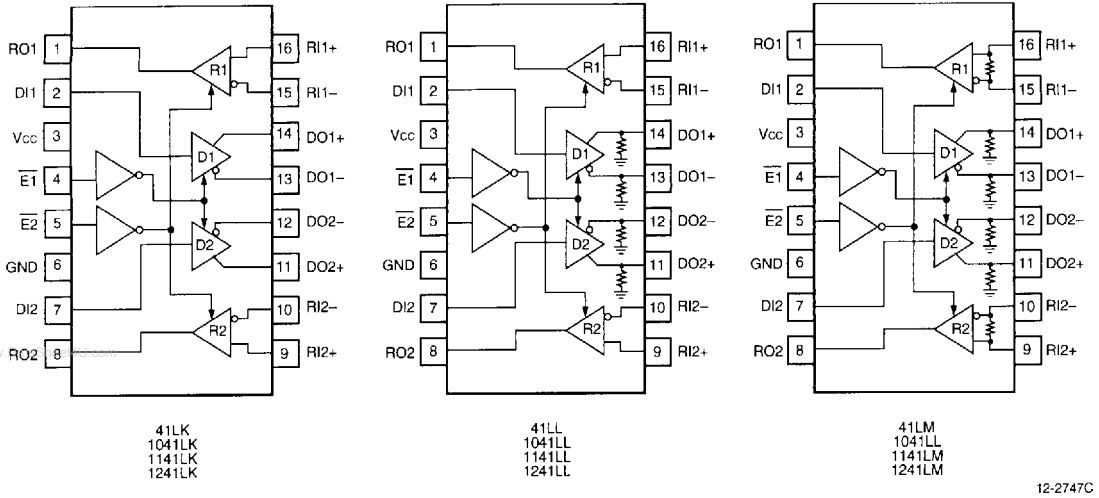

Figure 5-1. 41LK, 41LL, and 41LM Logic Diagrams

Enable Truth Table

$\overline{E1}$	$\overline{E2}$	DO1	DO2	RO1	RO2
0	0	Active	Active	Active	Active
1	0	Disabled	Disabled	Active	Active
0	1	Active	Active	Disabled	Disabled
1	1	Disabled	Disabled	Disabled	Disabled

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	—	7.0	V
Ambient Operating Temperature	T_A	0	85	°C
Storage Temperature	T_{stg}	−40	125	°C

Handling Precautions

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

AT&T employs a human-body model (HBM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. 41 Series receiver differential inputs are not equipped with ESD protection. The standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is used. The HBM ESD threshold voltages presented here were obtained by using this circuit.

HBM ESD Threshold Voltage	
Device	**Rating**
41 Series Receiver	
Differential Inputs (LK, LL)	>100 V
(LM)	>750 V
All other pins	>1000 V

Electrical Characteristics

Table 5-1. 41LK, 41LL, and 41LM Power Supply Current Characteristics

T_A = 0 °C to 85 °C, V_{CC} = 5 V ± 0.5 V.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current, V_{CC} = 5.5 V:					
41LK					
All Outputs Disabled	I_{CC}	—	45	70	mA
All Outputs Enabled	I_{CC}	—	30	45	mA
41LL and 41LM					
All Outputs Disabled	I_{CC}	—	70	100	mA
All Outputs Enabled	I_{CC}	—	85	125	mA

Electrical Characteristics (continued)

Table 5-2. 41LK, 41LL, and 41LM Voltage and Current Characteristics (Driver)

T_A = 0 °C to 85 °C.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages, V_{CC} = 4.5 V:					
Low, I_{OL} = –8.0 mA*	V_{OL}	—	3.0	V_{OH} – 0.8†	V
High, I_{OH} = –40.0 mA*	V_{OH}	3.0	4.0	—	V
High Z, I_{OH} = –1.0 mA, V_{CC} = 4.75 V	V_{OZ}	—	2.0	V_{OL} – 0.02	V
Input Voltages:					
Low, V_{CC} = 5.5 V	V_{IL}‡	—	—	0.7	V
High, V_{CC} = 4.5 V	V_{IH}‡	2.0	—	—	V
Clamp, V_{CC} = 4.5 V, I_{IN} = –5.0 mA	V_{IK}	—	—	–1.5	V
Short-circuit Output Current, V_{CC} = 5.5 V	I_{OS}§	–100	–200	–300	mA
Input Currents, V_{CC} = 5.5 V:					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	–400	µA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20	µA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	µA
Output Resistors (41LL, 41LM)	R_O	—	220	—	Ω

* Typical value of the output current for the 41LK, 41LL, and 41LM when terminated per Figure 6-5
† V_{OL} must be a minimum of 0 8 V less than its complementary output
‡ The input levels provide zero noise immunity and should be tested only in a static, noise-free environment.
§ Test must be performed one lead at a time to prevent damage to the device.

Table 5-3. 41LK, 41LL, and 41LM Voltage and Current Characteristics (Receiver)

T_A = 0 °C to 85 °C.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage, V_{CC} = 4.5 V:					
Low, I_{OL} = 8.0 mA	V_{OL}*	—	—	0.5	V
High, I_{OH} = –400 µA	V_{OH}*	2.5	—	—	V
Enable Input Voltages:					
Low, V_{CC} = 5.5 V	V_{IL}*	—	—	0.7	V
High, V_{CC} = 4.5 V	V_{IH}*	2.0	—	—	V
Minimum Differential Input Voltage, $V_{IH} – V_{IL}$:†					
–0.80 V < V_{IH} < 7.2 V, –1.2 V < V_{IL} < 6.8 V	V_{TH}*	—	0.1	0.20	V
Output Currents, V_{CC} = 5.5 V:					
Off-state (high Z), V_O = 0.4 V	I_{OZL}	—	—	–20	µA
Off-state (high Z), V_O = 2.4 V	I_{OZH}	—	—	20	µA
Short Circuit	I_{OS}‡	–25.0	—	–100	mA
Enable Input Currents, V_{CC} = 5.5 V:					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	–400	µA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20	µA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	µA
Differential Input Currents (41LK, 41LL)					
Low, V_{IN} = –1.2 V	I_{IL}	—	—	–1.0	mA
High, V_{IN} = 7.2 V	I_{IH}	—	—	1.0	mA
Differential Input Impedance (41LM) Connected Between RI^+ and RI^-	RI	—	110	—	Ω

* The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment
† Outputs of unused receivers assume a logic 1 level when the inputs are left open.
‡ Test must be performed one lead at a time to prevent damage to the device

Timing Characteristics

Table 5-4. 41LK, 41LL, and 41LM Timing Characteristics (Driver) (See Figures 6-1 and 6-2.)

Propagation-delay test circuit connected to output (see Figure 6-6).

T_A = 25 °C, V_{CC} = 5 V.

Symbol	Parameter	Typ	Max	Unit
	Propagation Delay:			
t_{P1}	Input High to Output	3.0	4.5	ns
t_{P2}	Input Low to Output	3.0	4.5	ns
	Disable Time:			
t_{PHZ}	High to High Impedance	10	15	ns
t_{PLZ}	Low to High Impedance	10	15	ns
	Enable Time:			
t_{PZH}	High Impedance to High	10	15	ns
t_{PZL}	High Impedance to Low	10	15	ns
t_{skew}	Output Skew, $\|t_{P1} - t_{P2}\|$	0.2	0.5	ns
Δt_{skew}	Difference Between Drivers	0.3	—	ns

Table 5-5. 41LK, 41LL, and 41LM Timing Characteristics (Receiver) (See Figures 6-3 and 6-4.)

Propagation-delay test circuit connected to output (see Figure 6-8).

T_A = 25 °C, V_{CC} = 5 V.

Symbol	Parameter	Typ	Max	Unit
	Propagation Delay:			
t_{PLH}	Input to Output High	3.5	7.0	ns
t_{PHL}	Input to Output Low	3.5	7.0	ns
	Disable Time, C_L = 5 pF:			
t_{PHZ}	High to High Impedance	10	15	ns
t_{PLZ}	Low to High Impedance	10	15	ns
	Enable Time, C_L = 5 pF:			
t_{PZH}	High Impedance to High	10	15	ns
t_{PZL}	High Impedance to Low	10	15	ns