DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD23C32020A

32M-BIT MASK-PROGRAMMABLE ROM
2M-WORD BY 16-BIT

Description

The μPD23C32020A is a 33,554,432 bits (2,097,152 words by 16 bits) mask-programmable ROM.

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C32020A is packed in 42-pin plastic DIP.

Features

- Word organization: 2,097,152 words by 16 bits
- Access time: 120 ns (MAX.)
- Low current consumption
  - Active ····· 70 mA (MAX.)
  - Standby ····· 100 μA (MAX.) (CMOS level input)

Ordering Information

Part Number	Package
μPD23C32020ACZ-×××	42-pin Plastic DIP (600 mil)

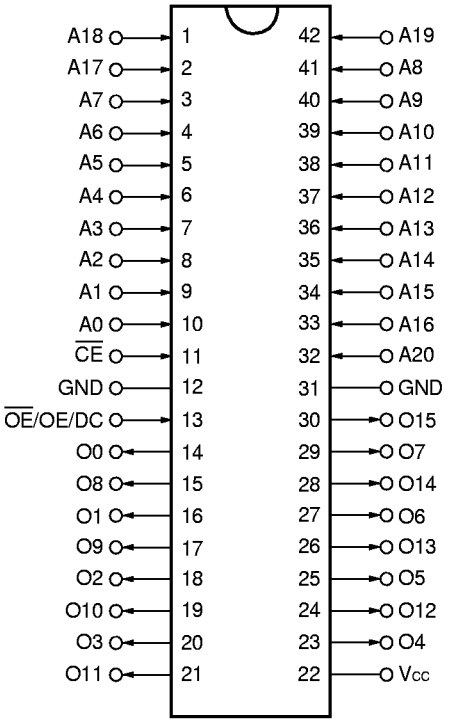
(×××: ROM code suffix No.)

Document No. M12073EJ1V0DS00 (1st edition)
Date Published November 1996 N
Printed in Japan

Pin Configuration (Marking Side)

42-pin Plastic DIP (600 mil)

μPD23C32020ACZ

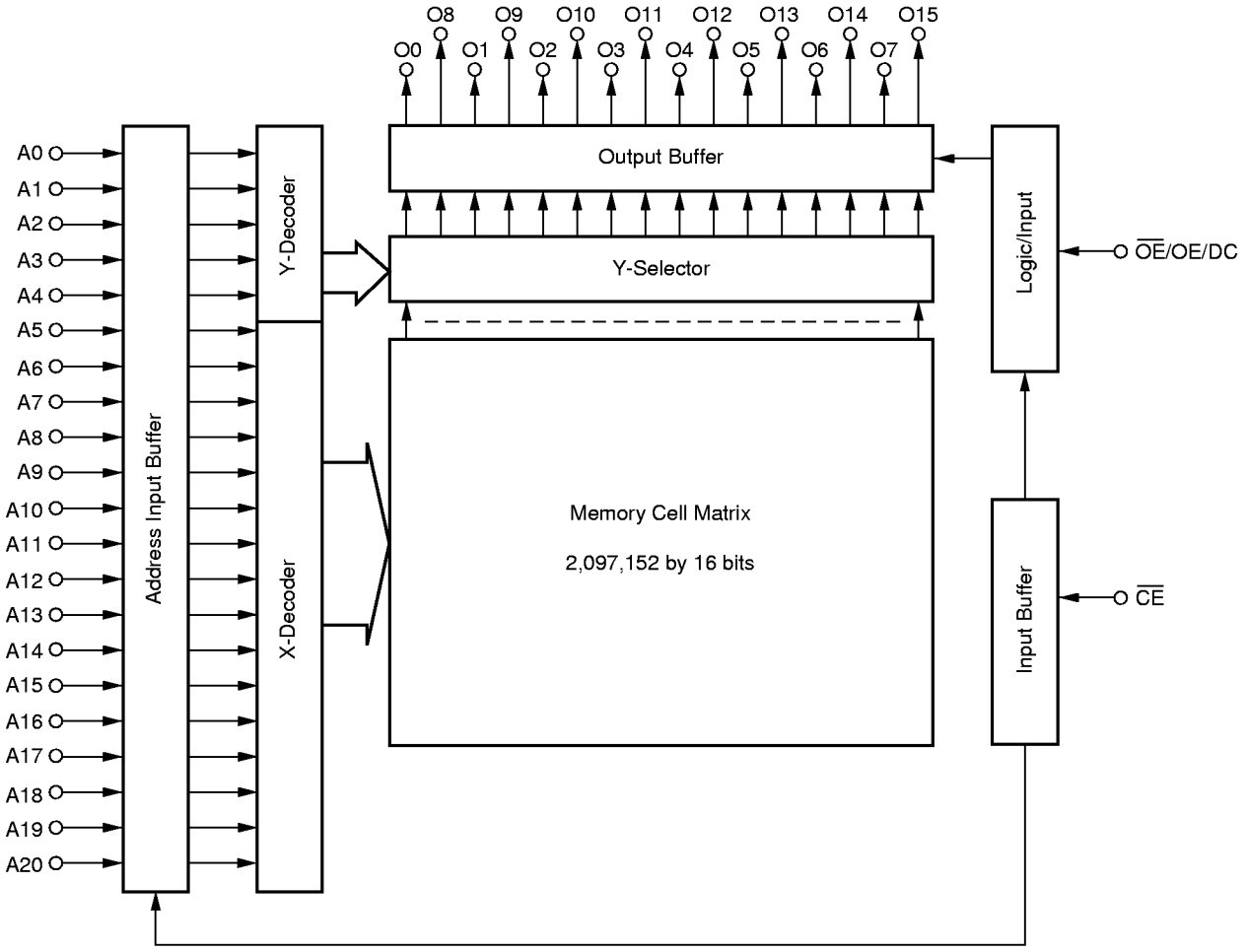


A0 - A20	:	Address inputs
O0 - O15	:	Data outputs
$\overline{CE}$	:	Chip enable
$\overline{OE}$/OE	:	Output enable
V_{CC}	:	Supply voltage
GND	:	Ground
DC	:	Don't care

Input/Output Pin Functions

Pin name	Input/ Output	Function
A0 to A20 (Address input)	Input	Address bus.
O0 - O15 (Data output)	Output	Output data bus.
$\overline{CE}$ (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. High level ····· High impedance Low level ····· Data out
$\overline{OE}$/OE/DC (Output Enable/Don't care)		Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	—	Supply voltage
GND	—	Ground

Block Diagram



Mask Option

The active levels of output enable pin ($\overline{OE}$/OE/DC) are mask programmable and optional, and can be selected from among "0" "1" "×" shown in the table below.

Option	$\overline{OE}$/OE/DC	OE active level
0	$\overline{OE}$	L
1	OE	H
×	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option: 0)

$\overline{CE}$	$\overline{OE}$	Mode	Output state
L	L	Active	Data out
	H		High impedance
H	H or L	Standby	High impedance

Operation mode (Option: 1)

$\overline{CE}$	OE	Mode	Output state
L	L	Active	High impedance
	H		Data out
H	H or L	Standby	High impedance

Operation mode (Option: ×)

$\overline{CE}$	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High impedance

Remark L: Low level input
H: High level input

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		–0.3 to +7.0	V
Input voltage	V_I		–0.3 to V_{CC} +0.3	V
Output voltage	V_O		–0.3 to V_{CC} +0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 5.0 V ± 10 %)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.2		V_{CC} +0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
High level output voltage	V_{OH1}	I_{OH} = –400 μA	2.4			V
	V_{OH2}	I_{OH} = –100 μA	V_{CC} –0.5			
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input leakage current	I_{LI}	V_I = 0 to V_{CC}	–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}, Chip deselected	–10		+10	μA
Power supply current	I_{CC1}	$\overline{CE}$ = V_{IL} (Active mode), I_O = 0 mA			70	mA
Standby current	I_{CC2}	$\overline{CE}$ = V_{IH} (Standby mode)			1.5	mA
	I_{CC3}	$\overline{CE}$ = V_{CC} –0.2 V (Standby mode)			100	μA

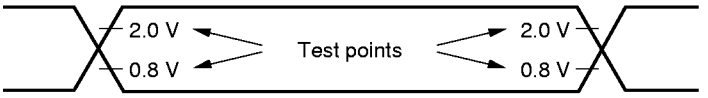
AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 5.0 V ±10 %)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Address access time	t_{ACC}				120	ns
Chip enable access time	t_{CE}				120	ns
Output enable access time	t_{OE}				50	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		25	ns

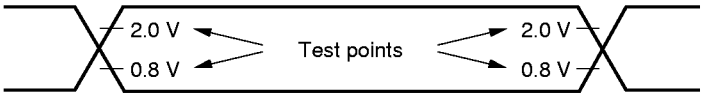
Remark t_{DF} is the time from inactivation of $\overline{CE}$ or $\overline{OE}$/OE to high-impedance state output.

AC Test Conditions

Input waveform (Rise/Fall time ≤ 5 ns)



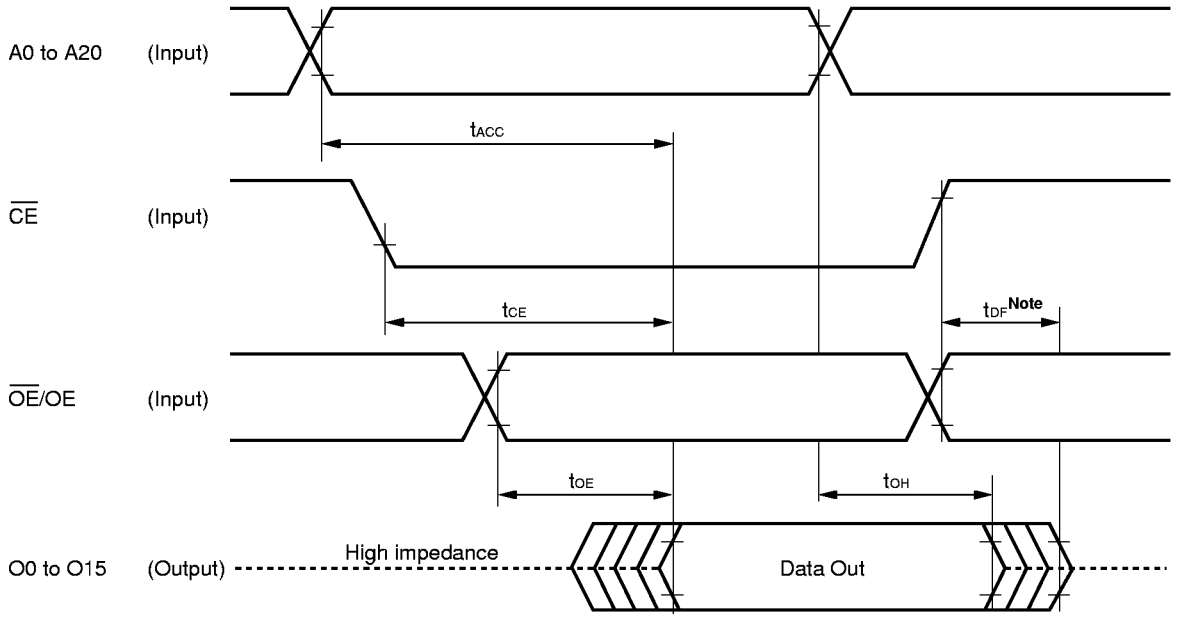
Output waveform



Output load

1TTL + 100 pF

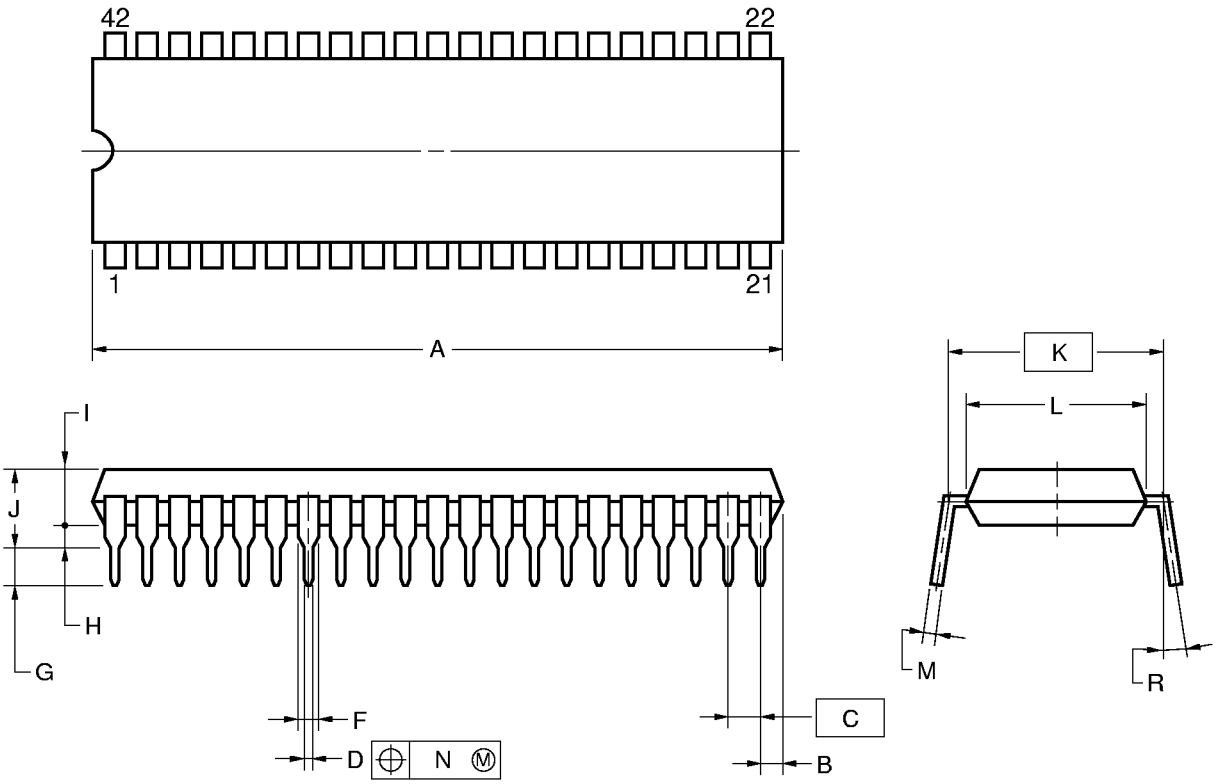
Read Cycle Timing Chart



Note t_{DF} is specified when the one of $\overline{CE}$, $\overline{OE}$ or OE is inactivated.

Package Drawing

42PIN PLASTIC DIP (600 mil)



NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	55.88 MAX.	2.200 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
R	0~15°	0~15°

P42C-100-600A,B-1

Recommended Soldering Conditions

The following conditions (see table below) must be met when soldering the μPD23C32020A.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Type of Through Hole Mount Device

μPD23C32020ACZ: 42-pin Plastic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.