NBSG86A

2.5V/3.3V SiGe Differential Smart Gate with Output Level Select

The NBSG86A is a multi–function differential Logic Gate which can be configured as an AND/NAND, OR/NOR, XOR/XNOR, or 2:1 MUX. This device is part of the GigaComm™ family of high performance Silicon Germanium products. The device is housed in a low profile 4x4 mm, 16–pin, flip–chip BGA package.

Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), CMOS, CML, or LVDS. The OLS input is used to program the peak–to–peak output amplitude between 0 and 800 mV in five discrete steps.

The NBSG86A employs input clamping circuitry so that under open input conditions the outputs of the device will remain stable.

- Maximum Input Clock Frequency > 8 GHz Typical
- 165 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- Selectable Swing PECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = –2.375 V to –3.465 V
- Digitally Selectable Output Level Select (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak–to–Peak Output)
- 50 Ω (to V_{TT}) Internal Input Termination Resistors

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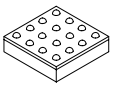


FCBGA–16
BA SUFFIX
CASE 489

MARKING DIAGRAM*

L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG86ABA	4x4 mm FCBGA–16	100 Units/Tray
NBSG86ABAR2	4x4 mm FCBGA–16	500/ Tape & Reel

Board	Description
SG86ABAEVB	NBSG86ABA Evaluation Board

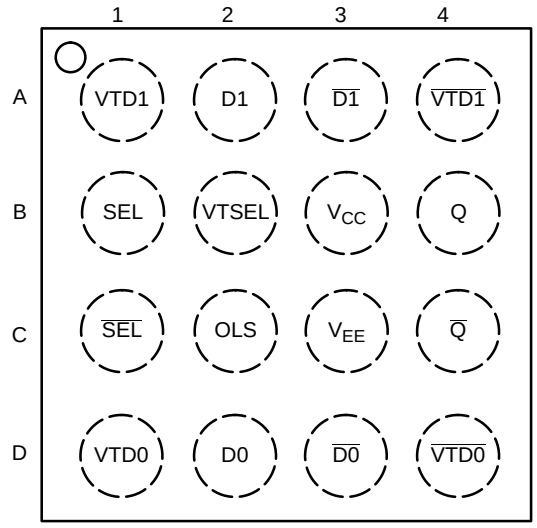


Figure 1. Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
D0*, D1*, $\overline{D0}$**, $\overline{D1}$**	Data Inputs
Q, $\overline{Q}$	Data Outputs
VTD0, $\overline{VTD0}$, VTD1, $\overline{VTD1}$	50 Ω Internal Input Termination Resistor
VTSEL	50 Ω Internal Input Termination Resistor Connected to SEL and $\overline{SEL}$
SEL, $\overline{SEL}$	Select Inputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
OLS	(Output Level Select) Input

* Pin will default low when left open.
** Pin will default to a slightly higher potential than D0/D1 when both are left open.

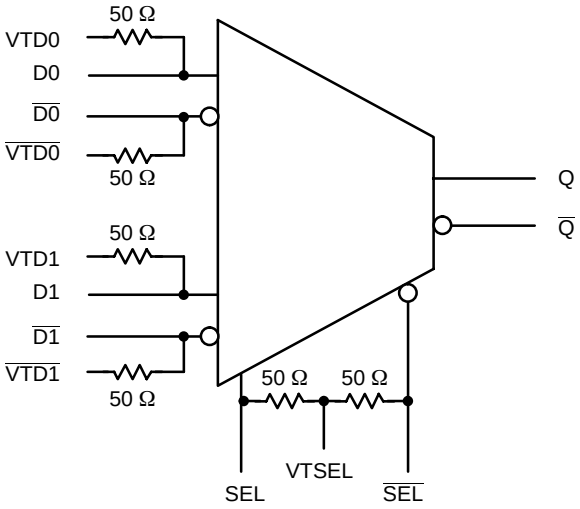


Figure 2. Logic Diagram

OUTPUT LEVEL SELECT (OLS)

OLS	Q/$\overline{Q}$ VPP	OLS Sensitivity
V_{CC}	800 mV	OLS – 75 mV
V_{CC} – 0.4 V	200 mV	OLS ± 150 mV
V_{CC} – 0.8 V	600 mV	OLS ± 100 mV
V_{CC} – 1.2 V	0	OLS ± 75 mV
V_{EE}*	400 mV	OLS + 100 mV
Float	600 mV	N/A

* When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, 2.0 kΩ resistor should be connected from OLS to V_{EE}.

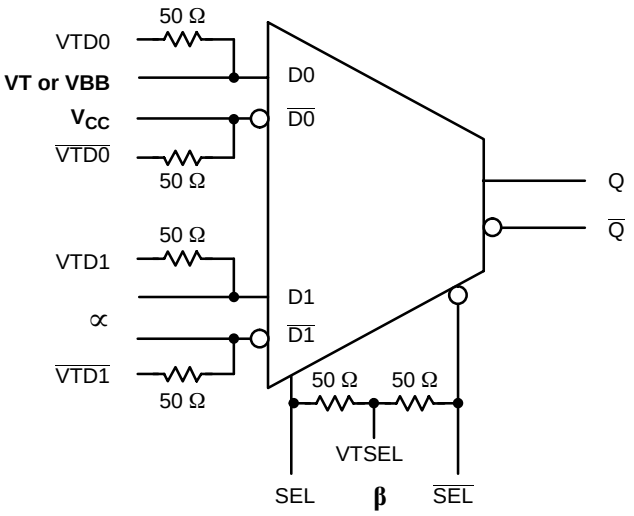
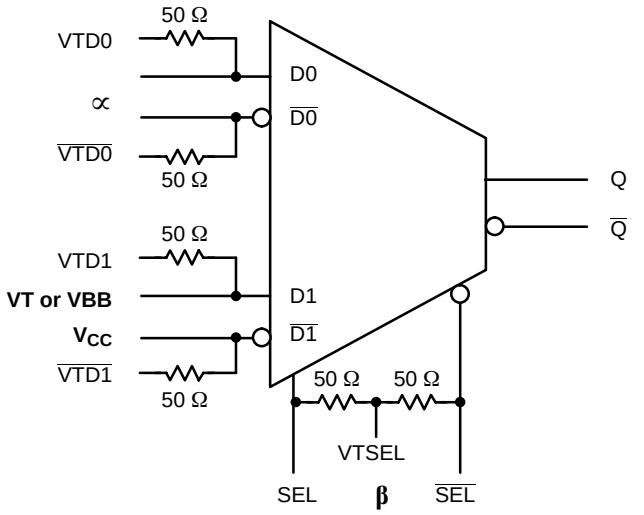


Figure 3. Configuration for AND/NAND Function

AND/NAND TRUTH TABLE**

	∝	β	∝ * β
D0	**D1**	**SEL**	**Q**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

** $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ are inverse of D0, D1, SEL unless specified otherwise.

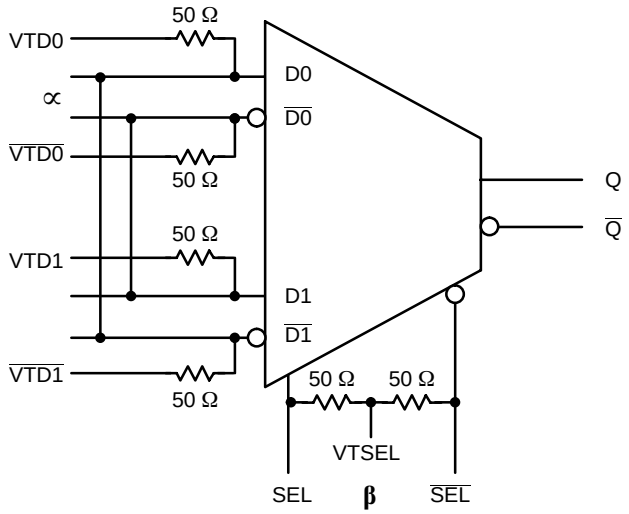


OR/NOR TRUTH TABLE**

∝		β	∝ or β
D0	**D1**	**SEL**	**Q**
0	1	0	0
0	1	1	1
1	1	0	1
1	1	1	1

** $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ are inverse of D0, D1, SEL unless specified otherwise.

Figure 4. Configuration for OR/NOR Function

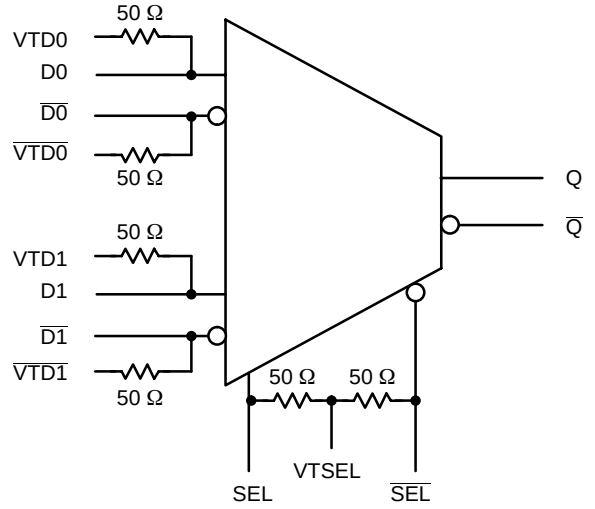


XOR/XNOR TRUTH TABLE**

∝		β	∝ XOR β
D0	**D1**	**SEL**	**Q**
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0

** $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ are inverse of D0, D1, SEL unless specified otherwise.

Figure 5. Configuration for XOR/XNOR Function



2:1 MUX TRUTH TABLE

SEL	Q
1	D1
0	D0

Figure 6. Configuration for 2:1 MUX Function

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD0, VTD1, VTSEL and $\overline{VTD0}$, $\overline{VTD1}$ to V_{CC}
LVDS	Connect VTD0, VTD1, $\overline{VTD0}$ and $\overline{VTD1}$ together. Leave VTSEL open.
AC–COUPLED	Bias VTD0, VTD1, VTSEL and $\overline{VTD0}$, $\overline{VTD1}$ Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistors		75 kΩ
Internal Input Pullup Resistor ($\overline{D}$)		37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1 KV > 50 V > 4 KV
Moisture Sensitivity (Note 1)	Oxygen Index: 28 to 34	Level 3
Flammability Rating		UL 94 V–0 @ 0.125 in
Transistor Count		364
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		–3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 –3.6	V V
V_{INPP} (IN–IN)	Differential Input Voltage Swing/Sensitivity	$V_{CC} - V_{EE} \ge$ 2.8 V $V_{CC} - V_{EE} <$ 2.8 V		2.8 $\lvert V_{CC} - V_{EE} \rvert$	V V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{out}	Output Current	Continuous Surge		25 50	mA mA
TA	Operating Temperature Range			–40 to +70	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) (Note 3)	0 LFPM 500 LFPM	16 FCBGA 16 FCBGA	108 86	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	2S2P (Note 3)	16 FCBGA	5	°C/W
T_{sol}	Wave Solder	< 15 Sec.		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

DC CHARACTERISTICS, INPUT WITH PECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 4)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	23	30	39	23	30	39	23	30	39	mA
V_{OH}	Output HIGH Voltage (Note 5)	1460	1510	1560	1490	1540	1590	1515	1565	1615	mV
V_{OL}	Output LOW Voltage (Note 5)										mV
	($OLS = V_{CC}$)	555	705	855	595	745	895	625	775	925	
	($OLS = V_{CC} – 0.4$ V)	1235	1295	1355	1270	1330	1390	1295	1355	1415	
	($OLS = V_{CC} – 0.8$ V, OLS = FLOAT)	775	895	1015	810	930	1050	840	960	1080	
	($OLS = V_{CC} – 1.2$ V)	1455	1505	1555	1490	1540	1590	1510	1560	1610	
	($OLS = V_{EE}$)	1005	1095	1185	1040	1130	1220	1065	1155	1245	
V_{outpp}	Output p–p Voltage										mV
	($OLS = V_{CC}$)	715	805		705	795		700	790		
	($OLS = V_{CC} – 0.4$ V)	125	215		120	210		120	210		
	($OLS = V_{CC} – 0.8$ V, OLS = FLOAT)	525	615		520	610		515	605		
	($OLS = V_{CC} – 1.2$ V)	0	5		0	0		0	5		
	($OLS = V_{EE}$)	325	415		320	410		320	410		
V_{IH}	Input HIGH Voltage (Single–Ended) (Note 7) D, $\overline{D}$	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC}– 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Note 8) D, $\overline{D}$	V_{EE}	V_{CC}– 1400*	V_{IH}– 150	V_{EE}	V_{CC}– 1400*	V_{IH}– 150	V_{EE}	V_{CC}– 1400*	V_{IH}– 150	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@V_{IH}) D, $\overline{D}$		30	100		30	100		30	100	μA
	SEL		5	50		5	50		5	50	
I_{IL}	Input LOW Current (@V_{IL}) D, $\overline{D}$		20	100		20	100		20	100	μA
	SEL		5	50		5	50		5	50	

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to –0.965 V.
5. All loading with 50 Ω to $V_{CC} – 2.0$ volts.
6. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
7. V_{IH} cannot exceed V_{CC}.
8. V_{IL} always $\geq V_{EE}$.

*Typicals used for testing purposes.

DC CHARACTERISTICS, INPUT WITH PECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 9)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	23	30	39	23	30	39	23	30	39	mA
V_{OH}	Output HIGH Voltage (Note 10)	2260	2310	2360	2290	2340	2390	2315	2365	2415	mV
V_{OL}	Output LOW Voltage (Note 10)										mV
	(OLS = V_{CC})	1320	1470	1620	1360	1510	1660	1390	1540	1690	
	(OLS = V_{CC} – 0.4 V)	2030	2090	2150	2065	2125	2185	2090	2150	2210	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	1550	1670	1790	1585	1705	1825	1615	1735	1855	
	(OLS = V_{CC} – 1.2 V)	2260	2310	2360	2290	2340	2390	2315	2365	2415	
	**(OLS = V_{EE})	1785	1875	1965	1820	1910	2000	1850	1940	2030	
V_{outpp}	Output p–p Voltage										mV
	(OLS = V_{CC})	750	840		740	830		735	825		
	(OLS = V_{CC} – 0.4 V)	130	220		125	215		125	215		
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	550	640		545	635		540	630		
	(OLS = V_{CC} – 1.2 V)	0	0		0	0		0	0		
	**(OLS = V_{EE})	345	435		340	430		335	425		
V_{IH}	Input HIGH Voltage (Single–Ended) (Note 12) D, $\overline{D}$	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Note 13) D, $\overline{D}$	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 11)	1.2		3.3	1.2		3.3	1.2		3.3	V
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@V_{IH}) D, $\overline{D}$		30	100		30	100		30	100	μA
	SEL		5	50		5	50		5	50	
I_{IL}	Input LOW Current (@V_{IL}) D, $\overline{D}$		20	100		20	100		20	100	μA
	SEL		5	50		5	50		5	50	

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

9. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.165 V.
10. All loading with 50 Ω to V_{CC} – 2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
12. V_{IH} cannot exceed V_{CC}.
13. V_{IL} always $\geq$ V_{EE}.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and V_{CC} – V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V (Note 14)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	23	30	39	23	30	39	23	30	39	mA
V_{OH}	Output HIGH Voltage (Note 15)	–1040	–990	–940	–1010	–960	–910	–985	–935	–885	mV
V_{OL}	Output LOW Voltage (Note 15)										mV
	–3.465 V ≤ V_{EE} ≤ –3.0 V										
	(OLS = V_{CC})	–1980	–1830	–1680	–1940	–1790	–1640	–1910	–1760	–1610	
	(OLS = V_{CC} – 0.4 V)	–1270	–1210	–1150	–1235	–1175	–1115	–1210	–1150	–1090	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	–1750	–1630	–1510	–1715	–1595	–1475	–1685	–1565	–1445	
	(OLS = V_{CC} – 1.2 V)	–1040	–990	–940	–1010	–960	–910	–985	–935	–885	
	**(OLS = V_{EE})	–1515	–1425	–1335	–1480	–1390	–1300	–1450	–1360	–1270	
	–3.0 V < V_{EE} ≤ –2.375 V										
	(OLS = V_{CC})	–1945	–1795	–1645	–1905	–1755	–1605	–1875	–1725	–1575	
	(OLS = V_{CC} – 0.4 V)	–1265	–1205	–1145	–1230	–1170	–1110	–1205	–1145	–1085	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	–1725	–1605	–1485	–1690	–1570	–1450	–1660	–1540	–1420	
	(OLS = V_{CC} – 1.2 V)	–1045	–995	–945	–1010	–960	–910	–990	–940	–890	
	(OLS = V_{EE})	–1495	–1405	–1315	–1460	–1370	–1280	–1435	–1345	–1255	
V_{outpp}	Output p–p Voltage										mV
	–3.465 V ≤ V_{EE} ≤ –3.0 V										
	(OLS = V_{CC})	750	840		740	830		735	825		
	(OLS = V_{CC} – 0.4 V)	130	220		125	215		125	215		
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	550	640		545	635		540	630		
	(OLS = V_{CC} – 1.2 V)	0	0		0	0		0	0		
	**(OLS = V_{EE})	345	435		340	430		335	425		
	–3.0 V < V_{EE} ≤ –2.375 V										
	(OLS = V_{CC})	715	805		705	795		700	790		
	(OLS = V_{CC} – 0.4 V)	125	215		120	210		120	210		
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	525	615		520	610		515	605		
	(OLS = V_{CC} – 1.2 V)	0	5		0	0		0	5		
	(OLS = V_{EE})	325	415		320	410		320	410		
V_{IH}	Input HIGH Voltage (Single–Ended) (Note 17) D, $\overline{D}$	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Note 18) D, $\overline{D}$	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 16)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
I_{IH}	Input HIGH Current (@V_{IH}) D, $\overline{D}$		30	100		30	100		30	100	μA
	SEL		5	50		5	50		5	50	
I_{IL}	Input LOW Current (@V_{IL}) D, $\overline{D}$		20	100		20	100		20	100	μA
	SEL		5	50		5	50		5	50	

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

14. Input and output parameters vary 1:1 with V_{CC}.
15. All loading with 50 Ω to V_{CC} – 2.0 volts.
16. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
17. V_{IH} cannot exceed V_{CC}.
18. V_{IL} always ≥ V_{EE}.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and V_{CC} – V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		–40°C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 7 F_{max}/JITTER) (Note 19)	7	8		7	8		7	8		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D/SEL → Q	110	160	210	115	165	215	120	170	220	ps
t_{SKEW}	Duty Cycle Skew (Note 20)		5	15		5	15		5	15	ps
t_{SKEW}	Channel Skew Q → D/SEL		5	20		5	20		5	20	ps
t_{JITTER}	Random Clock Jitter (RMS) (See Figure 7. F_{max}/JITTER) (Note 19)		0.5	1.5		0.5	1.5		0.5	1.5	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential) (Note 21)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) (Q, $\overline{Q}$)	20	40	65	20	40	65	20	40	65	ps

19. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} – 2.0 V.
20. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 8.
21. V_{INPP} (max) cannot exceed $V_{CC} - V_{EE}$.

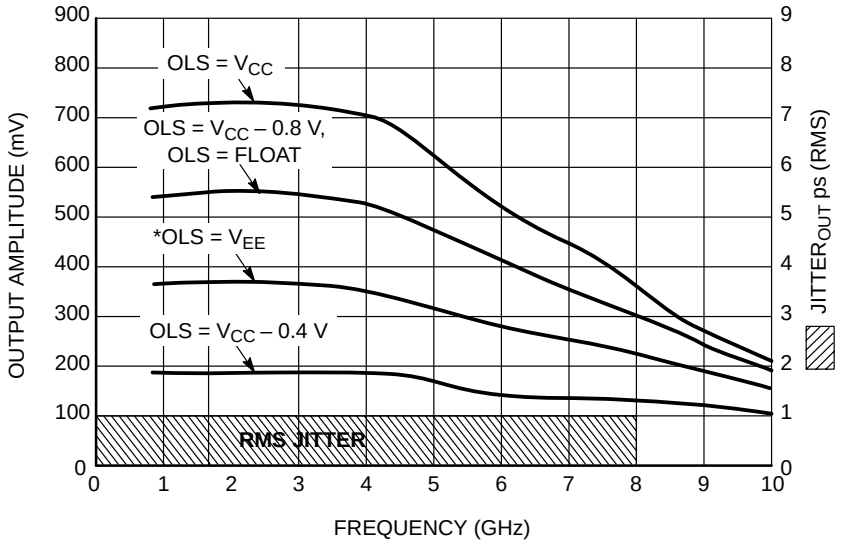


Figure 7. V_{OUT}/Jitter vs. Frequency for 2:1 MUX Mode (V_{CC} − V_{EE} = 2.5 V @ 25°C; Repetitive 1010 Input Data Pattern)

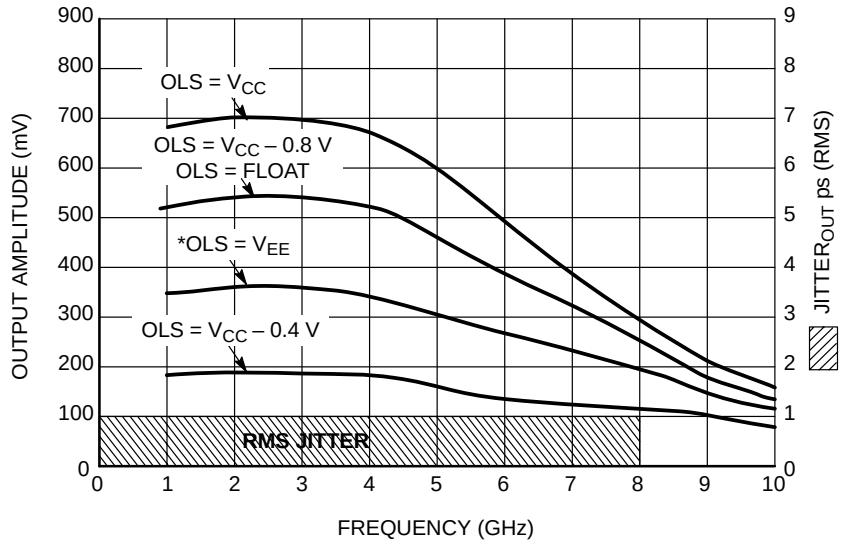


Figure 8. V_{OUT}/Jitter vs. Frequency for 2:1 MUX Mode (V_{CC} − V_{EE} = 3.3 V @ 25°C; Repetitive 1010 Input Data Pattern)

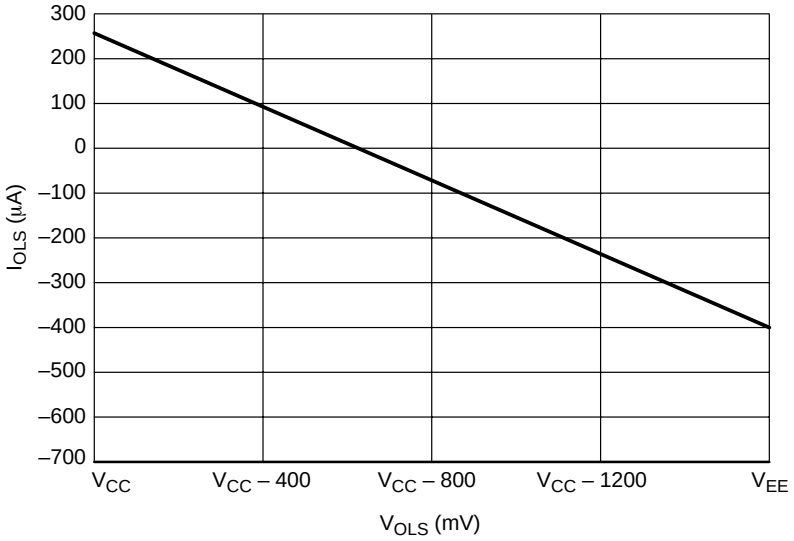


Figure 9. Typical OLS Input Current vs. OLS Input Voltage (V_{CC} − V_{EE} = 3.3 V @ 25°C)

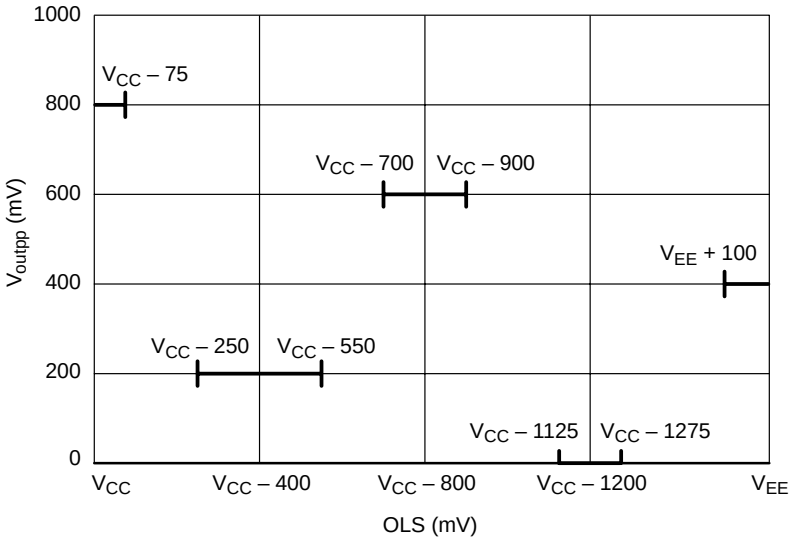


Figure 10. OLS Operating Area

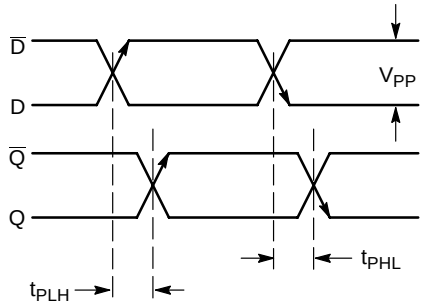


Figure 11. AC Reference Measurement

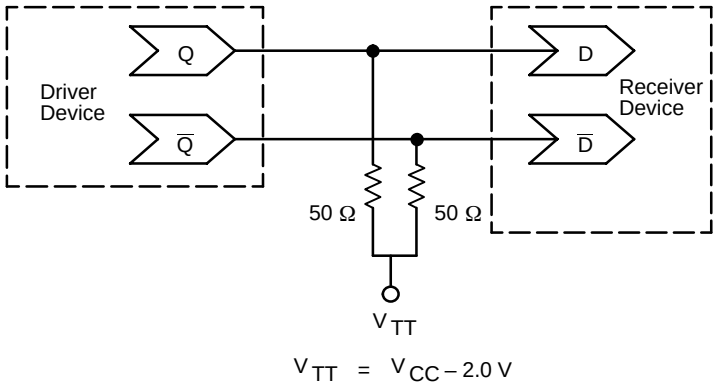
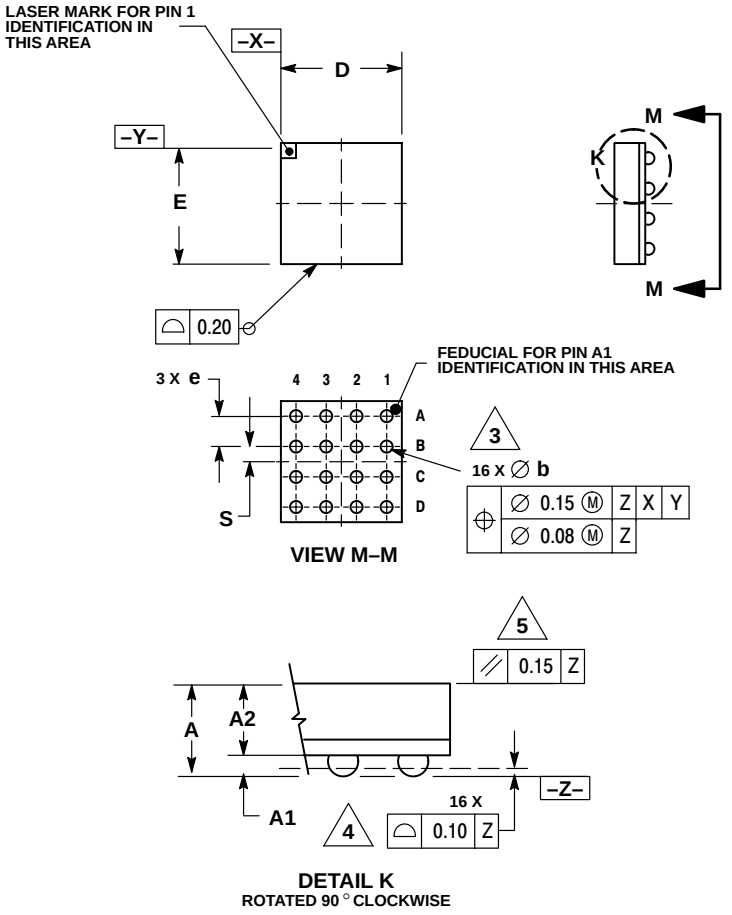


Figure 12. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 – Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA–16
BA SUFFIX
PLASTIC 4 X 4 (mm) BGA FLIP CHIP PACKAGE
CASE 489–01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

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