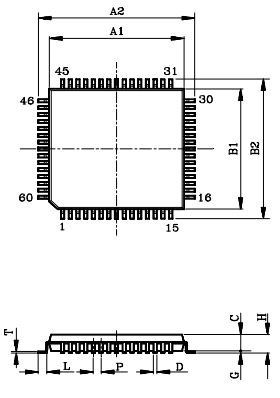
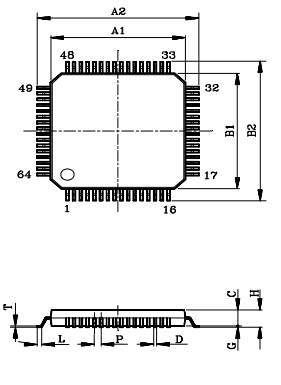
DTS MICRO CONTROLLER CONTAINING
PLL, LCD DRIVER (DTS-11)

The KIC9316F/FA/FB are a 4bit CMOS microcontroller for digital tuning system capable of making 3V low voltage operation, and containing PLL circuit, LCD driver.
CPU has 4bit parallel addition and substruction (AI/SI instructions, etc.), logical operation (OR, AN instructions etc.), plural bit judge, comparison instructions (TM, SL instructions, etc.) and time base function.
The package is 60pin mini-flat type (KIC9316F), 64 pin mini-flat type (KIC9316FA, KIC9316FB) and has abundant I/O ports and exclusive key-input ports controlled by the powerful input/output instructions (IO, KEY instructions), besides containing PLL circuit.
By combining with the prescaler KID6134AF or KID7101F or KID7103F, it permits the configuration of DTS that receives FM/AM and TV(VHF) bands.



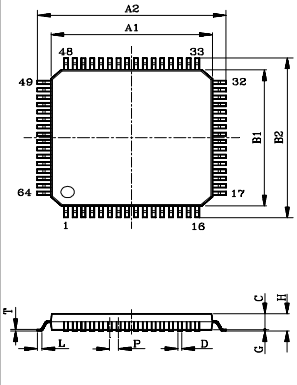
DIM	MILLIMETERS
A1	14.0±0.2
A2	16.2±0.3
B1	14.0±0.2
B2	16.2±0.3
C	1.9±0.2
D	0.35±0.1
G	0.15±0.1
H	2.25 MAX
L	0.73±0.2
P	0.8
T	0.15+0.1/−0.05

QFP−60 (1414E)



DIM	MILLIMETERS
A1	10.0±0.2
A2	12.0±0.2
B1	10.0±0.2
B2	12.0±0.2
C	1.4±0.2
D	0.2±0.1
G	0.1+0.15/−0.1
H	1.85 MAX
L	0.5±0.2
P	0.5
T	0.125+0.1/−0.05

QFP−64 (1010)



DIM	MILLIMETERS
A1	12.0±0.2
A2	14.0±0.2
B1	12.0±0.2
B2	14.0±0.2
C	1.4±0.2
D	0.3±0.1
G	0.1+0.15/−0.1
H	1.85 MAX
L	0.5±0.2
P	0.65
T	0.125+0.1/−0.05

QFP−64 (1212)

FEATURES

- 4bit micro controller for digital tuning system use.
- It is operated with 3V single power supply.
  (V_{DD}=1.8~3.6V)
- Back up of data memory (RAM) and each ports are easily made.
  (By $\overline{INH}$ terminal)
- Built-in LCD driver (1/3 duty, 1/2 bias driving, driving frequency : 52Hz) and boosting circuit for display.
- Program memory (ROM) : 16bit×2048 steps.
- Data memory (RAM) : 4bit×128 words.
- Powerful instruction set of 65 kinds. (all single word instruction).
- Instruction executing time 80μS. (75kHz crystal connection).
- Abundant addition and substruction instructions.
  (Addition instructions 12 kinds, substraction instructions 12 kinds).
- Powerful compound judge instructions.
  (TMTR, TMFR, TMT, TMF, TMTN, TMFN instructions).
- Data transfer in same low address is possible.
- Indirect transfer of register is possible.
  (MVRD, MVRS, MVGD, MVGS instructions).
- 16 Powerful general registers. (arranged in RAM).
- Stack level : 1 Level.
- Program memory (ROM) has no conception of page, field, and JUMP and CAL instruction can be freely made among 2048 steps.
- At the FM or TV band, swallow counter is composed by combining with prescaler KID6134AF or KID7103F, and is able to receive TV VHF band. At the AM or FM band, swallow counter is composed by combining with prescaler KID7101F, and is able to receive SW, AM, FM band.

- It is possible to freely refer to the contents, 16bits, of optional address within 1024 steps in program memory (ROM). (DAL instruction)
- Independent frequency input terminal at FM and AM (FM_{IN}, AM_{IN}), and two phase-comparator outputs. (DO1, DO2)
- 7 kinds of reference frequency can be selected with program.
- Powerful input/output instructions. (IO, KEY instructions)
- Exclusive input port (K0~K3) for key input use and abundant 23 exclusive LCD driving terminals.
- Abundant 15 I/O ports. (ports for which input and output can be assigned for each bit : 8, exclusive output port : 7)
  IF_{IN} port and DO1 port are able to use IN port (exclusive input port) and OT2 port (exclusive output port) by changing instruction.
- 3 kinds of back-up mode (only CPU operating, crystal oscillation and clock stop) are possible by instructions.
- 2Hz timer F/F and 10Hz interval pulse output are contained. (internal port for time base use)
- Locked condition of PLL can be detected.
- Universal-type IF counter is built in.
- 8 Output ports in LCD segment ports (S13~S20) are able to use as key return timing output ports. exclusive output ports are not only use key return timing output ports but use the others.
- 16 bit universal-type IF counter is built in, It is able to detect the auto stop signal at auto-tuning mode with counting intermediate frequency of each band.
- Built-in 3V voltage regulation circuit for driving LCD.

MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	-0.3~4.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Power Dissipation	P_D	100	mW
Operating Temperature Range	T_{opr}	-10~60	℃
Storage Temperature Range	T_{stg}	-55~125	℃

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{DD}=3.0V, Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage Range	V_{DD}	-	-	1.8	3.0	3.6	V
Memory Holding Voltage Range	V_{HD}	-	Crystal oscillation stops * (Executing CKSTP instruction)	1.2	~	3.6	
Operating Power Supply Current	I_{DD1}	-	Normal Operation, Output No-load	-	0.7	2.0	mA
	I_{DD2}	-	At only CPU operation, (Radio off, lighting display)	-	60	150	μA
	I_{DD3}	-	At stand-by mode (Radio off, only crystal oscillation)	-	50	100	
Memory Holding Power Supply Current	I_{HD}	-	Crystal oscillation stop (Executing CKSTP instruction)	-	0.1	1.0	μA
Crystal Oscillation Frequency	f_{XT}	-	*	-	75	-	kHz
Crystal Oscillation Starting Time	t_{ST}	-	Crystal Oscillation=75kHz	-	-	1.0	S

Voltage Double Boosting Circuit

Voltage Double Reference Voltage	V_{EE}	-	V_{DD} Reference (C3)	-1.2	-1.5	-1.8	V
Voltage Double Boosting Voltage	V_{LCD}	-	V_{DD} Reference (V_{LCD})	-2.4	-3.0	-3.6	
V_{LCD} Pull-Down Resistance	R_{IN3}	-	(V_{LCD})	0.75	1.5	3.0	MΩ

* Marked items are guaranteed by all conditions of V_{DD}=1.8~3.6V, Ta=-10~60℃

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Programmable counter, IF counter							
Operating Frequency Range	f_{IN1}	-	V_{IN}=0.3V_{P-P} * (FM_{IN}, AM_{IN})	0.2	~	5.0	MHz
	f_{IN2}	-	V_{IN}=0.3V_{P-P} (IF_{IN}) *	0.35	~	12.0	
Operating Input Amplitude Range	V_{IN1}	-	f_{IN}=0.2~5.0MHz * (FM_{IN}, AM_{IN})	0.3	~	V_{DD} -0.3	V_{P-P}
	V_{IN2}	-	f_{IN}=0.35~12.0MHz * (IF_{IN})	0.3	~	V_{DD} -0.3	
Programmable counter, IF counter							
FM_{IN}-PSC Transfer Delay Time	t_{pd}	-	V_{IN}=0.3V_{P-P}, * C=15pF (FM_{IN})	-	-	200	nS
PSC Maximum Load Capacity	C_L	-	(PSC) *	-	-	15	pF
LCD common output (COM1~COM3)							
Output Current	"H" Level	I_{OH1}	-	V_{LCD}=0V, V_{OH}=2.7V	-100	-200	-	μA
	"L" Level	I_{OL1}	-	V_{LCD}=0V, V_{OL}=0.3V	100	200	-	
LCD segment output (S1~S20)							
Output Current	"H" Level	I_{OH2}	-	V_{LCD}=0V, V_{OH}=2.7V	-0.5	-1.0	-	mA
	"L" Level	I_{OL2}	-	V_{LCD}=0V, V_{OL}=0.3V	50	100	-	μA
Key return output port, general purpose output port (T0~T3, OT0~OT1)							
"H" Level Output Current	I_{OH3}	-	V_{OH}=2.7V (T0~T3)	-0.5	-1.0	-	mA
N-ch FET Side Load Resistance	R_{ON}	-	V_{OL}=3.0V (T0~T3)	75	150	300	kΩ
Mute, psc output							
Output Current	"H" Level	I_{OH4}	-	V_{OH}=2.7V	-300	-600	-	μA
	"L" Level	I_{OL4}	-	V_{OL}=0.3V	300	600	-	
DO1/OT2, DO2 output							
Output Current	"H" Level	I_{OH4}	-	V_{OH}=2.7V	-300	-600	-	μA
	"L" Level	I_{OL4}	-	V_{OL}=0.3V	300	600	-	
Output off-Leakage Current		I_{TL}	-	V_{TLH}=3.0V, V_{TLL}=0V	-	-	±100	nA

* Marked items are guaranteed by all conditions of V_{DD}=1.8~3.6V, Ta=-10~60℃

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT

General purpose I/O port (P1-0~P1-3, P2-0~P2-3)

Output Current	"H" Level	I_{OH4}	-	V_{OH}=2.7V	-300	-600	-	μA
	"L" Level	I_{OL4}	-	V_{OL}=0.3V	300	600	-	
Input Leakage Current		I_{LI}	-	V_{IH}=3.0V, V_{IL}=0V	-	-	±1.0	
Input Voltage	"H" Level	V_{IH1}	-	-	2.4	~	3.0	V
	"L" Level	V_{IL1}	-	-	0	~	0.6	

$\overline{INI}$ input, IF_{IN}/IN port (When using in port)

Input Leakage Current		I_{LI}	-	V_{IH}=3.0V, V_{IL}=0V	-	-	±1.0	μA
Input Voltage	"H" Level	V_{IH2}	-	($\overline{INI}$, IN0~IN3)	2.4	~	3.0	V
	"L" Level	V_{IL2}	-	($\overline{INI}$, IN0~IN3)	0	~	0.6	

Key input port (K0~K3)

Input Pull-Down Resistance		R_{IN1}	-	-	75	150	300	kΩ
Input Voltage	"H" Level	V_{IH2}	-	-	1.8	~	3.0	V
	"L" Level	V_{IL2}	-	-	0	~	0.3	

$\overline{INH}$ input port

Input Leakage Current		I_{LI}	-	V_{IH}=3.0V, V_{IL}=0V	-	-	±1.0	μA
Input Voltage	"H" Level	V_{IH3}	-	-	2.6	~	3.0	V
	"L" Level	V_{IL3}	-	-	0	~	1.2	

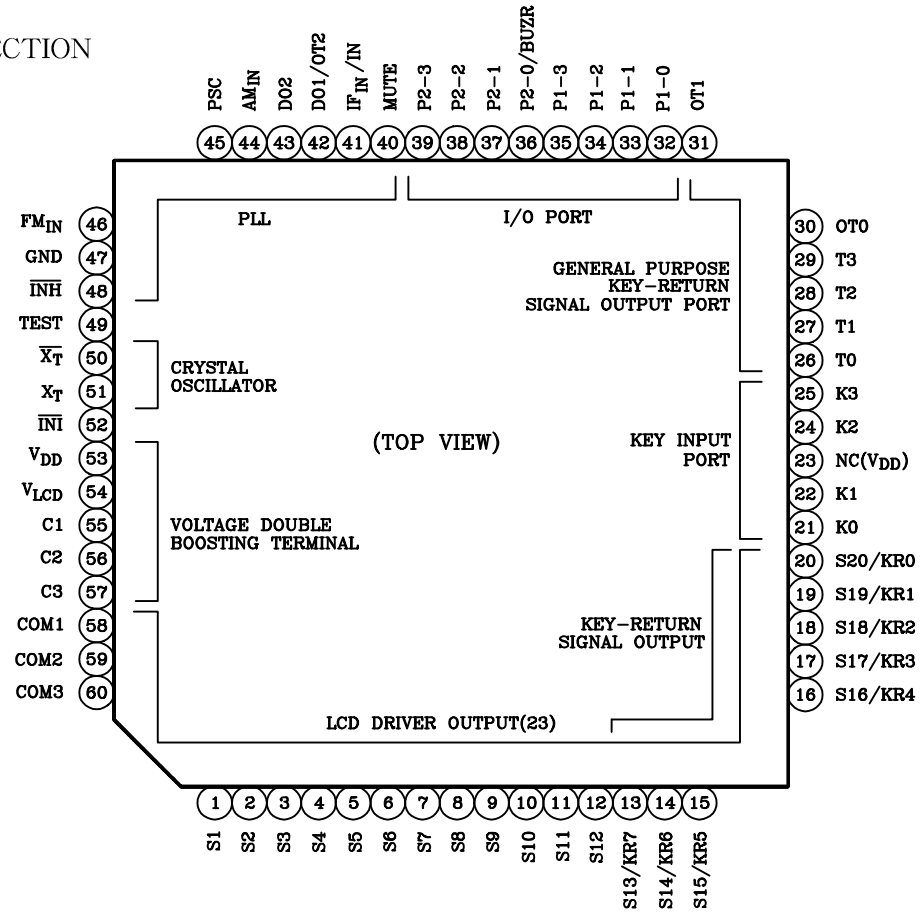
Others

Input Pull-Down Resistance	R_{IN2}	-	(TEST)	25	50	100	kΩ
XT Input Feedback Resistance	R_{fXT}	-	(X_T~$\overline{X_T}$)	3.75	7.5	15.0	MΩ
$\overline{XT}$ Output Resistance	R_{OUT}	-	($\overline{X_T}$)	50	100	200	kΩ
Input Pull-Down Resistance	R_{fIN}	-	(FM_{IN}, AM_{IN}, IF_{IN})	375	750	1500	

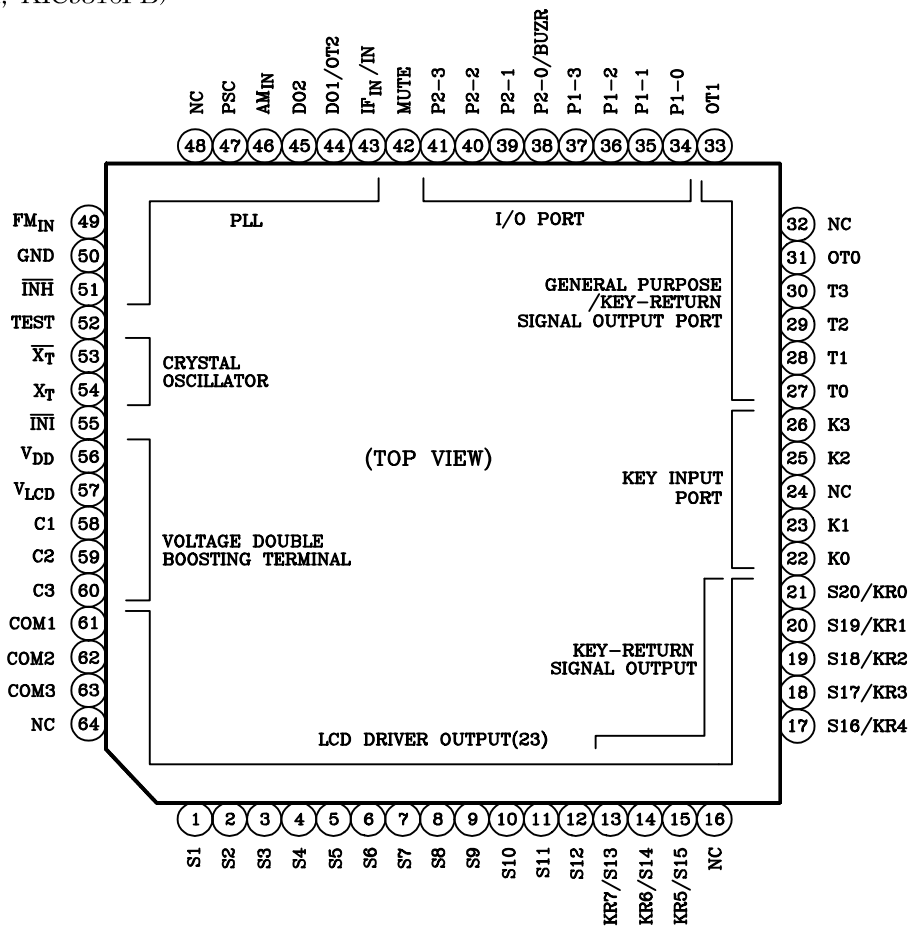
* Marked items are guaranteed by all conditions of V_{DD}=1.8~3.6V, Ta=-10~60℃

PIN CONNECTION

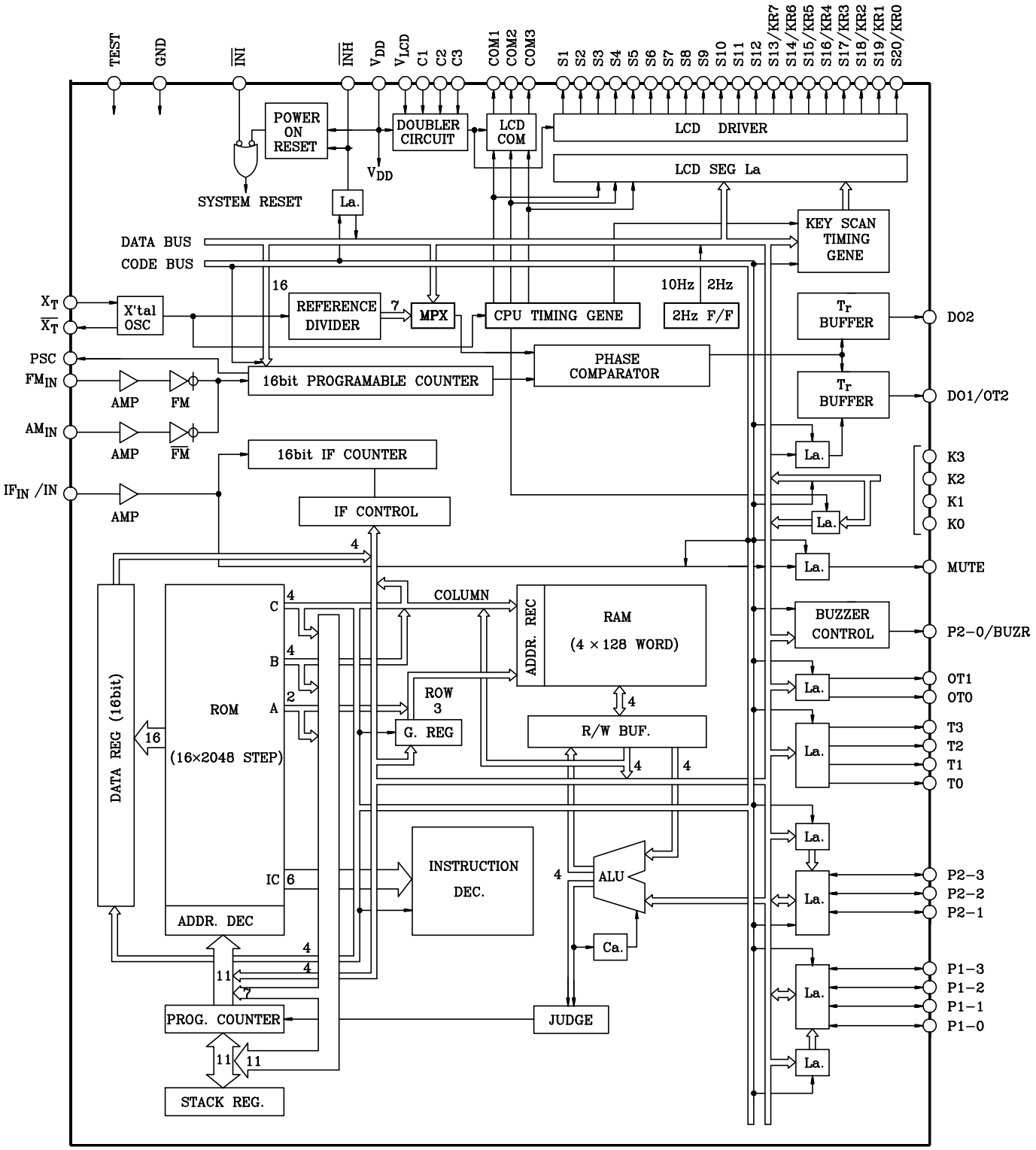
(KIC9316F)



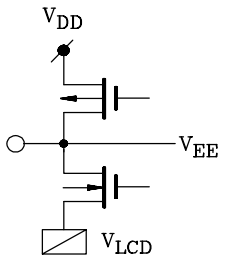
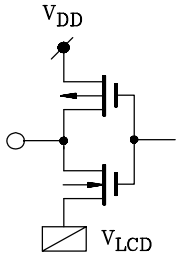
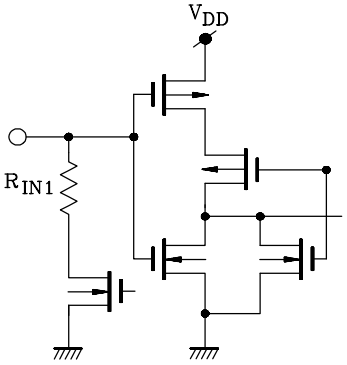
(KIC9316FA, KIC9316FB)

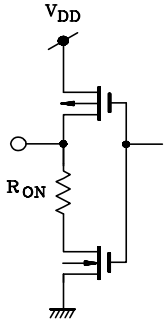
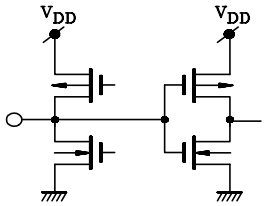
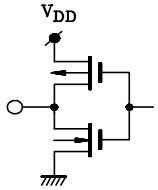
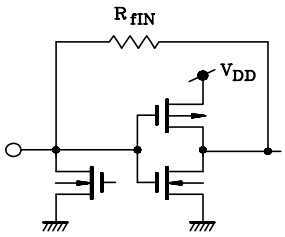
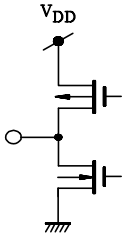


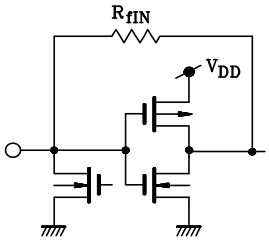
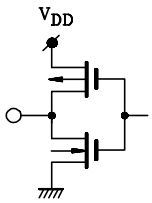
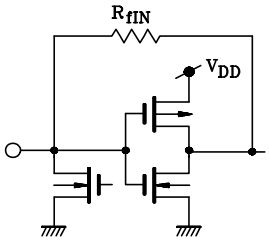
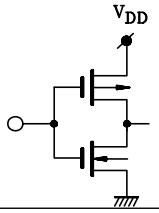
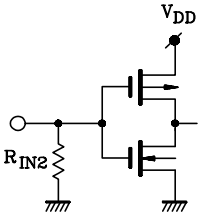
BLOCK DIAGRAM

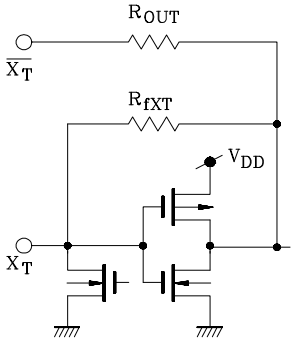
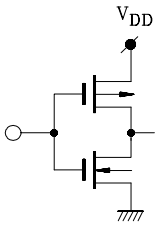


PIN FUNCTION
(Data in parentheses are for KIC9316FA, KIC9316FB)

PIN NO.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
58 (61)	COM1	LCD Common Output	This is a common signal output terminal to LCD. Indication of maximum 60 segments is possible with matrix made with S1 ~S20. To this terminal, three value levels of V_{DD}, V_{EE}, V_{LCD} are output with 3.2mS interval and 52Hz cycle.	
59 (62)	COM2			
60 (63)	COM3			
1~12	S1~S12	LCD Segment Output	This is a segment signal output terminal to LCD. Indication of maximum 60 segments is possible with matrix made with COM1, COM2 and COM3. The data for these terminals are output by the execution of SEG instruction and MARK instruction. S13/KR7~S20/KR0 are able to output LCD segment signal and Key Return Timing signal at same time by program. Maximum 32(=8×4) Key input be able to combine with matrix made with Key input ports K0~K3 without the other output port.	
13~20 (13~15) (17~21)	S13/KR7 ~S20/KR0	LCD Segment Output/Key Return Output		
21, 22 24, 25 (22, 23) (25, 26)	K0~K3	Key Input Port	This is a 4bit input port for key matrix input. It is able to input data of maximum total 56 key, maximum 24 key (=6×4) with matrix made with Key Return Timing output port, besides maximum 32 key (8×4) with matrix made with LCD Segment Output S13/KR7~S20/KR0. All these terminals are built in pull down resistances.	

PIN NO.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
26~29 (27~30)	T0~T3	General Purpose /Key Return Timing Output Port	This is a 6bit output port for General Purpose/Key Return Timing output. Besides use for general purpose output port, it is able to output the timing signal for key matrix by program. For making the key matrix, it is built in load resistance at N-ch FET side, useless the diode when used push key.	
30, 31 (31, 33)	OT0, OT1			
32~35 (34~37)	P1-0~P1-3	I/O Port	This is a 8bit general purpose I/O Port. It is possible to assign input and output for each bit by program. P2-0 is able to use as the beep sound pulse output port by program. It is able to output 3 kinds of the beep sound pulse signal by program.	
36 (38)	P2-0/BUZR	I/O Port/Buzzer Pulse Output Port		
37~39 (34~41)	P2-1~P2-3	I/O Port		
40 (42)	MUTE	Muting Output Port	This is a 1bit output port. This is usually used as muting control signal output.	
41 (43)	IF_{IN}/IN	IF Counter Input Port/Input Port	This is an IF signal input terminal of 16bit general purpose IF counter. This terminal has built-in amplifiers, and operates with C-connection and small amplitude. It is able to use as a 1bit general purpose input port by program.	
42 (44)	DO1/OT2	Phase Comparator Output/Output Port	This is a phase comparator output terminal of PLL. DO1 and DO2 are parallel outputs. Therefore, optimum filter constant can be set for each band of FM/AM. DO1 is able to use as a 1bit general purpose output port by program.	
43 (45)	DO2	Phase Comparator Output		

PIN NO.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
44 (46)	AM_{IN}	AM Programmable Counter Input	This is a programmable counter input terminal at 12bit direct frequency-divider mode. Usually the local oscillator signal at AM band is input to this terminal. This terminal has built-in amplifiers, and operated with C-connection and small amplitude.	
45 (47)	PSC	Prescaler Control Output	This is an output terminal which controls 1/15 or 1/16 frequency-dividing mode of two modulus prescaler. This output signal controls two frequency-dividing mode of external prescaler as using programmable counter for pulse-swallow counter. "H" : 1/16, "L" : 1/15	
46 (49)	FM_{IN}	FM Programmable Counter Input	This is an input terminal of programmable counter at 16bit swallow-counter mode. This terminal is input the divided frequency output signal of external prescaler, and has built-in input amplifiers and operates with C-connection and small amplitude.	
48 (51)	$\overline{INH}$	Inhibit Input	This is a signal input terminal for selecting radio mode. "H" : radio ON, "L" : radio OFF	
49 (52)	TEST	Test Input	This is an input terminal for controlling test mode control. At "H" level, test mode is made, and at "L" level, normal operation is carried out. In the test mode, the device operates as evaluator chip, and program evaluation is made possible on EPROM base through combination with external simulation board. This terminal is built in a pull-down resistance.	

PIN NO.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
50 (53)	$\overline{X_T}$	Crystal Oscillation Terminal	This is a connecting terminal of crystal resonator. Reference crystal of 75kHz is connected. During the execution of CKSTP instruction, oscillation is automatically stopped.	
51 (54)	X_T			
52 (55)	$\overline{INI}$	Initializing Input	This is a system reset signal input terminal of the device. During $\overline{INT}$ is at "L" level, reset is applied, and when it becomes "H" level, it is normal operation mode.	
54 (57)	V_{LCD}	Voltage Double Boosting Terminal	These are voltage double boosting terminal for driving LCD. Boosting capacitors are connected to these terminals. (Typ. 0.1μF~3.3μF)	-
55 (58)	C1			
56 (59)	C2			
57 (60)	C3	Reference Voltage Stabilizing Capacitor Connecting Terminal	The stabilizing capacitor of Reference Voltage is connected to this terminal for LCD driving. (Typ. 0.01μF~0.1μF)	-
53 (56)	V_{DD}	Power Supply Terminal	Power supply voltage is applied. V_{DD}=1.8~3.6V (Typ. 3.0V)	-
47 (50)	GND			