

HB56D25636 Series

262,144-Word x 36-Bit High Density Dynamic RAM Module

DESCRIPTION

The HB56D25636B is a 256k x 36 dynamic RAM module, mounted 8 pieces of 1 Mbit DRAM (HM514256JP) sealed in SOJ package and 4 pieces of 256k-bit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB56D25636B is 72-pin single in-line package. Therefore, the HB56D25636B makes high density mounting possible without surface mount technology. The HB56D25636B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ and PLCC.

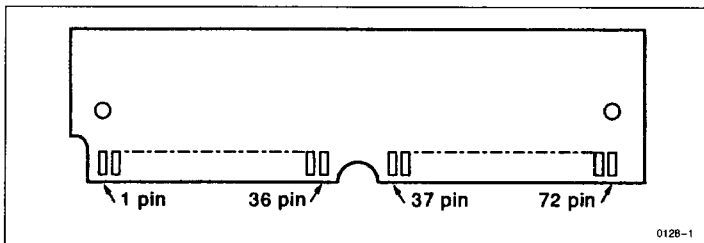
FEATURES

- 72-pin Single In-line Package
Lead Pitch 1.27mm
- Single 5V ($\pm 5\%$) Supply
- High Speed
Access Time 85 ns/100 ns/120 ns (max)
- Low Power Dissipation
Active Mode 4.24 mW/3.57 mW/3.02 mW (max)
Standby Mode 126 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle (8 ms)
- 2 Variations of Refresh
RAS Only Refresh
CAS Before RAS Refresh
- TTL Compatible

ORDERING INFORMATION

Part No.	Access Time	Package
HB56D25636B-85	85 ns	72-pin SIP Socket Type
HB56D25636B-10	100 ns	
HB56D25636B-12	120 ns	

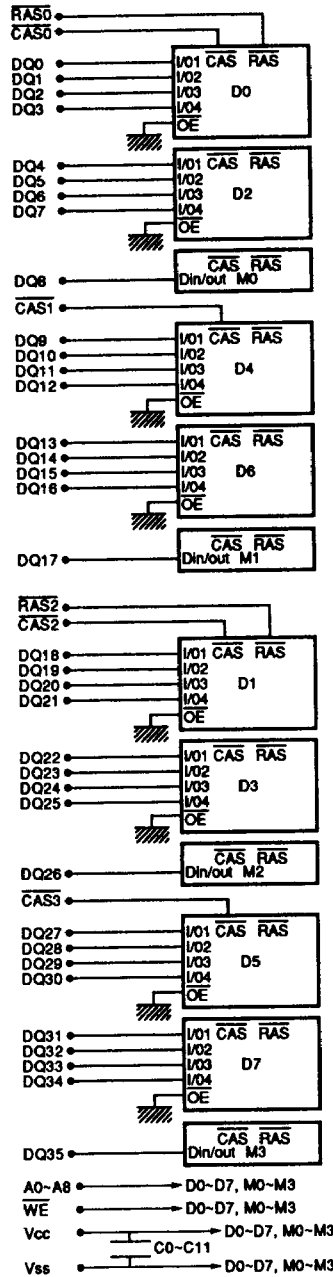
PIN OUT



Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	37	DQ ₁₇
2	DQ ₀	38	DQ ₃₅
3	DQ ₁₈	39	V _{SS}
4	DQ ₁	40	CAS ₀
5	DQ ₁₉	41	CAS ₂
6	DQ ₂	42	CAS ₃
7	DQ ₂₀	43	CAS ₁
8	DQ ₃	44	RAS ₀
9	DQ ₂₁	45	NC
10	V _{CC}	46	NC
11	NC	47	WE
12	A ₀	48	NC
13	A ₁	49	DQ ₉
14	A ₂	50	DQ ₂₇
15	A ₃	51	DQ ₁₀
16	A ₄	52	DQ ₂₈
17	A ₅	53	DQ ₁₁
18	A ₆	54	DQ ₂₉
19	NC	55	DQ ₁₂
20	DQ ₄	56	DQ ₃₀
21	DQ ₂₂	57	DQ ₁₃
22	DQ ₅	58	DQ ₃₁
23	DQ ₂₃	59	V _{CC}
24	DQ ₆	60	DQ ₃₂
25	DQ ₂₄	61	DQ ₁₄
26	DQ ₇	62	DQ ₃₃
27	DQ ₂₅	63	DQ ₁₅
28	A ₇	64	DQ ₃₄
29	NC	65	DQ ₁₆
30	V _{CC}	66	NC
31	A ₈	67	PD ₁
32	NC	68	PD ₂
33	NC	69	PD ₃
34	RAS ₂	70	PD ₄
35	DQ ₂₆	71	NC
36	DQ ₈	72	V _{SS}



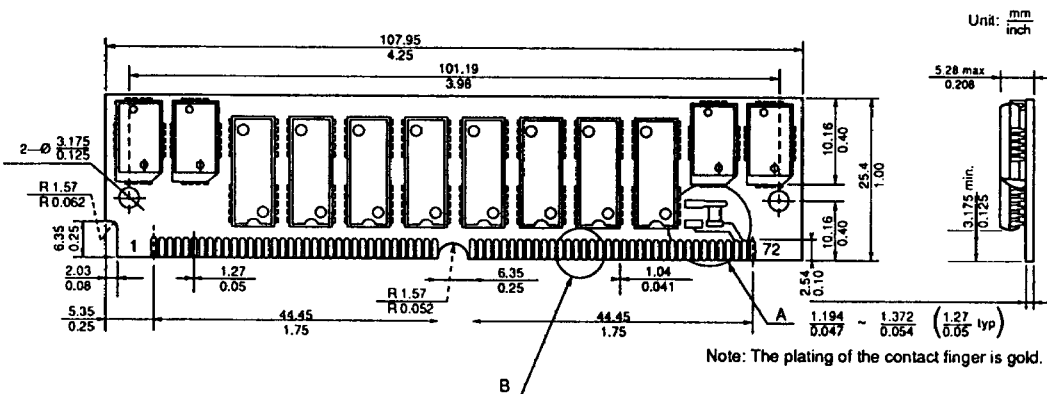
■ BLOCK DIAGRAM



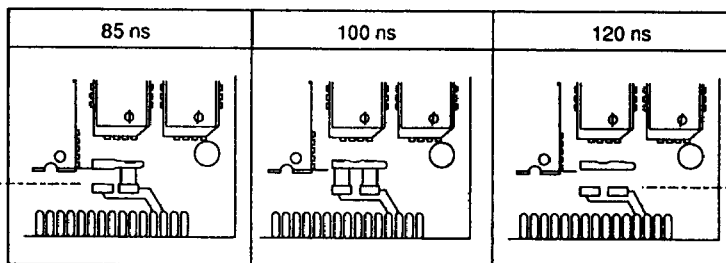
0128-2



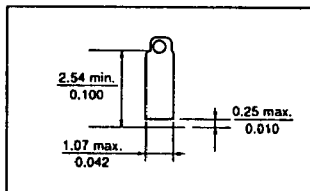
■ PHYSICAL OUTLINE



Detail A



Detail B



0128-3

■ PIN DESCRIPTION

Pin Name	Function
A ₀ –A ₈	Address Input
A ₀ –A ₈	Refresh Address Input
DQ ₀ –DQ ₃₅	Data-in/Data-out
CAS ₀ , CAS ₃	Column Address Strobe
RAS ₀ , RAS ₂	Row Address Strobe
WE	Read/Write Enable
V _{CC}	Power Supply (+ 5V)
V _{SS}	Ground
PD ₁ –PD ₄	Presence Detect Pin
NC	Non-Connection

■ PRESENCE DETECT PIN ARRANGEMENT

Pin No.	Pin Name	HB56D25636B		
		85 ns	100 ns	120 ns
67	PD ₁	V _{SS}	V _{SS}	V _{SS}
68	PD ₂	NC	NC	NC
69	PD ₃	NC	V _{SS}	NC
70	PD ₄	V _{SS}	V _{SS}	NC

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V _{SS}	(Input)	V _{IN}	– 1.0 to + 7.0
	(Output)	V _{OUT}	– 1.0 to + 7.0
Supply Voltage Relative to V _{SS}	V _{CC}	– 1.0 to + 7.0	V
Short Circuit Output Current	I _{out}	50	mA
Power Dissipation	P _T	12	W
Operating Temperature	T _{opr}	0 to + 70	°C
Storage Temperature	T _{stg}	– 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V _{SS}	0	0	0	V	
	V _{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V _{IH}	2.4	—	5.5	V	1
Input Low Voltage	V _{IL}	– 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$)

Parameter	Symbol	HB56D25636B						Unit	Test Conditions	Note
		-85		-10		-12				
		Min	Max	Min	Max	Min	Max			
Operating Current	I _{CC1}	—	808	—	680	—	576	mA	t _{RC} = Min	1, 2
Standby Current	I _{CC2}	—	24	—	24	—	24	mA	TTL Interface $\overline{\text{RAS}}$, CAS = V _{IH} , D _{out} = High-Z	
		—	12	—	12	—	12	mA	CMOS Interface $\overline{\text{RAS}}$, CAS ≥ V _{CC} - 0.2V, D _{out} = High-Z	
$\overline{\text{RAS}}$ Only Refresh Current	I _{CC3}	—	808	—	680	—	576	mA	t _{RC} = Min	2
Standby Current	I _{CC5}	—	64	—	64	—	64	mA	$\overline{\text{RAS}}$ = V _{IH} , CAS = V _{IL} , D _{out} = Enable	1
CAS Before RAS Refresh Current	I _{CC6}	—	768	—	660	—	556	mA	t _{RC} = Min	
Page Mode Current	I _{CC7}	—	764	—	680	—	576	mA	t _{PC} = Min	1, 3
Input Leakage Current	I _{LI}	- 10	10	- 10	10	- 10	10	μA	0V ≤ V _{in} ≤ 7V	
Output Leakage Current	I _{LO}	- 10	10	- 10	10	- 10	10	μA	0V ≤ V _{out} ≤ 7V, D _{out} = Disable	
Output High Voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High I _{out} = - 5 mA	
Output Low Voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low I _{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Address can be changed less than three times while $\overline{\text{RAS}} = V_{IL}$.
 3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

• Capacitance ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	88	pF	1
Input Capacitance ($\overline{\text{WE}}$)	C_{I2}	—	104	pF	1
Input Capacitance ($\overline{\text{RAS}}$)	C_{I3}	—	57	pF	1
Input Capacitance ($\overline{\text{CAS}}$)	C_{I4}	—	36	pF	1
Output Capacitance (DQ_0 – DQ_7 , DQ_9 – DQ_{16} , DQ_{18} – DQ_{25} , DQ_{27} – DQ_{34})	$C_{I/O1}$	—	17	pF	1, 2
Output Capacitance (DQ_8 , DQ_{17} , DQ_{26} , DQ_{35})	$C_{I/O2}$	—	22	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{\text{CAS}} = V_{IH}$ to disable D_{out} .

• AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$)^{1, 12}

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
RAS Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
RAS Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
CAS Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time to $\overline{\text{RAS}}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{\text{RAS}}$ to CAS Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
RAS Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
CAS Hold Time	t_{CSH}	85	—	100	—	120	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ns	15

Read Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{RAS}}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Refresh Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ Setup Time (CAS Before $\overline{\text{RAS}}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time (CAS Before $\overline{\text{RAS}}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{\text{RAS}}$ Precharge to CAS Hold Time	t_{RPC}	15	—	15	—	15	—	ns	



Write Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	20	—	25	—	30	—	ns	
Write Command Hold Time to $\overline{\text{RAS}}$	t _{WCR}	65	—	80	—	95	—	ns	
Write Command Pulse Width	t _{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t _{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t _{DH}	20	—	20	—	25	—	ns	11
Data-in Hold Time to $\overline{\text{RAS}}$	t _{DHR}	60	—	75	—	90	—	ns	

Fast Page Mode Cycle

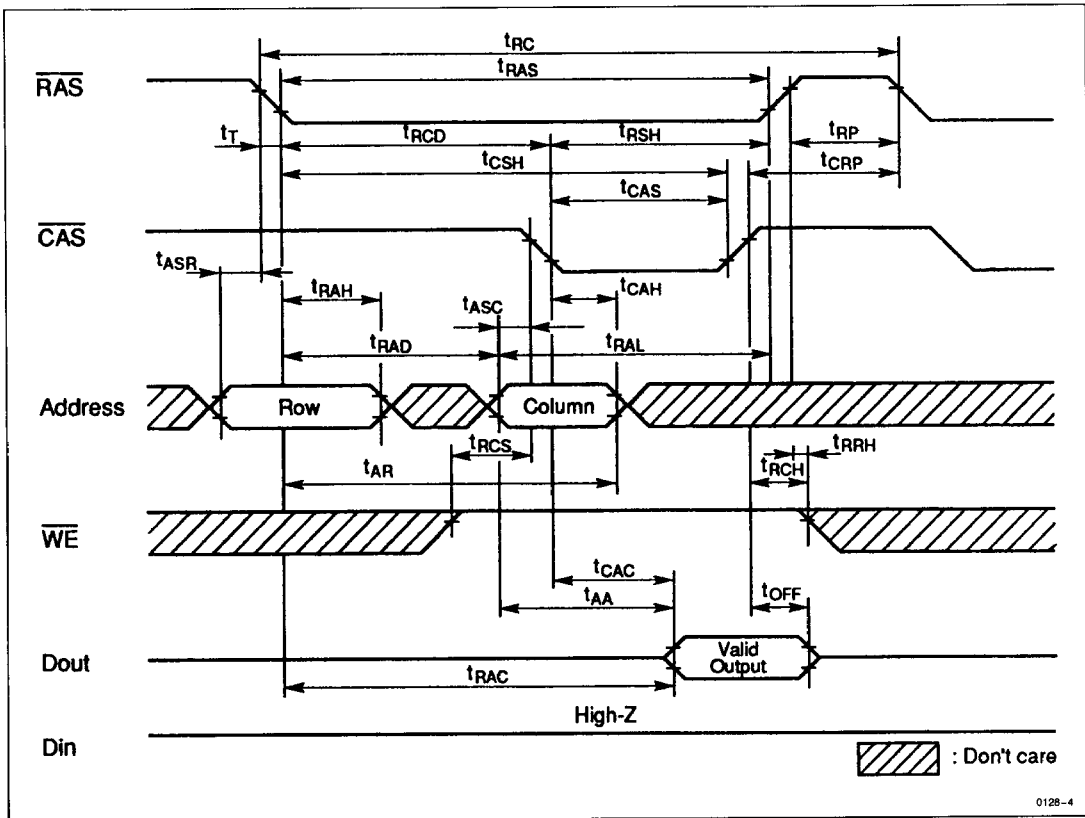
Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t _{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	t _{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	—	50	—	50	—	60	ns	14
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	50	—	50	—	60	—	ns	

Notes: 1. AC measurements assume $t_T = 5$ ns.

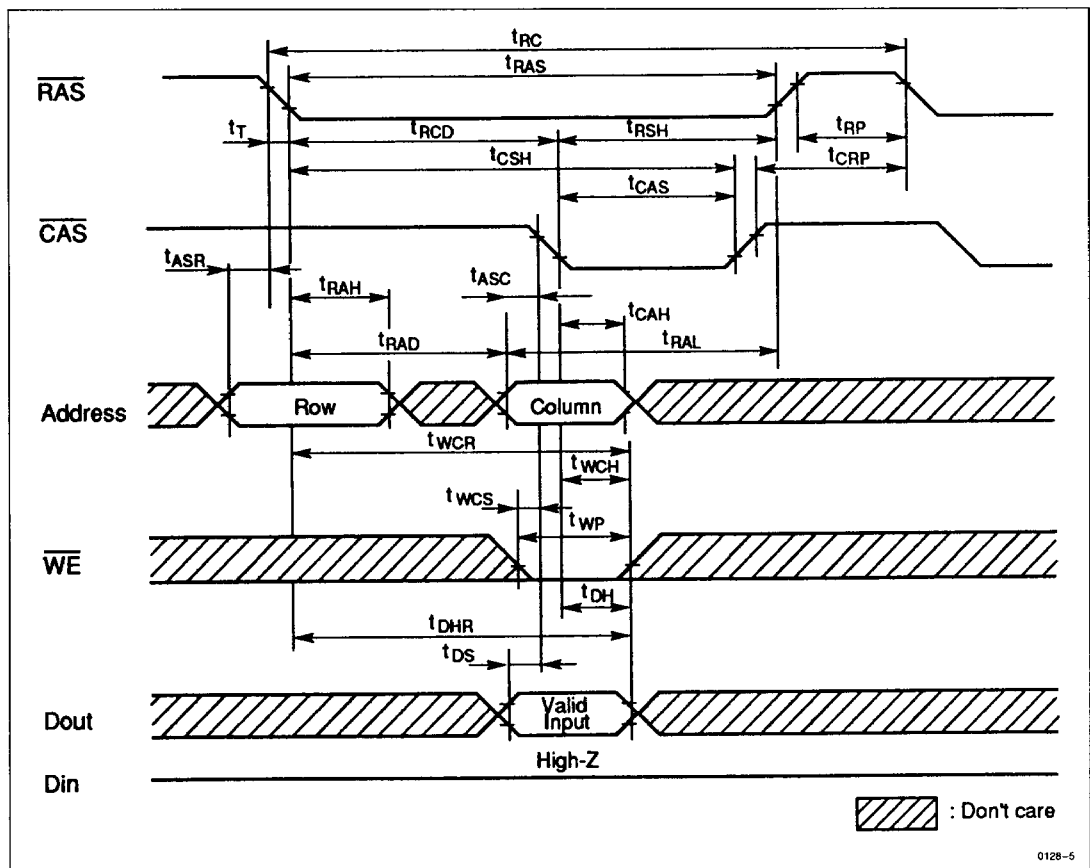
- Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2 TTL load and 100 pF.
- Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$, $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$.
- Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$, $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.
- $t_{\text{OFF}}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
- Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
- Early write cycle only ($t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$).
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle.
- An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ only refresh).
- t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
- Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
- t_{REF} defines 512 refresh cycles.

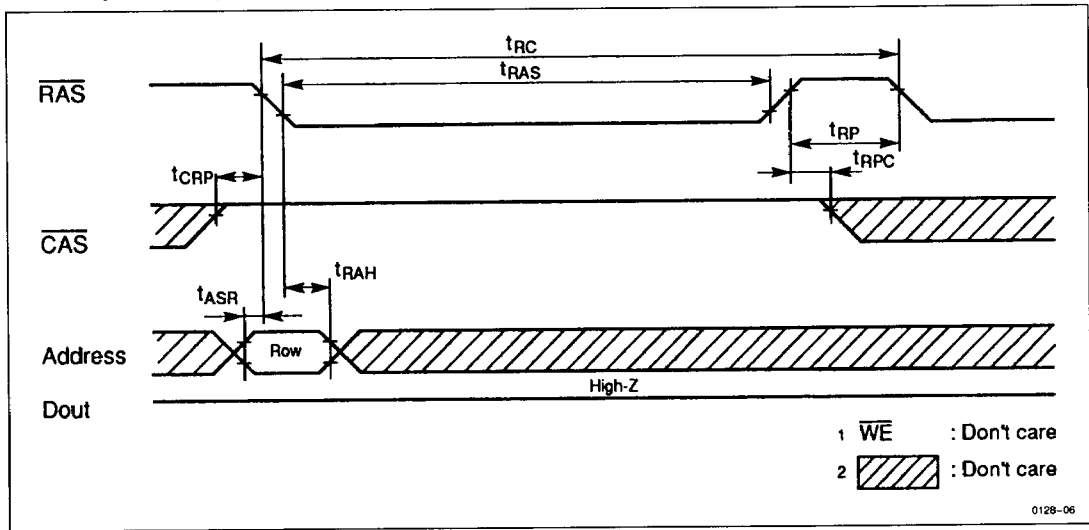
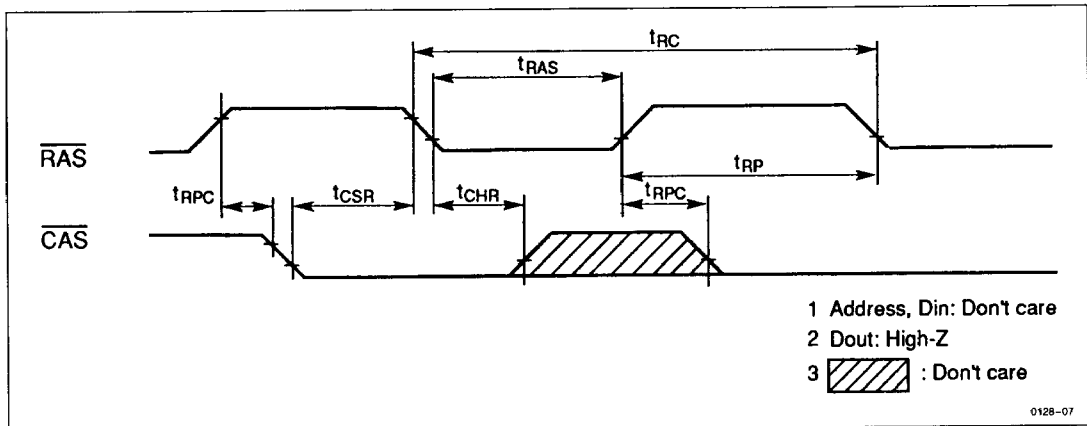
■ TIMING WAVEFORMS

• Read Cycle

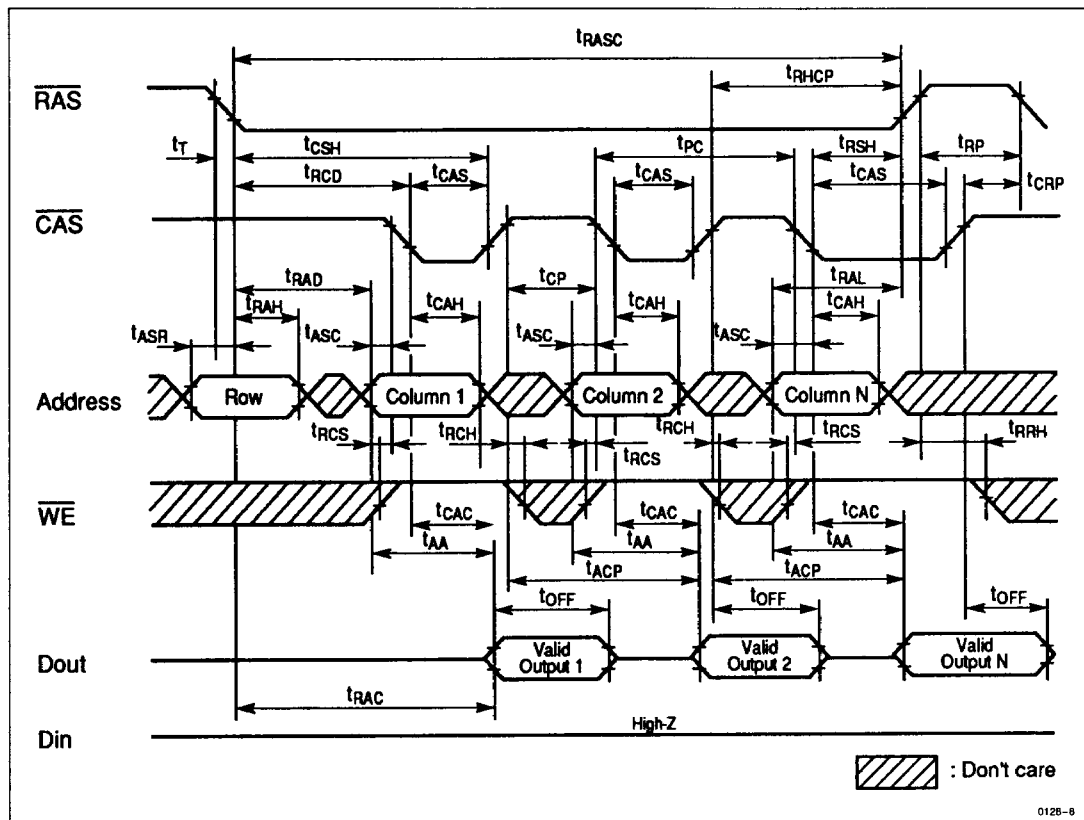


• Early Write Cycle



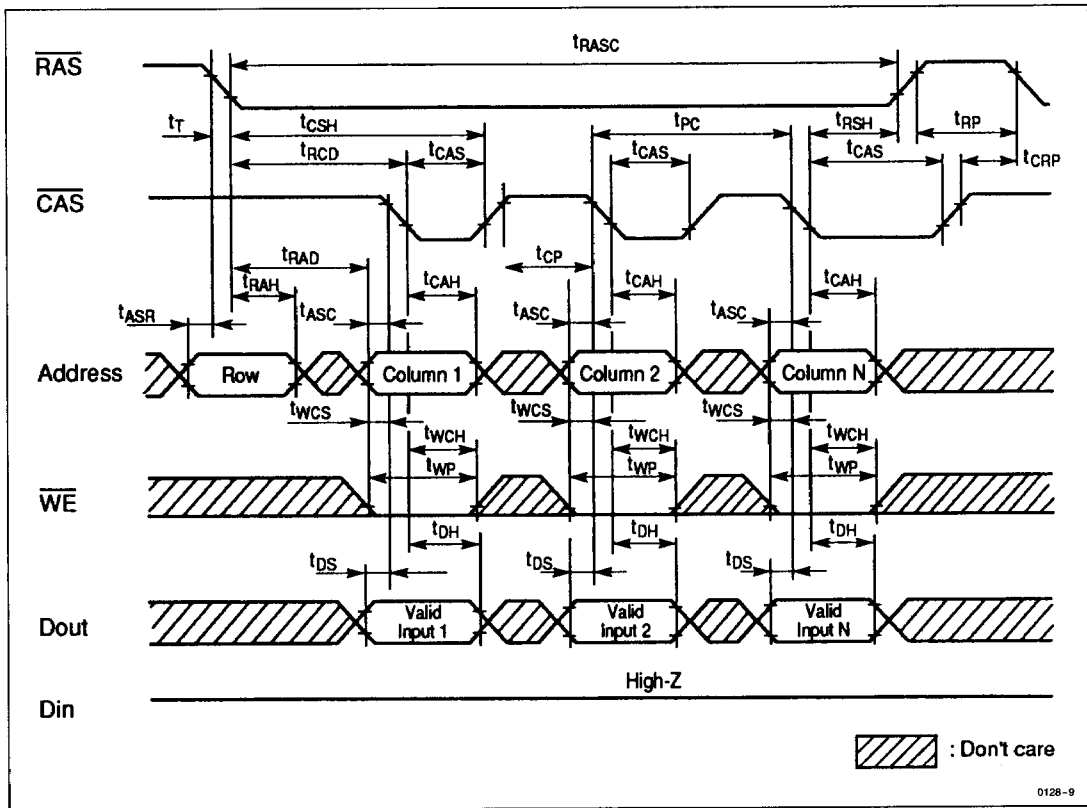
• $\overline{\text{RAS}}$ Only Refresh Cycle• $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

• Fast Page Mode Read Cycle



0126-6

• Fast Page Mode Early Write Cycle

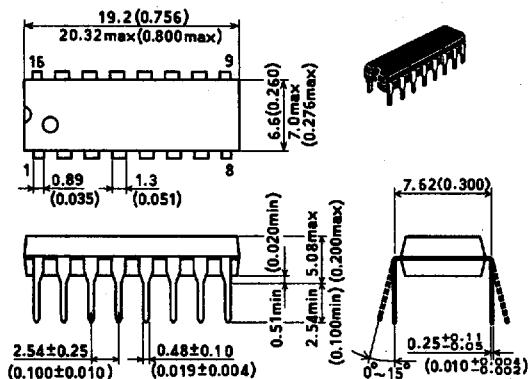


T-90-20

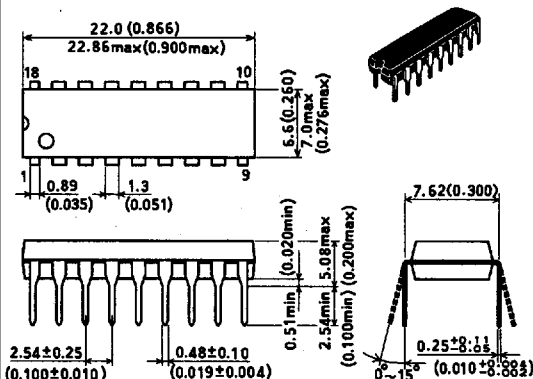
Unit: mm (inch) Scale 3/2

• Dual-in-line Plastic

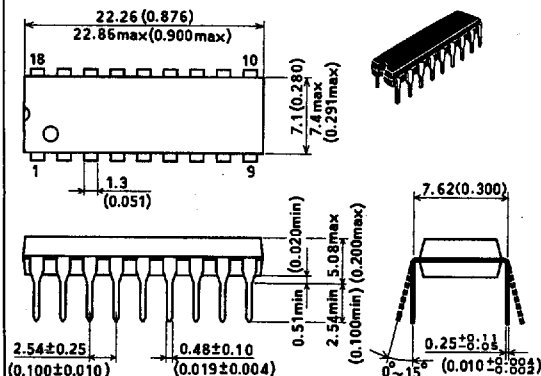
• DP-16B



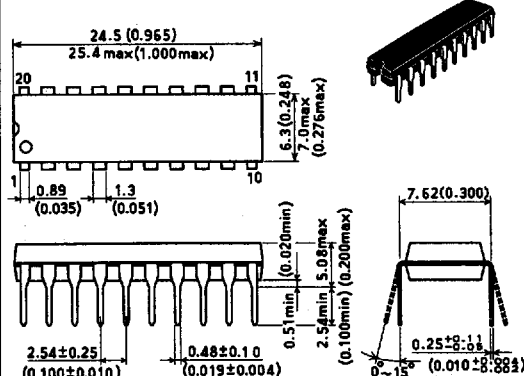
• DP-18B



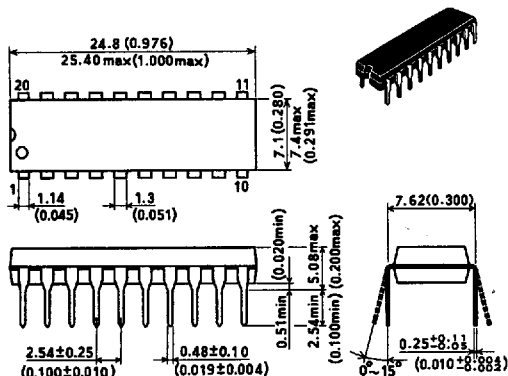
• DP-18C



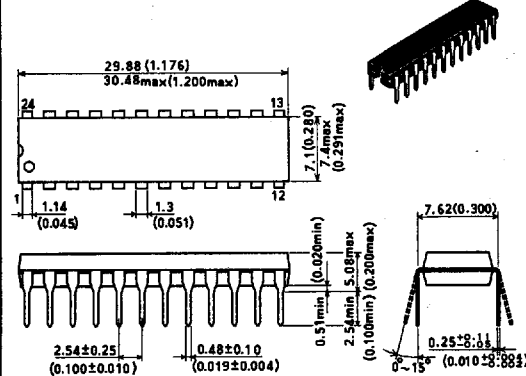
• DP-20N



• DP-20NA



• DP-20NC

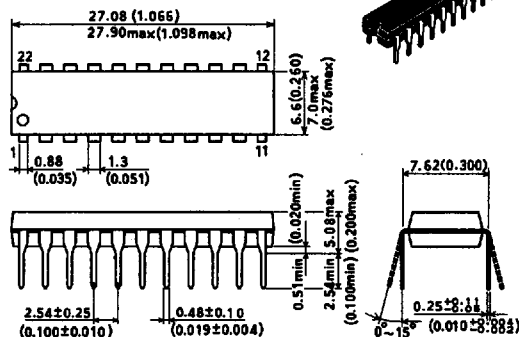


• Dual-In-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

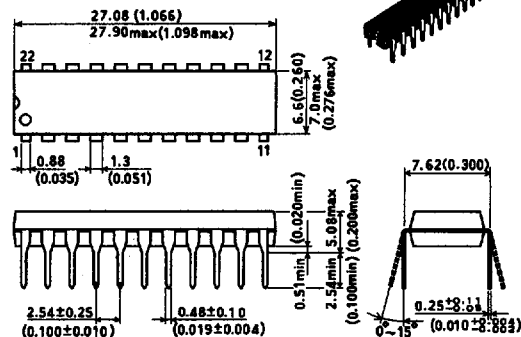
Unit: mm (inch) Scale 3/2

• DP-22N

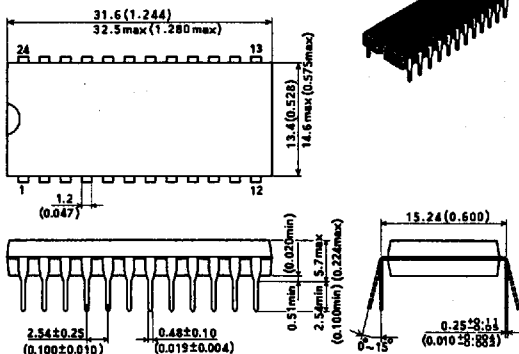


• DP-22NB

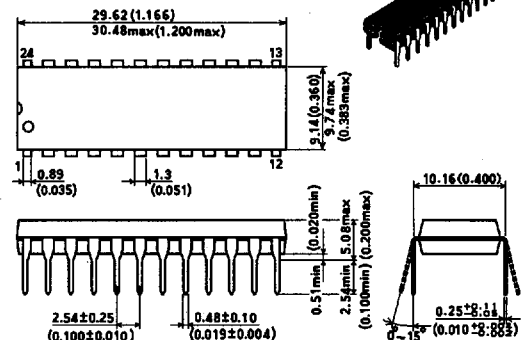
T-90-20



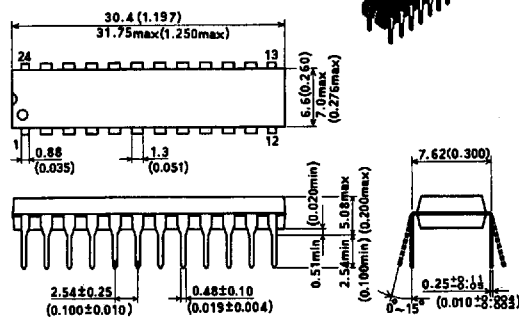
• DP-24



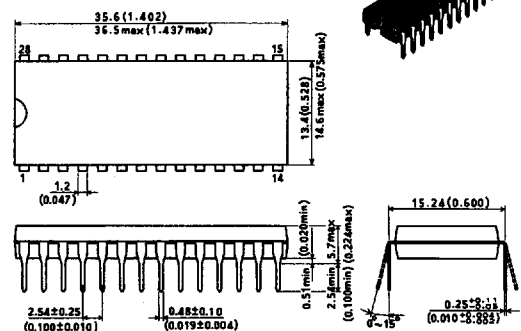
• DP-24A



• DP-24N



• DP-28

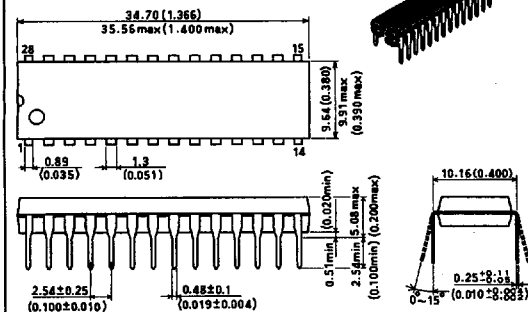


• Dual-in-line Plastic

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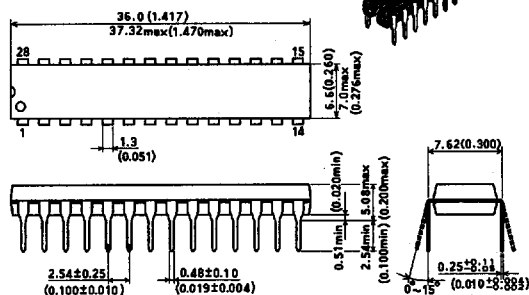
Unit: mm (inch) Scale 3/2

• DP-28C

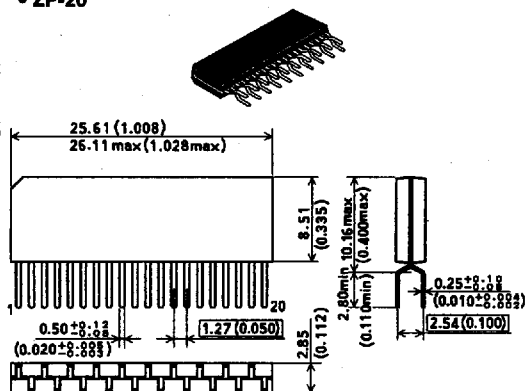


• DP-28N

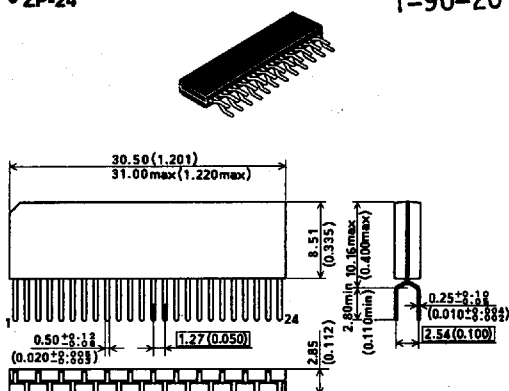
T-90-20



• ZP-20

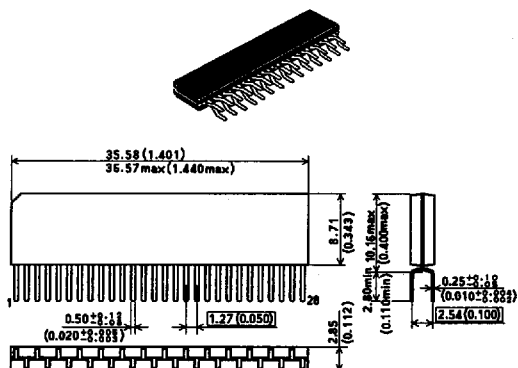


• ZP-24

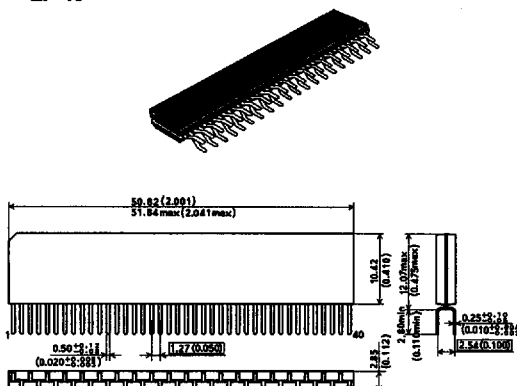


T-90-20

• ZP-28



• ZP-40



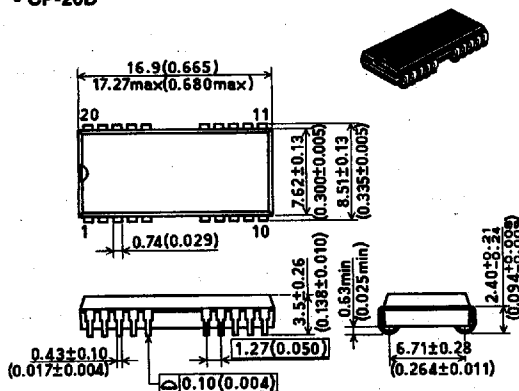
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

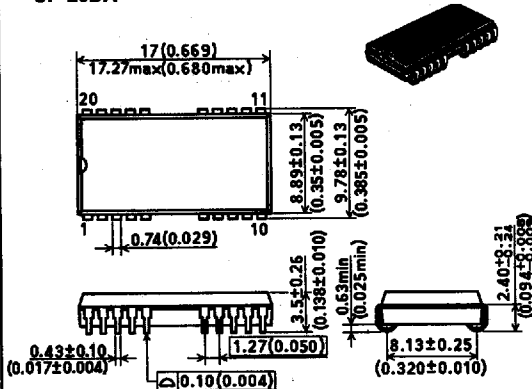
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T-90-20

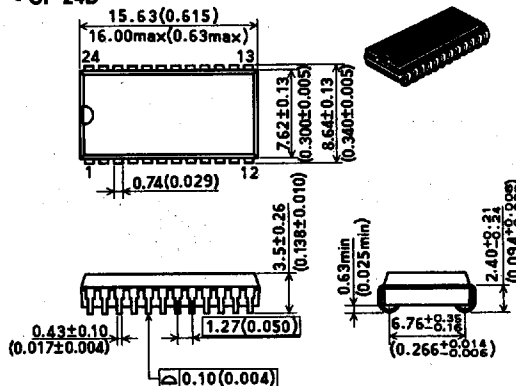
• CP-20D



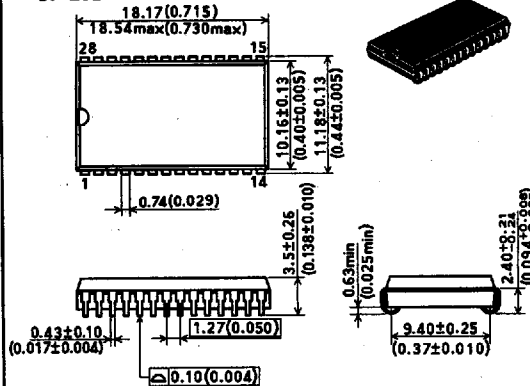
• CP-20DA



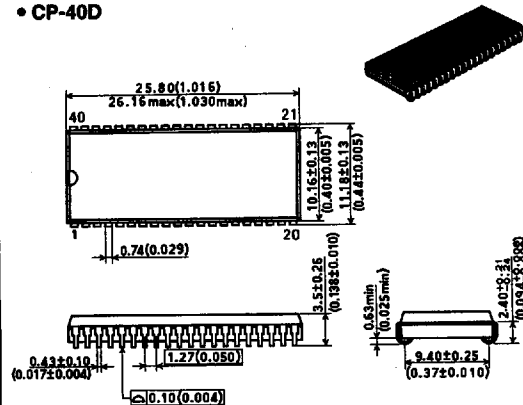
• CP-24D



• CP-28D



• CP-40D

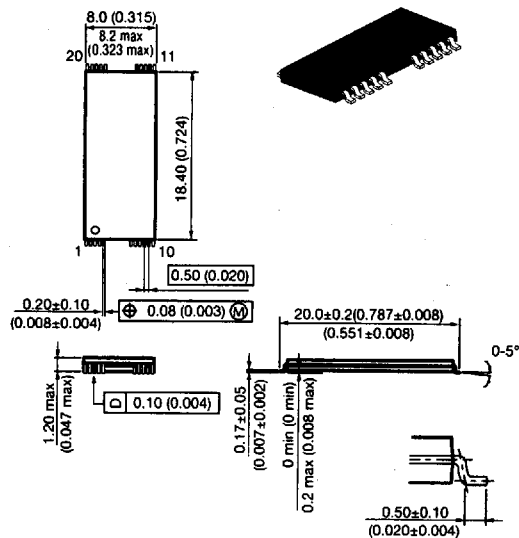


• TSOP (Thin Small Outline Package)

HITACHI/ LOGIC/ARRAYS/MEM

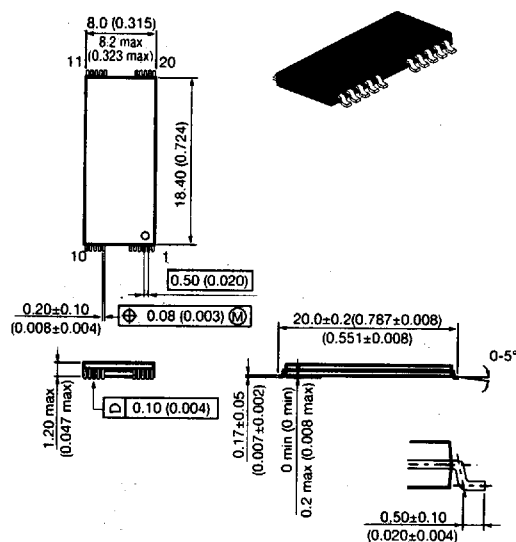
Unit: mm (inch) Scale 3/2

• TFP-20DA

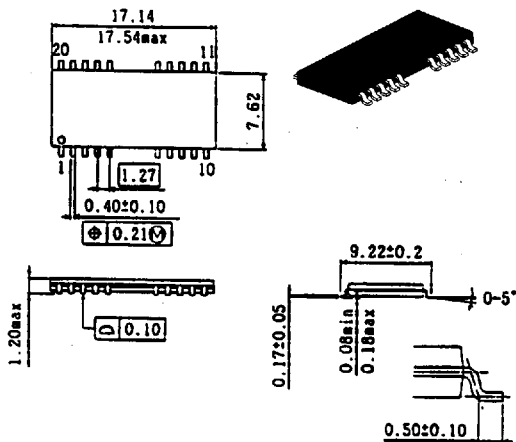


• TFP-20DAR

T-90-20



• TTP-20D



• TTP-20DR

