DPS32X16A

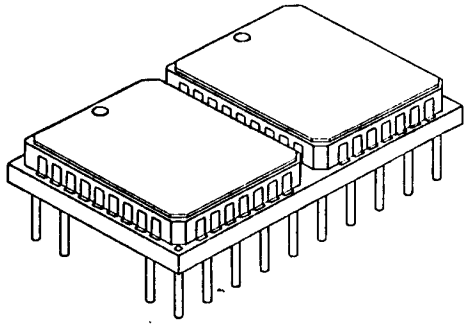
HIGH SPEED 32K X 16 CMOS SRAM PGA MODULE

PRELIMINARY

DESCRIPTION:

The DPS32X16A is a 40-pin Pin Grid Array (PGA) consisting of two 32K X 8 SRAM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients.

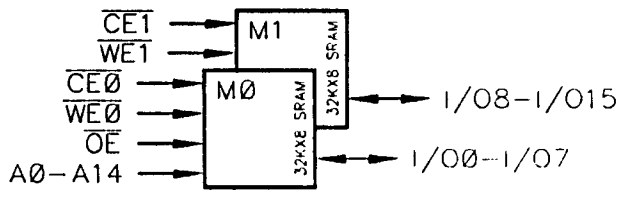
The pins have been arranged around a central 0.3" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing two 0.1µf decoupling capacitors.



FEATURES:

- Organization Available: 32K X 16
- Access Times:
  25, 35, 45, 55, 70, 85,
  100, 120, 150ns (max.)
- Low Data Retention: 2.0V min.
- Fully Static Operation - No clock or refresh required
- Three-State Outputs
- TTL-compatible Inputs and Outputs
- 40-Pin PGA (Pin Grid Array) Package
- Module can be built with devices compliant to MIL-STD 883C

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES	
A0 - A14	Address Inputs
I/O0 - I/O15	Data In/Out
$\overline{CE0}$, $\overline{CE1}$	Chip Enables
$\overline{WE0}$, $\overline{WE1}$	Write Enables
$\overline{OE}$	Output Enable
VDD	Power (+5V)
Vss	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

(TOP VIEW)

$\overline{CE0}$	1	I/O7	11	21	I/O3	31	VDD
A9	2	I/O6	12	22	I/O2	32	A0
A10	3	I/O5	13	23	I/O1	33	A1
A11	4	I/O4	14	24	I/O0	34	A2
A12	5	$\overline{OE}$	15	25	A3	35	A4
A13	6	$\overline{WE1}$	16	26	$\overline{WE0}$	36	A5
A14	7	I/O15	17	27	I/O11	37	A6
N.C.	8	I/O14	18	28	I/O10	38	A7
N.C.	9	I/O13	29	29	I/O9	39	A8
VSS	10	I/O12	20	30	I/O8	40	$\overline{CE1}$

DPS32X16A-25, -35, -45, -55, -70, -85, -100 DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-10	+10	-10	+10	-10	+10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-10	+10	-10	+10	-10	+10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		200		230		240	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		280		320		320	mA
I_{SB1}	Full Standby Supply Current (CMOS)	V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ V_{SS} + 0.2V, $\overline{CE}$ ≥ V_{DD} -0.2V		4		4		4	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		60		70		70	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

DPS32X16A-25, -35, -45, -55, -70, -85, -100 DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V, $\overline{CE}$ ≥ V_{DD} -0.2V	0.6	0.7	1.2	mA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V, $\overline{CE}$ ≥ V_{DD} -0.2V	0.7	0.8	2.4	mA
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	5			ms

DPS32X16A-120, -150 DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-10	+10	-10	+10	-10	+10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-10	+10	-10	+10	-10	+10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		90		90		90	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		120		130		140	mA
I_{SB1}	Full Standby Supply Current (CMOS)	V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ V_{SS} + 0.2V, $\overline{CE}$ ≥ V_{DD} -0.2V		200		400		600	µA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH},		4		4		4	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

DPS32X16A-120, -150 DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V, $\overline{CE}$ ≥ V_{DD} -0.2V	60	80	400	µA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V, $\overline{CE}$ ≥ V_{DD} -0.2V	80	100	480	µA
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	5			ms

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Operating Temp.	0	+25	+70	°C

ABSOLUTE MAXIMUM RATINGS[3]		
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	H*	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

* If $\overline{OE}$ is LOW during Write, t_{WHZ} must be observed before data is presented to the device.

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	20	pF	V_{IN} = 0V
C_{CE}	Chip Enable	10		
C_{WE}	Write Enable	10		
C_{OE}	Output Enable	20		
$C_{I/O}$	Data Input/Output	15		

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns**
Input and Output Timing Reference Levels	1.5V

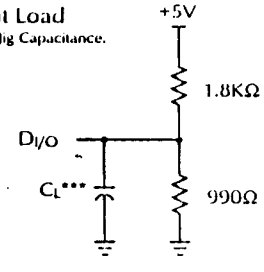
** Transition between 0.8V and 2.2V.

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 2.1mA	-	0.4	V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}

Figure 1. Output Load

*** Including Probe and Jig Capacitance.



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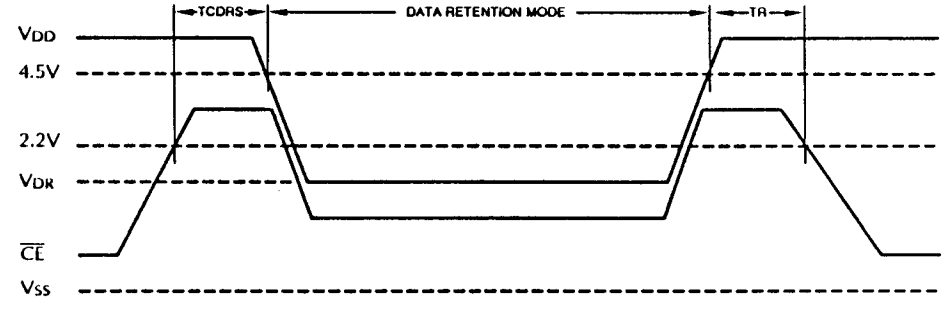
DATA RETENTION WAVEFORM



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	-25		-35		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		70		ns
2	t_{AA}	Address Access Time		25		35		45		55		70	ns
3	t_{CO}	Chip Enable to Output Valid		25		35		45		55		70	ns
4	t_{OV}	Output Enable to Output Valid		15		25		25		35		40	ns
5	t_{OH}	Output Hold from Address Change	3		3		3		3		3		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	5		5		5		5		5		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	0		0		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]

No.	Symbol	Parameter	-25		-35		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	25		35		45		55		70		ns
11	t_{AW}	Address Valid to End of Write	20		30		40		50		65		ns
12	t_{CW}	Chip Enable to End of Write	20		30		40		50		65		ns
13	t_{DW}	Data Valid to End of Write	15		20		25		25		30		ns
14	t_{DH}	Data Hold Time	3		3		3		3		3		ns
15	t_{WP}	Write Pulse Width	20		30		40		50		60		ns
16	t_{AS}	Address Set-up Time*	0		0		0		0		0		ns
17	t_{AH}	Address Hold Time	0		0		0		0		0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

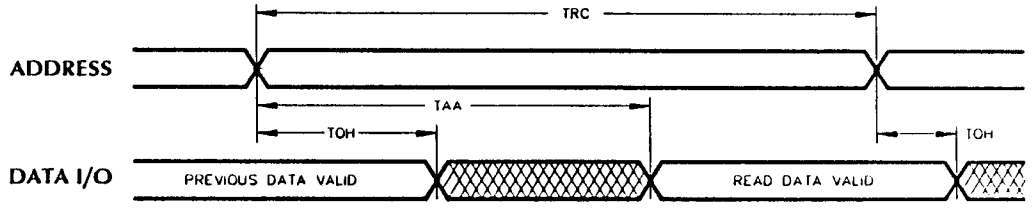
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	85		100		120		150		ns
2	t_{AA}	Address Access Time		85		100		120		150	ns
3	t_{CO}	Chip Enable to Output Valid		85		100		120		150	ns
4	t_{OV}	Output Enable to Output Valid		60		60		60		70	ns
5	t_{OH}	Output Hold from Address Change	5		10		10		10		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	10		10		10		10		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		30		35		40		50	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		30		35		40		50	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]

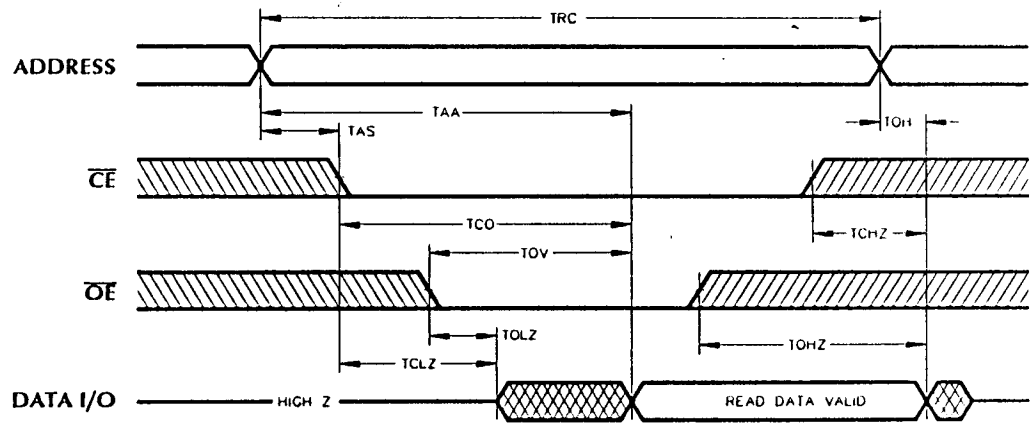
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	85		100		120		150		ns
11	t_{AW}	Address Valid to End of Write	75		90		100		120		ns
12	t_{CW}	Chip Enable to End of Write	75		90		100		120		ns
13	t_{DW}	Data Valid to End of Write	35		40		50		60		ns
14	t_{DH}	Data Hold Time	0		0		0		0		ns
15	t_{WP}	Write Pulse Width	75		80		90		100		ns
16	t_{AS}	Address Set-up Time*	0		0		0		0		ns
17	t_{AH}	Address Hold Time	0		0		0		0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		35		35		40		50	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns

* Valid for both Read and Write Cycles.

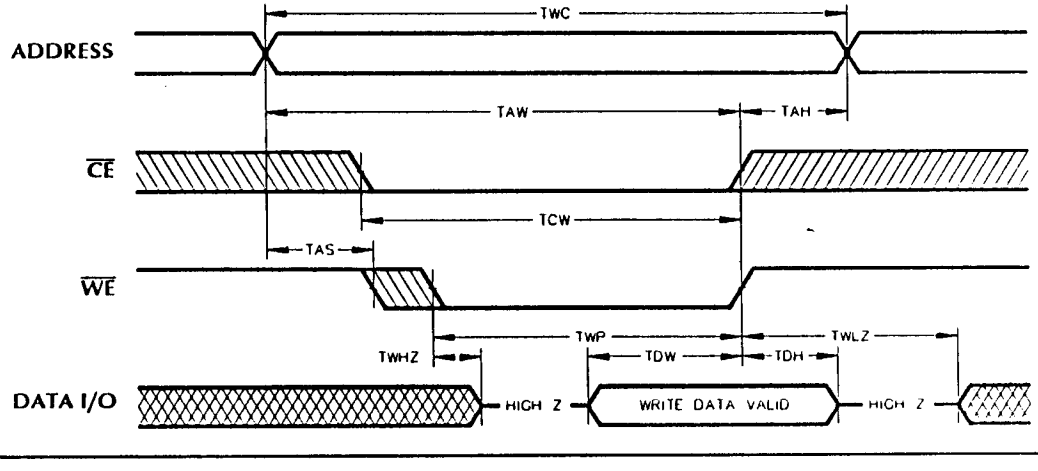
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



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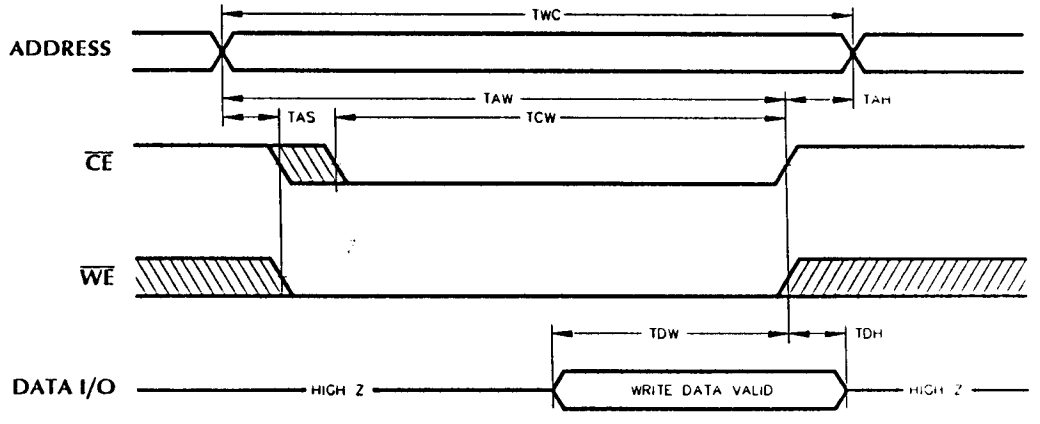
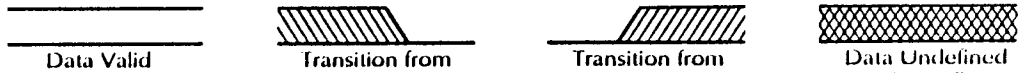
WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min.= -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY



ORDERING INFORMATION

DP S32X16 A – XXX X

PREFIX | DEVICE TYPE | PACKAGE | SPEED | GRADE

C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	-40°C to +85°C
M	MILITARY	-55°C to +125°C
B *	MIL-PROCESSED	-55°C to +125°C

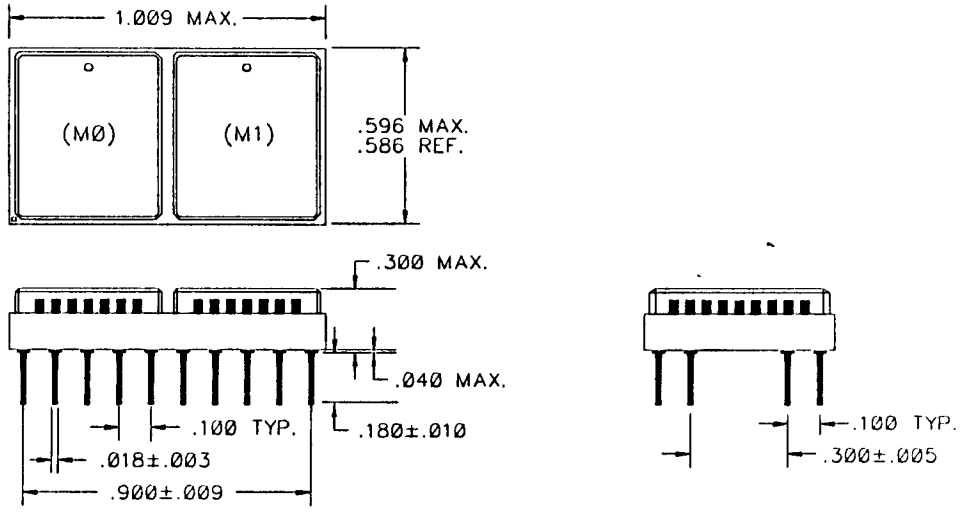
25	25ns
35	35ns
45	45ns
55	55ns
70	70ns
85	85ns
100	100ns
120	120ns
150	150ns

A 40-PIN PGA MODULE

CMOS SRAM 32KX16

* B grade modules can be constructed with 883 devices.

MECHANICAL DRAWING



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