NEWBRIDGE MICROSYSTEMS

JANUARY, 1993

LIFE CHIP

(Logical Interface Futurebus+ Engine)

CA91C899

- **Fully compatible with IEEE Std 896.1 - 1991**
  - **Profiles A & B (register selectable)**
- **TTL input/output levels**
- **Low power CMOS implementation**
- **Futurebus+ interface**
  - **896.1 compelled mode data transfer protocol**
  - **Supports split and locked transactions**
  - **Supports partial, aligned and burst transfers**
  - **Burst transfer lengths register selectable 1-64 transfers**
  - **Automatically breaks bursts into lengths slave and local bus can handle**
  - **Supports Futurebus+ 32 & 64-bit data & address widths with parity**
  - **Parity on all command lines**
  - **Operates with distributed arbiter or directly with central arbiter**
  - **Programmable split & transaction timeouts**
  - **Programmable busy retries**
  - **Registers accessible from Futurebus+**
- **Incorporates all logic and FIFOs to decouple Futurebus+ from local bus**
- **Holds multiple outstanding transactions (both incoming and outgoing)**
- **Synchronous local bus interface**
  - **32-bit address and data path with byte parity**
  - **32-bit read/write registers with default values**
  - **Supports partial, aligned and burst transfers**
  - **Supports local bus split and locked transactions**
  - **Supports single & multi-address locked transactions**
  - **Easily adapted to variety of local bus protocols**
- **Performance of 80 - 120 Mbytes/sec**
- **IEEE Std 1149.1 JTAG testability port**
- **304-PQFP or 299-PGA Package**

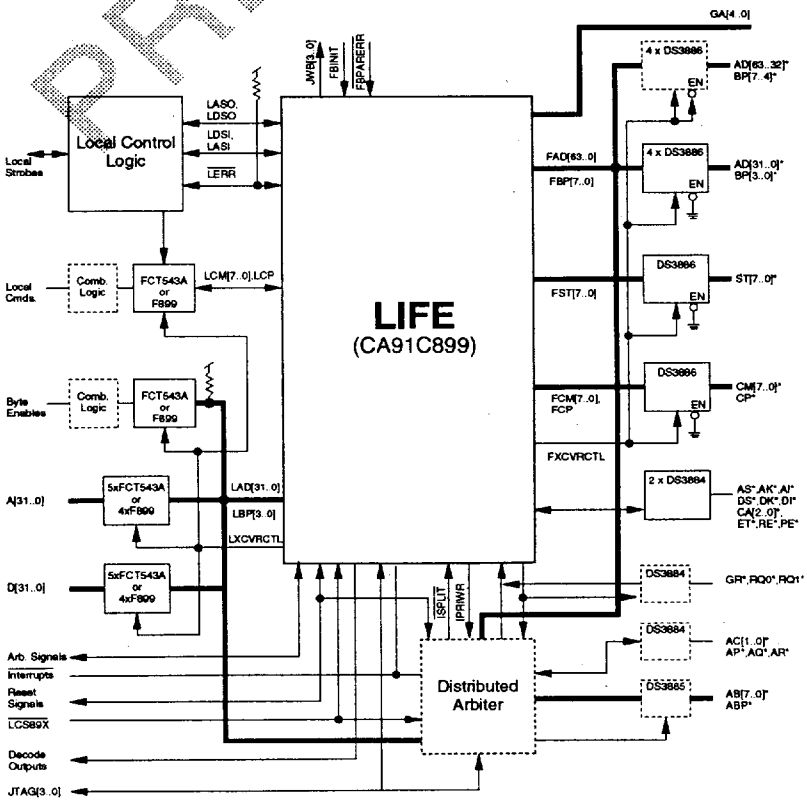

Figure 1 : Typical Use for LIFE Chip

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The *Newbridge Microsystems* LIFE chip (CA91C899) is a high performance IEEE Std 896.1-1991 Futurebus+ interface chip. It provides support for Futurebus+ compelled mode data transfer protocols as both master and slave. Internal DMAC and Futurebus+ programmable registers allow the LIFE chip to be used effectively in applications from simple I/O boards through Single Board Computers utilizing RISC or CISC microprocessors. The LIFE chip is also designed to operate in conjunction with either a distributed or central arbiter.

The internal read/write registers of the LIFE chip are accessed through the 32-bit local interface, either directly or via a Futurebus+ access that the local address decoder reflects to the on-chip registers. This scheme allows additional registers to be implemented by the module logic transparently. The registers are used to tailor the operation of the Futurebus+ Interface Chip to the requirements of each particular application. The device powers-up with default values for all parameters, allowing the LIFE chip to be accessed as a slave without programming internal registers. By setting a Profile B register bit, the device is fully compliant to IEEE Std 896.2-1991 Profile B. With the Profile B bit cleared, the chip is compliant with all the mandatory provisions of Profile A.

All the logic required to control a Futurebus+ interface is included in the LIFE chip. The device will support the protocols of any local bus architecture from a simple peripheral bus through any of the most recent CPU architectures. Support for split and locked transactions on both the local and Futurebus+ allow tightly-coupled multi-processing to occur within a module and across the backplane. Logic within the LIFE chip supports burst transactions of lengths from 1 to 64 transfers, in addition to the unlimited length allowed with connected cycles. The circuitry incorporated to allow busy retries also provides the capability of breaking a burst transaction into multiple sub-bursts of a length the slave module or local bus can best accommodate. This allows each module on the backplane to operate with the most efficient block length for its local bus and for the Futurebus+.

The LIFE chip supports a full 32-bit local and 64-bit Futurebus+ address and data path as well as local and Futurebus+ transceivers. Expansion of the address to 64-bits is accomplished by programming an internal address extension register to create a 64-bit Futurebus+ address. Outgoing data is packed into 64-bit widths from 32-bit local words, and incoming is unpacked in the reverse manner if desired. Incoming 64-bit addresses are compared against two address ranges and captured if a match occurs. The lower 32-bits of the address, along with a decode space indicator are passed to the local bus.

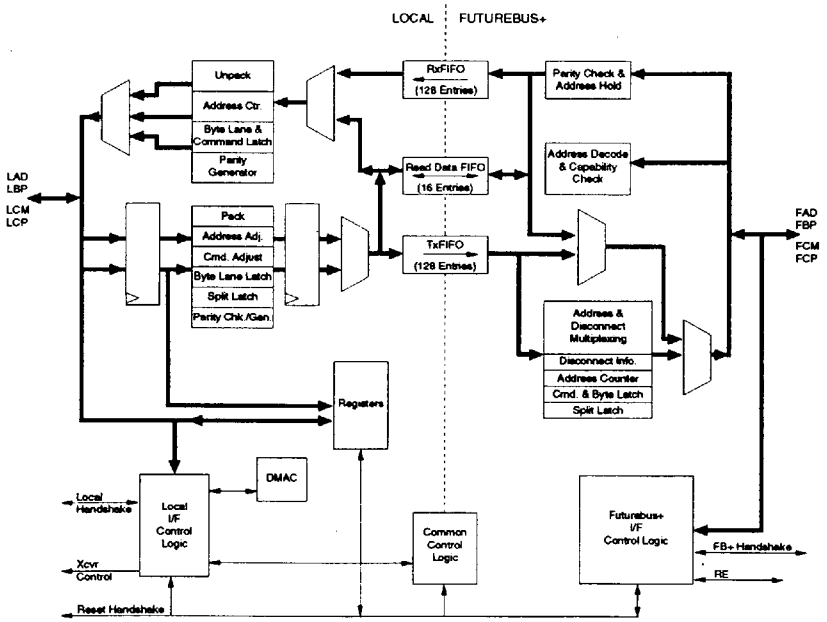


Figure 2 : LIFE Block Diagram

Table 1 : Futurebus+ Defined Register Summary

Name	Offset	D7	D6	D5	D4	D3	D2	D1	D0
ID	8	32-bit ID Register							
RST	12	32-bit Reset Start							
STIME	28	0	0	ST5	ST4	ST3	ST2	ST1	ST0
		0							
		0							
		0							
TEST	32-44	4 x 32-bit Read/Write Area Reserved for Test Registers							
UBAS	48	64-bit Futurebus+ start address of extended units space							
UBND	56	64-bit end address of extended units space							
MBAS	64	64-bit Futurebus+ start address of extended memory space							
MBND	72	64-bit end address of extended memory space							
ERRHI	384	Error Summary	Master	Connect Phase	Data Phase	Disconn Phase	Address Error	–	Command Parity Error
		AD Parity Error	Protocol Error	Transaction Timeout	Split Timeout	Unit Specific Error	Failed Beat CA [2..0]		
		8-bit Failed Beat ST[7..0] lines							
		8-bit Connection Phase CM[7..0] lines							
ERRLO	388	0							
		0							
		Connection Phase CA [2..0]			Profile B Error	–	–	–	–
		Busy Retry Threshold Exceeded	–	–	–	–	–	–	Non-Existent Transaction ID
ERRAD	392	64-bit Futurebus+ address of failed beat							
ERRBY	400	32-bit Futurebus+ Byte Lane in Error Field							
LCOM	512	32-bit Logical Common Control							
LCTL	516	32-bit Module Logical Control							
FILT	520	32-bit Bus Propagation Delay value used for Glitch Filter for Data Strobe Signals							
TTIME	528	0	0	0	TR3	TR2	TR1	TR0	0
		0							
		0							
		0							
RTY	540	16-bit Retry Threshold							
		16-bit Retry Count							
BDLY	544	0	0	0	0	DL12	DL11	DL10	DL9
		DL8	DL7	DL6	DL5	DL4	DL3	DL2	DL1
		DL0	0	0	0	0	0	0	0
		0							

Table 2 : ROM and Unit Specific Register Summary

Name	Offset	D7	D6	D5	D4	D3	D2	D1	D0
RCRC	1024	32-bit ROM Header & Checksum							
FBID	1028	32-bit Futurebus+ Identifier Code							
PID	1032	64-bit Profile Identification Area							
LCAP	1040	32-bit Module Logical Capabilities Entry							
NCAPE	1044	32-bit Node Capabilities Extended Entry							
BCCAP	1060	32-bit Busy Retry Counter Capability Entry							
BDCAP	1064	32-bit Busy Retry Delay Capability Entry							
ROOT	1088	32-bit Root Directory Header & Checksum							
VENDID	1092	32-bit Module Vendor Identifier Code Entry							
SPECID	1096	32-bit Interface Architecture Defined Identifier Code Entry							
NCAP	1100	32-bit Node Capabilities Entry							
HDWID	1104	32-bit Module Hardware Version Entry							
UNIT	1108	32-bit Pointer to Module Dependant Leafs Entry							
ISR	2048	Interrupt Enable	Interrupt Pending	Error Interrupt Pending	64-bit Data Underrun Error	Locked Transaction was Split	Bus Initialize Occurred	Ready For Withdrawal	Live Insertion Occurred
		RxFIFO Empty	TxFIFO Empty	RdFIFO Empty6	–	Loss of Synchron-ization	DMA Error	Transfer Run/ Stop(ped)	Transfer Done
		0							
		0							
CTL	2052	DMA A64 Mode Enable	DMA Local Peripheral Mode	Profile B	Remove Locks on Writes	Wrap Address	Live Withdrawal Command	Bus Initialize Command	System Reset Command
		–	–	Read / Write Transfer	Cycle Steal 16/64	4-bit transfer width field			
		0							
		8-bit Input Clock Frequency							
DLY	2056	32-bit Delay Element Programming							
AEXT	2060	32-bit address extension value							
LEN	2064	16-bit total number of transfers + 16-bit count of transfers loaded into the FIFO							
MADDR	2068	32-bit local bus address of start of block to be transferred							
FADDR	2072	64-bit Futurebus+ address of start of block to be transferred							

Table 3 : DC Characteristics for Inputs and Outputs
(Commercial / Military: T_A = -55° to +125°C, V_{DD} = 5V ± 10%)

Parameter		Test Conditions	Limits			Unit
Symbol	Description		Min	Typical	Max	
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD} = 5.5V$				
		without Pull-Down	-	-	10	µA
		with Pull-Down	-	-	150	µA
I_{IL}	Input LOW Current	$V_{IN} = V_{SS}$, $V_{DD} = 5.5V$				
		without Pull-Up	-10	-	-	µA
		with Pull-Up	-150	-	-	µA
I_{OZ}	Tri-state Output Leakage Current	$V_O = V_{SS}$, $V_{DD} = 5.5V$				
		without Pull-Up	-10	-	10	µA
		I/O with Pull-Up	-160	-	160	µA
V_{HYST}	Schmitt Trigger Hysteresis	TTL SCH	1.0	1.6	-	V
V_{T+}	Positive-going Schmitt Threshold	TTL SCH	2.7	-	3.6	V
V_{T-}	Negative-going Schmitt Threshold	TTL SCH	1.4		2.2	V
V_{IH}	Input HIGH voltage	-55° to +125°C				
		TTL	2.0	-	-	V
		CMOS	70% V_{DD}	-	-	V
V_{IL}	Input LOW Voltage	-55° to +125°C				
		TTL	-	-	0.8	V
		CMOS	-	-	30% V_{DD}	V
V_{OH}	Voltage Output HIGH	-55° to +125°C				
	TP1	I_{OH} = –1 mA	3.7	-	-	V
	TS1	I_{OH} = – 1mA	3.7	-	-	V
	TP4	I_{OH} = –4 mA	3.7	-	-	V
	TS4	I_{OH} = – 4mA	3.7	-	-	V
V_{OL}	Voltage Output LOW	-55° to +125°C				
	TP1	I_{OL} = 1mA	-	-	0.4	V
	TS1	I_{OL} = 1 mA	-	-	0.4	V
	TP4	I_{OL} = 4 mA	-	-	0.4	V
	TS4	I_{OL} = 4 mA	-	-	0.4	V
	OD4	I_{OL} = 4 mA	-	-	0.4	V

Note that the type abbreviations used above have a number suffix which indicate the current rating.

Table 4 : Capacitive Loading for the LIFE Chip

Symbol	Parameter	Limits			Unit
		Min	Type	Max	
C_{IN}	Input Pin Capacitance	-	-	5	pF
C_{IO}	Bi-directional Pin Capacitance TS4, TS1	-	-	7	pF
C_{OUT}	Output Pin Capacitance TP4, OD4, TP1	-	-	7	pF

The nominal capacitive load under operating conditions for outputs signals is 50 pF.

Pin Drive Strengths and Receiver Types

The I/O type abbreviations used in Table 5 are defined below. A numbered suffix indicates the current rating of the output.

Analog	Analog input signal
I	Input only
I/O	Input and output
O	Output only
OD	Open drain output
TP	Totem pole output
TS	Tri-state totem pole output
TTL	Input with TTL thresholds
TTL SCH	Schmitt trigger input with TTL thresholds

Table 5 : Pin List and DC Characteristics (-55°C to 125°C)

Signal Name	Type	Pin Number		In Type	Out Type	Signal Description
		CPGA	PQFP			
CLK	I	A16	132	CMOS	-	Local bus clock input
$\overline{\text{CSRDEC}}$	O	H4	59	-	TP4	Master cycle is in CSR area
$\overline{\text{EXTMEM}}$	O	H5	61	-	TP4	Master cycle is in extended memory
$\overline{\text{EXTUNIT}}$	O	G2	60	-	TP4	Master cycle is in extended units
FAD [63..0]	I/O	See Table 7		TTL	TS1	Futurebus+ address and data
FAIF	I	F18	168	TTL	-	Address inverse filtered from Futurebus+
FAIO	O	E19	166	-	TP1	Address inverse to Futurebus+
FAKF	I	H16	174	TTL	-	Address acknowledge filtered from Futurebus+
FAKO	O	F19	173	-	TP1	Address acknowledge to Futurebus+
FAQF	I	G19	179	TTL	-	Futurebus+ arbitration handshake line
FARF	I	H17	176	TTL	-	Futurebus+ arbitration handshake line
FARO	I	G18	175	TTL	-	Futurebus+ arbitration handshake line
FAS	I	J16	178	TTL	-	Address sync from Futurebus+
FASO	O	F20	177	-	TP1	Address sync to Futurebus+
FBINIT	I	M3	35	TTL	-	Bus initialization input, should be pulled down (inactive) by user
FBP [7..0]	I/O	see Table 7		TTL	TS1	Futurebus+ address parity line
FCA [2]	I	M19	193	TTL	-	Compelled capability line from Futurebus+
FCAO 2	O	L16	192	-	TP1	Capability line to Futurebus+
FCAO 1		L17	191	-		
FCM [7..0]	I/O	see Table 8		TTL	TS1	Futurebus+ command lines
FCP	I/O	L18	194	TTL	TS1	Command line parity for data and disconnect phases
FDI	I	H18	181	TTL	-	Data inverse from Futurebus+
FDIF	I	J18	182	TTL	-	Filtered data inverse from Futurebus+
FDIO	O	J17	180	-	TP1	Data inverse to Futurebus+
FDK	I	K18	184	TTL	-	Data acknowledge from Futurebus+
FDKF	I	H19	185	TTL	-	Filtered data acknowledge from Futurebus+
FDKO	O	G20	183	-	TP1	Data acknowledge to Futurebus+
FDS	I	G17	172	TTL	-	Data sync from Futurebus+
FDSO	O	E20	169	-	TP1	Data sync to Futurebus+
FET	I	J19	187	TTL	-	Futurebus+ end-of -tenure input signal
FETO	O	K16	186	-	TP1	Futurebus+ end-of-tenure output signal
FGR	I	M5	31	TTL	-	Futurebus+ control granted
FILCAP	I	L4	41	Analog	-	Filter capacitor for internal delay line
FPE	I	P2	32	TTL	-	Futurebus+ pre-empt input signal

Table 5 : Pin List and DC Characteristics (-55°C to 125°C) CONT'D

Signal Name	Type	Pin Number		In Type	Out Type	Signal Description
		CPGA	PQFP			
FREF	I	D20	165	TTL	-	Futurebus+ reset input signal (filtered)
FREO	O	E18	163	-	TP1	Futurebus+ reset output signal
FRQO1	O	R1	30	-	TP1	Futurebus+ control request priority level 1
FRQO0	O	N4	29	-	TP1	Futurebus+ control request priority level 0
FST [7..0]	I/O	see Table 8		TTL	TS1	Futurebus+ status line
FXADDIR	O	P16	220	-	TP4	Direction control for Futurebus+ AD[ ] buffers
FXADW 1	O	T17	219	-	TP4	Encoded width of Futurebus+ AD[ ] lines
FXADW 0		P17	218	-		
FXCLK	O	T18	216	-	TP4	Futurebus+ transceiver transmit clock
FXCMDIR	O	U18	221	-	TP4	Direction control for Futurebus+ CM [ ] buffers
FXLE	O	U19	217	-	TP4	Futurebus+ transceiver receive latch
FXSTDIR	O	R17	222	-	TP4	Direction control for Futurebus+ ST [ ] buffers
GA [4..0]*	I	see Table 8		TTL	-	Futurebus+ geographical address line
$\overline{\text{IBUSHLD}}$	O	D19	162	-	TP1	Live insertion alignment in progress
$\overline{\text{IBUSINIT}}$	O	G16	161	-	TP1	Futurebus+ initialize in progress
$\overline{\text{IPRIWR}}$	O	M4	33	-	TP1	Signal to arbiter to latch response priority
$\overline{\text{ISPLIT}}$	I	N3	34	TTL	-	Current Futurebus+ master is split capable
JTAG 3	I	K5	48	TTL	-	IEEE 1149.1 Testability bus
JTAG 2		K2	47			
JTAG 1		K4	46			
JTAG 0	O	L2	45	-	TP4	
LAD [31..0]	I/O	see Table 6		TTL	TS4	Local bus address and data
LASI	I	B15	130	TTL	-	Local handshake address strobe IN
LASO	O	C15	134	-	TP4	Local handshake address strobe OUT
LBP 3	I/O	E12	126	TTL	TS4	Local bus address and data parity line
LBP 2		B12	117			
LBP 1		B8	104			
LBP 0		A6	94			
LCM [7..0]	I/O	see Table 6		TTL	TS4	Local bus command
LCP	I/O	D2	74	TTL	TS4	Local bus command parity
$\overline{\text{LCS}}$	I	B16	135	TTL	-	Selects DS3805 internal registers
LDSI	I	A17	137	TTL	-	Local handshake data strobe IN
LDSO	O	C16	138	-	TP4	Local handshake data strobe OUT
$\overline{\text{LERR}}$	I	H1	51	TTL/SCH	-	Local bus error
LGR	I	H3	56	TTL	-	Local bus control granted

Table 5 : Pin List and DC Characteristics (-55°C to 125°C) CONT'D

Signal Name	Type	Pin Number		In Type	Out Type	Signal Description
		CPGA	PQFP			
$\overline{\text{LINT}}$	O	J3	53	-	OD4	Local bus interrupt
$\overline{\text{LPAREN}}$	I	J2	49	TTL	-	Local bus parity checking enable
LREQ	O	G1	58	-	TP4	Local bus control requested
LRSTDN	I	J4	55	TTL/SCH	-	Local module reset complete
$\overline{\text{LSYSRST}}$	I/O	H2	54	TTL	OD4	System reset command to/from local module
$\overline{\text{LXABOOE}}$	O	C14	128	-	TP4	Enable LAD onto local address bus
$\overline{\text{LXAIOE}}$	O	E13	129	-	TP4	Enable local address onto LAD
$\overline{\text{LXAOLE}}$	O	D13	127	-	TP4	Allow LAD through address latch
$\overline{\text{LXBIOE}}$	O	B17	140	-	TP4	Enable local byte disables onto LAD bus
$\overline{\text{LXBOLE}}$	O	C17	143	-	TP4	Allow LAD through byte disable latch
$\overline{\text{LXDIOE}}$	O	D16	141	-	TP4	Enable local data onto LAD
$\overline{\text{LXDOOE}}$	O	D14	142	-	TP4	Enable LAD onto local data bus
$\overline{\text{POR}}$	I	G5	75	TTL	-	Power on reset

Table 6 : Local Address and Data Pins (FAD) and Command Line Pins (LCM)

Signal	CPGA	PQFP	Signal	CPGA	PQFP
LAD31	B14	125	LAD11	D8	99
LAD30	D12	124	LAD10	B7	98
LAD29	C13	123	LAD9	E8	97
LAD28	C12	122	LAD8	C7	96
LAD27	A14	121	LAD7	D7	93
LAD26	C11	120	LAD6	B6	91
LAD25	B13	119	LAD5	C6	90
LAD24	E11	118	LAD4	A5	88
LAD23	D11	116	LAD3	B5	87
LAD22	B11	115	LAD2	C5	85
LAD21	D10	111	LAD1	B4	84
LAD20	B10	110	LAD0	E7	83
LAD19	E10	109	LCM7	G4	73
LAD18	B9	108	LCM6	E3	72
LAD17	C10	107	LCM5	E2	70
LAD16	A8	106	LCM4	E1	69
LAD15	D9	103	LCM3	F3	67
LAD14	C8	102	LCM2	F2	66
LAD13	E9	101	LCM1	F1	64
LAD12	A7	100	LCM0	G3	62

Table 7 : Futurebus+ Address and Data (FAD) and Address and Data Parity (FBP) Pins

Signal	CPGA	PQFP	Signal	CPGA	PQFP
FAD63	N5	27	FAD27	W10	271
FAD62	R2	26	FAD26	T10	270
FAD61	P4	24	FAD25	W11	269
FAD60	T1	23	FAD24	U10	268
FAD59	R3	21	FAD23	U11	263
FAD58	T2	20	FAD22	X13	262
FAD57	U1	18	FAD21	T11	261
FAD56	T3	17	FAD20	W13	260
FAD55	T4	14	FAD19	V13	258
FAD54	P5	13	FAD18	V12	257
FAD53	U3	12	FAD17	X14	256
FAD52	V2	10	FAD16	W14	254
FAD51	R5	9	FAD15	V14	252
FAD50	W2	8	FAD14	U13	251
FAD49	W3	301	FAD13	X15	250
FAD48	U6	300	FAD12	T13	249
FAD47	T7	298	FAD11	U14	248
FAD46	U5	297	FAD10	W15	246
FAD45	U7	296	FAD9	V15	245
FAD44	W4	295	FAD8	X16	243
FAD43	V5	294	FAD7	V16	240
FAD42	X4	292	FAD6	W17	239
FAD41	W5	291	FAD5	U16	237
FAD40	V6	289	FAD4	T14	236
FAD39	W6	286	FAD3	V17	235
FAD38	V7	285	FAD2	W18	233
FAD37	X6	283	FAD1	T15	232
FAD36	T8	282	FAD0	W19	231
FAD35	W7	281	FBP7	P3	28
FAD34	U8	280	FBP6	U2	15
FAD33	V8	279	FBP5	V4	299
FAD32	T9	278	FBP4	X5	288
FAD31	W8	275	FBP3	X7	277
FAD30	V9	274	FBP2	W12	264
FAD29	W9	273	FBP1	T12	253
FAD28	V10	272	FBP0	W16	242

Table 8 : Futurebus+ Command (FCM), Status Line (FST) and Geographical Address (GA*) Pins

Signal	CPGA	PQFP		Signal	CPGA	PQFP
FCM7	P19	203		FST4	T20	210
FCM6	N17	202		FST3	R19	208
FCM5	N18	201		FST2	P18	207
FCM4	M16	200		FST1	R20	205
FCM3	P20	199		FST0	N16	204
FCM2	N19	197		GA4*	E17	160
FCM1	M18	196		GA3*	F17	159
FCM0	N20	195		GA2*	D18	158
FST7	U20	214		GA1*	F16	157
FST6	T19	213		GA0*	C19	156
FST5	R18	211				

Table 9 : Pin Assignments for Power and Ground

V_{SS} Pins							V_{DD} Pins					
CPGA				PQFP			CPGA				PQFP	
A2	A4	A10		16	19	22	A3	A9	C9		11	25	42
A12	A19	B20		43	44	57	A11	A13	A18		50	63	81
H20	K20	M20		65	68	71	A20	C20	J20		82	95	105
W20	X19	X17		86	89	92	L20	M17	U15		112	131	144
U12	X11	X9		113	114	133	V20	X20	X18		145	171	190
U9	V1	X3		136	139	164	X12	V11	X10		198	206	229
X1	N1	L1		167	170	188	X8	W1	X2		230	234	247
J5	J1	C1		189	209	212	R4	M1	K1		259	267	284
				215	238	241	K3	D1	B1		302	303	
				244	255	265							
				266	276	287							
				290	293								

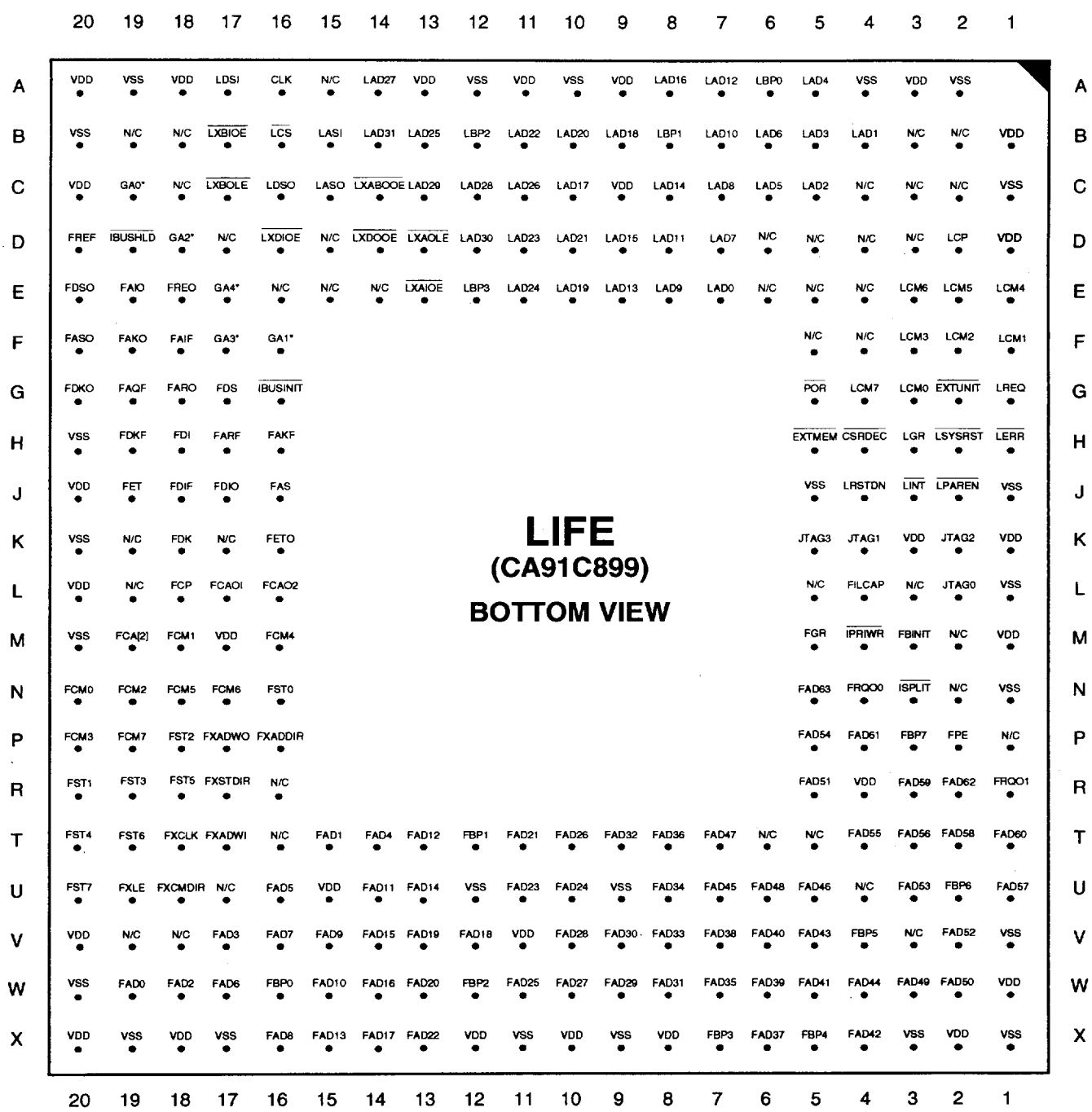


Figure 3 : Pin Configuration for the 299-CPGA Package

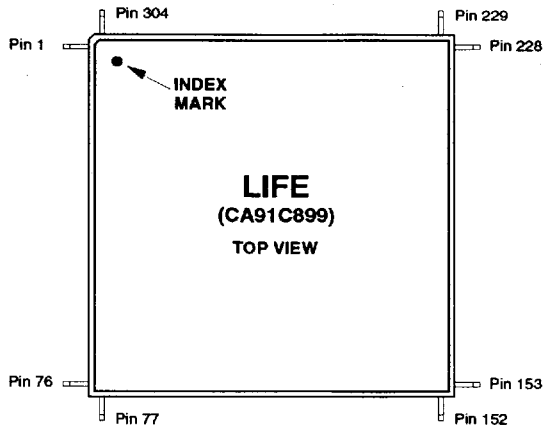
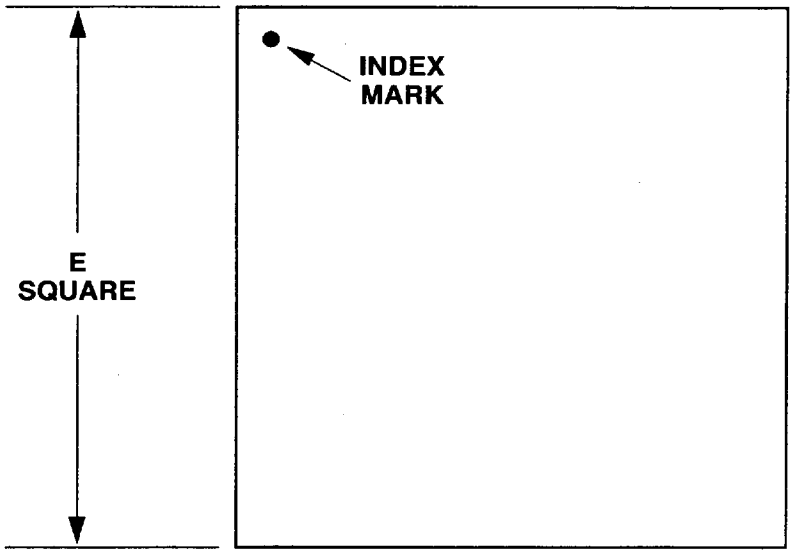


Figure 4 : Pin Configuration for 304-Pin PQFP Package

304 PIN PLASTIC QFP

1. N/C	39. N/C (RSVD)	77. N/C	115. LAD22	153. N/C	191. FCAO1	229. V_{DD}	267. V_{DD}
2. N/C	40. N/C (RSVD)	78. N/C	116. LAD23	154. N/C	192. FCAO2	230. V_{DD}	268. FAD24
3. N/C	41. FILCAP	79. N/C	117. LBP2	155. N/C	193. FCA[2]	231. FAD0	269. FAD25
4. N/C	42. V_{DD}	80. N/C	118. LAD24	156. GA0*	194. FCP	232. FAD1	270. FAD26
5. N/C	43. V_{SS}	81. V_{DD}	119. LAD25	157. GA1*	195. FCM0	233. FAD2	271. FAD27
6. N/C	44. V_{SS}	82. V_{DD}	120. LAD26	158. GA2*	196. FCM1	234. V_{DD}	272. FAD28
7. N/C	45. JTAG0	83. LAD0	121. LAD27	159. GA3*	197. FCM2	235. FAD3	273. FAD29
8. FAD50	46. JTAG1	84. LAD1	122. LAD28	160. GA4*	198. V_{DD}	236. FAD4	274. FAD30
9. FAD51	47. JTAG2	85. LAD2	123. LAD29	161. IBUSINIT	199. FCM3	237. FAD5	275. FAD31
10. FAD52	48. JTAG3	86. V_{SS}	124. LAD30	162. IBUSHLD	200. FCM4	238. V_{SS}	276. V_{SS}
11. V_{DD}	49. LPAREN	87. LAD3	125. LAD31	163. FREO	201. FCM5	239. FAD6	277. FBP3
12. FAD53	50. V_{DD}	88. LAD4	126. LBP3	164. V_{SS}	202. FCM6	240. FAD7	278. FAD32
13. FAD54	51. LERR	89. V_{SS}	127. LXAOLE	165. FREF	203. FCM7	241. V_{SS}	279. FAD33
14. FAD55	52. N/C	90. LAD5	128. LXABOOE	166. FAIO	204. FST0	242. FBP0	280. FAD34
15. FBP6	53. LINT	91. LAD6	129. LXAIOE	167. V_{SS}	205. FST1	243. FAD8	281. FAD35
16. V_{SS}	54. LSYSRST	92. V_{SS}	130. LASI	168. FAIF	206. V_{DD}	244. V_{SS}	282. FAD36
17. FAD56	55. LRSTDN	93. LAD7	131. V_{DD}	169. FDSO	207. FST2	245. FAD9	283. FAD37
18. FAD57	56. LGR	94. LBP0	132. CLK	170. V_{SS}	208. FST3	246. FAD10	284. V_{DD}
19. V_{SS}	57. V_{SS}	95. V_{DD}	133. V_{SS}	171. V_{DD}	209. V_{SS}	247. V_{DD}	285. FAD38
20. FAD58	58. LREQ	96. LAD8	134. LASO	172. FDS	210. FST4	248. FAD11	286. FAD39
21. FAD59	59. CSRDEC	97. LAD9	135. LCS	173. FAKO	211. FST5	249. FAD12	287. V_{SS}
22. V_{SS}	60. EXTUNIT	98. LAD10	136. V_{SS}	174. FAKF	212. V_{SS}	250. FAD13	288. FBP4
23. FAD60	61. EXTMEM	99. LAD11	137. LDSI	175. FARO	213. FST6	251. FAD14	289. FAD40
24. FAD61	62. LCM0	100. LAD12	138. LDSO	176. FARF	214. FST7	252. FAD15	290. V_{SS}
25. V_{DD}	63. V_{DD}	101. LAD13	139. V_{SS}	177. FASO	215. V_{SS}	253. FBP1	291. FAD41
26. FAD62	64. LCM1	102. LAD14	140. LXBIOE	178. FAS	216. FXCLK	254. FAD16	292. FAD42
27. FAD63	65. V_{SS}	103. LAD15	141. LXDIOE	179. FAQF	217. FXLE	255. V_{SS}	293. V_{SS}
28. FBP7	66. LCM2	104. LBP1	142. LXDOOE	180. FDIO	218. FXADW0	256. FAD17	294. FAD43
29. FRQO0	67. LCM3	105. V_{DD}	143. LXBOLE	181. FDI	219. FXADW1	257. FAD18	295. FAD44
30. FRQO1	68. V_{SS}	106. LAD16	144. V_{DD}	182. FDIF	220. FXADDIR	258. FAD19	296. FAD45
31. FGR	69. LCM4	107. LAD17	145. V_{DD}	183. FDKO	221. FXCMDIR	259. V_{DD}	297. FAD46
32. FPE	70. LCM5	108. LAD18	146. N/C	184. FDK	222. FXSTDIR	260. FAD20	298. FAD47
33. IPRIWR	71. V_{SS}	109. LAD19	147. N/C	185. FDKF	223. N/C	261. FAD21	299. FBP5
34. ISPLIT	72. LCM6	110. LAD20	148. N/C	186. FETO	224. N/C	262. FAD22	300. FAD48
35. FBINIT	73. LCM7	111. LAD21	149. N/C	187. FET	225. N/C	263. FAD23	301. FAD49
36. N/C (RSVD)	74. LCP	112. V_{DD}	150. N/C	188. V_{SS}	226. N/C	264. FBP2	302. V_{DD}
37. N/C (RSVD)	75. POR	113. V_{SS}	151. N/C	189. V_{SS}	227. N/C	265. V_{SS}	303. V_{DD}
38. N/C (RSVD)	76. N/C	114. V_{SS}	152. N/C	190. V_{DD}	228. N/C	266. V_{SS}	304. N/C

MECHANICALS



CONTROLLING DIMENSIONS IN In.

DIMENSION	PGA 299 CERAMIC	
	Min.	Max.
A	0.091 in.	0.111 in.
B	0.045 in.	0.055 in.
E	2.040 in.	2.080 in.
F	0.095 in.	0.105 in.
L	0.185 in.	0.195 in.
Q	0.065 in.	0.075 in.

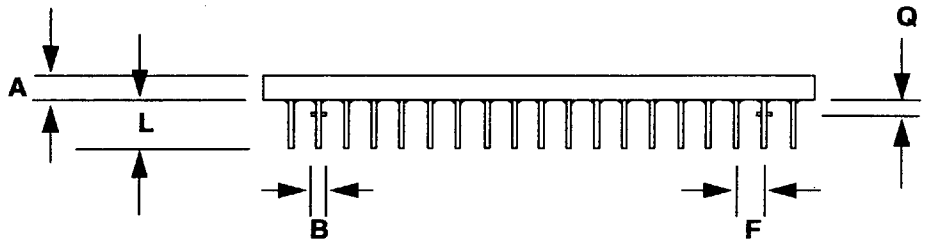
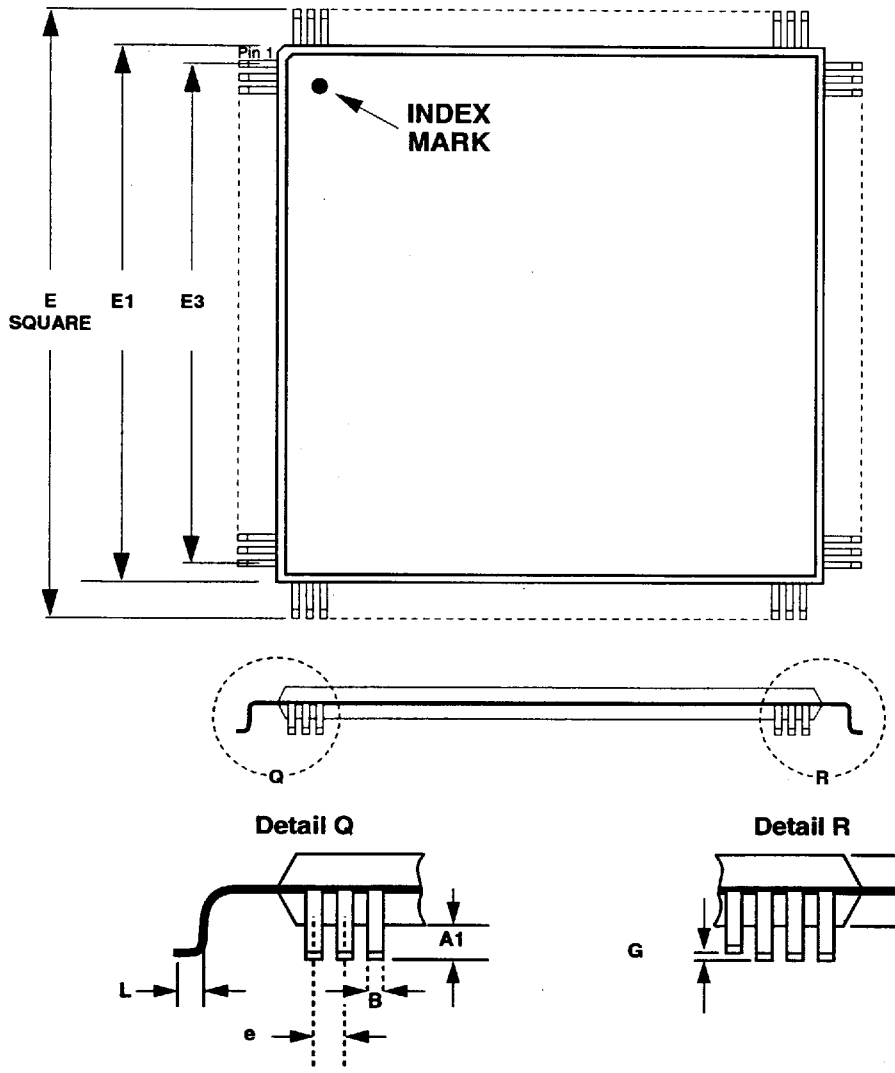


Figure 5 : Mechanical Dimensions for 299-Pin CPGA

MECHANICALS CONT'D

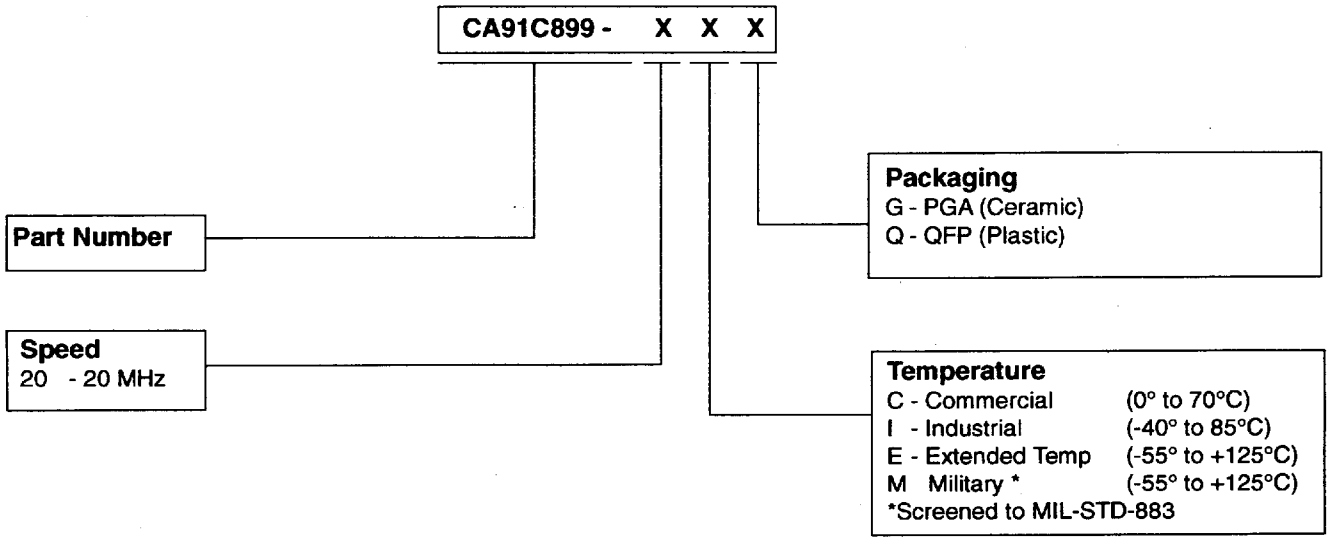


CONTROLLING DIMENSIONS IN mm

DIMENSION	304 PQFP	
	Min.	Max.
A	3.95 mm	4.25 mm
A1	0.00 mm	0.30 mm
A2	3.95 mm	
B	0.18 mm	0.27 mm
e	0.40 mm	0.60 mm
E	43.7 mm	44.3 mm
E1	39.9 mm	40.1 mm
E3	37.5 mm	
G	0.076 mm	
L	0.78 mm	0.82 mm

Figure 6 : Mechanical Dimensions for Lead-formed 304-Pin PQFP

ORDERING INFORMATION and PRODUCT CODE



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