High Speed 6-Bit A/D Converters

AD9006/AD9016

FEATURES
500MSPS Encode Rate
Very Low Input Capacitance: 8pF
30dB SNR @ 200MHz Analog Input
MIL-STD-883 Available
Bipolar Input Range (±1V)
Demultiplexed Outputs (AD9016)
MIL-STD-883-Compliant Versions Available

APPLICATIONS
Radar Warning Receivers
Electronic Countermeasures
Transient Recorders
"Smart" Munitions
Digital Oscilloscopes

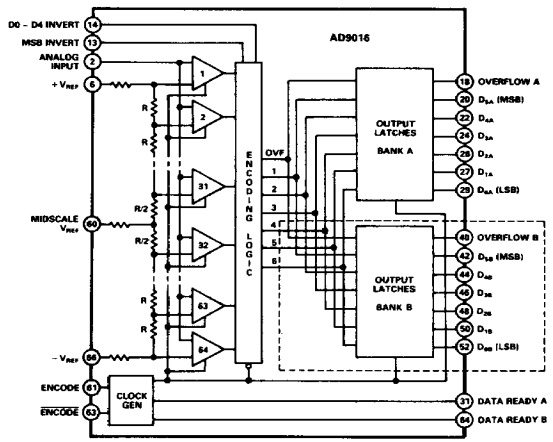
GENERAL DESCRIPTION

The AD9006 and AD9016 are 6-bit, ultrahigh speed analog-to-digital converters. Both are fabricated in an advanced bipolar process, assuring exceptionally wide analog input bandwidth, and encode rates up to 500MSPS. Functionally, the AD9006 and AD9016 use "flash" architecture; the outputs of 64 parallel comparator stages are decoded to drive a bank of ECL output latches.

The AD9006 features a bipolar analog input range (±1V). Output data is provided in a single 6-bit data bank; the data is ECL compatible and also includes complementary Data Ready signals and an overflow bit. ECL-level control pins allow the user to invert the MSB and/or LSBs. The AD9006 exhibits excellent SNR performance (30dB SNR @ 200MHz input), and requires less than two watts of power.

In the AD9016, the performance and features of the AD9006 are combined with on-board demultiplexing circuits. Output data of the AD9016 are demultiplexed to two 6-bit data banks, each of which includes a Data Ready signal and overflow bit.

FUNCTIONAL BLOCK DIAGRAM



(Dotted Area Not Included in AD9006)

The AD9006 and AD9016 are available as commercial temperature range devices: 0 to +70°C; and military temperature range devices: −55°C to +125°C. Both versions are offered in a ceramic 68-pin LCC, and a ceramic 68-pin leaded package.

The AD9006/AD9016 are available in versions compliant with MIL-STD-883. Refer to the *Analog Devices Military Products Databook* or current AD9006/AD9016/883B data sheet for detailed specifications

AD9006/AD9016—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ to Ground . . . . . −0.5V dc to +7.0V dc
AGND to DGND . . . . . −0.5V dc to +0.5V dc
$-V_S$ to Ground . . . . . +0.5V dc to −6.0V dc
ANALOG IN, $+V_{REF}-V_{REF}$ . . . . . −1.5V to +1.5V
MIDSCALE V_{REF}[2]
$+V_{REF}$ to $-V_{REF}$ 2.1V
MIDSCALE V_{REF} Current . . . . . ±4mA
Digital Input Voltages . . . . . $-V_S$ to 0V
ENCODE to $\overline{\text{ENCODE}}$ 4V
Digital Output Current 20mA
HYSTERESIS Input . . . . . $-V_S$ to +3V
ANALOG $-V_S$ to DIGITAL $-V_S$ . . . . . ±0.5V
Operating Temperature Range
AD9006/AD9016KE/KZ . . . . . 0 to +70°C
AD9006/AD9016TE/TZ/883 . . . . . −55°C to +125°C
Maximum Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS ($+V_S = +5.0V$; $-V_S = -5.2V$; $+V_{REF} = +1V$; $-V_{REF} = -1V$, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9006/AD9016KE AD9006/AD9016KZ Min	Typ	Max	Units
RESOLUTION			6			Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.2	0.25	LSB
	Full	VI		0.25	0.5	LSB
Integral Nonlinearity	+25°C	I		0.2	0.25	LSB
	Full	VI		0.25	0.5	LSB
No Missing Codes	Full	VI		GUARANTEED		
INITIAL OFFSET ERROR						
Top of Reference Ladder	+25°C	I		15	20	mV
	Full	VI			20	mV
Bottom of Reference Ladder	+25°C	I		14	20	mV
	Full	VI			20	mV
Offset Drift Coefficient	Full	V		20		µV/°C
ANALOG INPUT						
Input Voltage Range	Full	V		±1		V
Input Bias Current[4]	+25°C	I		60	100	µA
	Full	VI			130	µA
Input Resistance	+25°C	III	25	70		kΩ
Input Capacitance	+25°C	III		8	10	pF
Analog Bandwidth[5]	+25°C	V		550		MHz
REFERENCE INPUT						
Reference Ladder Resistance	+25°C	I	64	80	110	Ω
	Full	VI	50		135	Ω
Ladder Temperature Coefficient	Full	V		0.24		Ω/°C
Reference Input Bandwidth	Full	V		30		MHz
DYNAMIC PERFORMANCE[6]						
Conversion Rate	+25°C	I	470	500		MSPS
Aperture Delay (t_A)	+25°C	V		1.2		ns
Aperture Uncertainty (Jitter)	+25°C	V		3		ps
Output Delay (t_{OD})[7]	+25°C	I	2.7	3.6	4.4	ns
Output Rise Time	+25°C	I		1.3	1.5	ns
Output Fall Time	+25°C	I		1.3	1.5	ns
Output Time Skew[8]	+25°C	I		0.45	0.7	ns
Data Ready Output Delay (t_{DR})[9]						
AD9006	+25°C	I	2.7	3.2	4.4	ns
AD9016	+25°C	I	3	3.6	4.7	ns
Transient Response[10]	+25°C	V		1		ns
Overvoltage Recovery Time[11]	+25°C	V		1		ns

Parameter (Conditions)	Temp	Test Level	AD9006/AD9016KE AD9006/AD9016KZ Min	Typ	Max	Units
ENCODE INPUT						
Logic "1" Voltage	Full	VI	−1.1			V
Logic "0" Voltage	Full	VI			−1.5	V
Logic "1" Current	Full	VI			400	μA
Logic "0" Current	Full	VI			200	μA
Input Capacitance	+25°C	V		3		pF
Encode Pulse Width[12]	+25°C	I	1.0			ns
AC LINEARITY[13]						
Effective Number of Bits (ENOB)						
Analog Input @ 49MHz	+25°C	I	5.2	5.5		Bits
Analog Input @ 196MHz	+25°C	I	4.4	5.0		Bits
In-Band Harmonics						
Analog Input @ 9.3MHz	+25°C	I	42	48		dBc
Analog Input @ 49MHz	+25°C	I	38	44		dBc
Analog Input @ 92MHz	+25°C	I	33	36		dBc
Analog Input @ 145MHz	+25°C	I	33	36		dBc
Analog Input @ 196MHz	+25°C	I	31	36		dBc
Signal-to-Noise Ratio[14]						
(With Harmonics)						
Analog Input @ 9.3MHz	+25°C	I	34	37		dB
Analog Input @ 49MHz	+25°C	I	30	35		dB
Analog Input @ 92MHz	+25°C	I	30	34		dB
Analog Input @ 145MHz	+25°C	I	30	33		dB
Analog Input @ 196MHz	+25°C	I	29	32		dB
Signal-to-Noise Ratio[14]						
(Without Harmonics)						
Analog Input @ 9.3MHz	+25°C	I	36	37		dB
Analog Input @ 49MHz	+25°C	I	33	36		dB
Analog Input @ 92MHz	+25°C	I	33	36		dB
Analog Input @ 145MHz	+25°C	I	33	35		dB
Analog Input @ 196MHz	+25°C	I	31	34		dB
Two-Tone Intermodulation Distortion Rejection[15]	+25°C	V		50		dB
DIGITAL OUTPUTS[6]						
Logic "1" Voltage	Full	VI	−1.1			V
Logic "0" Voltage	Full	VI			−1.5	V
POWER SUPPLY (AD9006)						
Positive Supply Current	+25°C	I		25	29	mA
($+V_S$ = +5.0V)	Full	VI			30	mA
Negative Supply Current	+25°C	I		320	380	mA
($-V_S$ = −5.2V)	Full	VI			395	mA
Nominal Power Dissipation	+25°C	V		1.7		W
Reference Ladder Dissipation	+25°C	V		50		mW
Power Supply Rejection Ratio[16]	Full	VI		2	4	mV/V
POWER SUPPLY (AD9016)						
Positive Supply Current	+25°C	I		25	29	mA
($+V_S$ = +5.0V)	Full	VI			30	mA
Negative Supply Current	+25°C	I		375	420	mA
($-V_S$ = −5.2V)	Full	VI			450	mA
Nominal Power Dissipation	+25°C	V		2.0		W
Reference Ladder Dissipation	+25°C	V		50		mW
Power Supply Rejection Ratio[16]	Full	VI		2	4	mV/V

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]$+V_{REF} > -V_{REF}$ under all circumstances.
[3]Typical thermal impedances:
68-pin leaded ceramic chip carrier θ_{JA} = 31°C/W; θ_{JC} = 1.1°C/W.
68-pin ceramic LCC θ_{JA} = 36°C/W; θ_{JC} = 2.6°C/W.
[4]Measured with analog input = 0V.
[5]Measured with use of Fast Fourier Transform (FFT). See Definitions.
[6]Outputs terminated through 100Ω to −2.0V; C_L < 4pF
[7]Measured from 50% point of leading edge of ENCODE command to −1.3V point of output data.
[8]Output time skew includes HIGH-to-LOW and LOW-to-HIGH transitions as well as bit-to-bit time skew differences.
[9]Measured from 50% point of trailing edge of ENCODE command to 50% point of Data Ready pulse.
[10]For full scale step input, 6-bit accuracy is attained in the specified time.
[11]Recovers to 6-bit accuracy in specified time after 150% full scale input overvoltage.
[12]ENCODE command rise/fall times should be less than 2.5ns for normal operation.
[13]Measured at 400MSPS encode rate; input level 1.0dB below full scale (FS).
[14]RMS signal to rms noise with analog input signal of 1dB below full scale at specified frequency.
[15]Intermodulation measured with analog input frequencies of 60MHz and 70MHz at 7dB below full scale.
[16]Measured at $+V_S$ = +5.0V ±5% or $-V_S$ = −5.2V ±5%; specification shown is for worst case (see Definitions).
Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

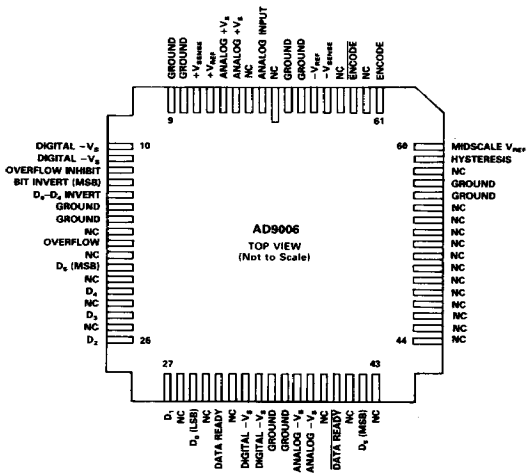
Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

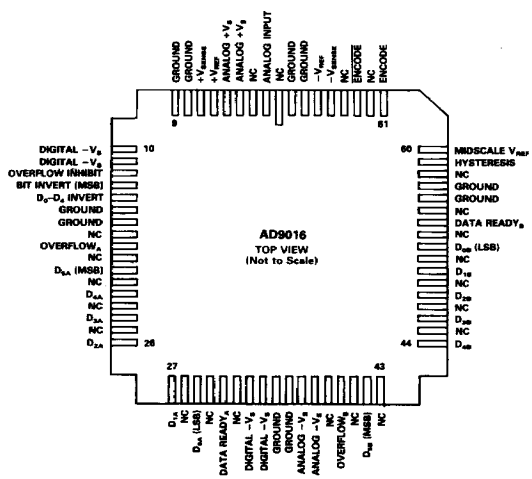
ORDERING GUIDE

Model[1]	Temperature	Description	Package Option[2]
AD9006KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9006KZ	0 to +70°C	68-Pin Leaded Ceramic Chip Carrier	Z-68
AD9016KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9016KZ	0 to +70°C	68-Pin Leaded Ceramic Chip Carrier	Z-68
AD9016KE/PCB	0 to +70°C	Evaluation Board; AD9016KE Installed	
AD9016/PCB	0 to +70°C	Evaluation Board; No Converter	

NOTES
[1]MIL-STD-883 versions available; contact factory.
[2]E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.



AD9006 Pin Designations



AD9016 Pin Designations

AD9006/AD9016 PIN DESCRIPTIONS

NC — Not internally connected.

ANALOG IN — Analog input connection. Analog input is nominally between −1.0V and +1.0V.

ANALOG $+V_S$ — Positive supply pins; nominally +5.0V.

$+V_{REF}$ — The positive reference voltage applied to the internal resistor ladder.

$+V_{SENSE}$ — Voltage sense line to the most positive reference voltage of the resistor ladder. The sense line is intended for connection to a high impedance node and has limited current capability. It is intended to be used to null offset at the top of the reference ladder.

GROUND — Analog and digital ground connections for the AD9006/AD9016 units. For optimum performance, all grounds should be connected together and to a low impedance ground plane as close to the device as possible. [NOTE: On both the AD9006 and the AD9016, Pins 8, 9, 15, 16, 35, 36, 56 and 57 are digital ground (DGND); pins 67 and 68 are analog ground (AGND).]

OVERFLOW INHIBIT — Overflow bit control pin. OVERFLOW INHIBIT is connected to ground for normal operation (no overflow bit, nonreturn-to- zero operation). When overflow inhibit is connected to −5.2V or allowed to float, OVERFLOW = HIGH and output bits = LOW when the analog input voltage exceeds $+V_{SENSE}$).

BIT INVERT (MSB) — Most significant bit (D_{05}) control pin. BIT INVERT (MSB) is connected to ground for normal operation. When connected to −5.2V or allowed to float, MSB output is inverted.

D_0–D_4 INVERT — Bits D_0–D_4 control pin, connected to ground for normal operation. When connected to −5.2V or allowed to float, D_0–D_4 data outputs are inverted.

$OVERFLOW_A$ — AD9016 only. Overflow data output for Data Bank "A." Logic HIGH indicates the analog input is greater than $+V_{SENSE}$ when OVERFLOW INHIBIT pin is LOW (−5.2V).

D_{5A} — AD9016 only. Most significant bit (MSB) digital data output of Data Bank "A."

D_{1A}–D_{4A} — AD9016 only. D_{1A} through D_{4A} digital data outputs from Data Bank "A."

D_{0A} — AD9016 only. Least significant bit (LSB) digital data output of Data Bank "A."

$DATA\ READY_A$ — AD9016 only. Output Data of Bank "A" are valid at the rising edge of the DATA $READY_A$ pulse. Bank "A" carries every other sample of the A/D conversion; Bank "B" carries the remaining samples.

DIGITAL $-V_S$ — Negative digital supply pins, nominally −5.2V.

ANALOG $-V_S$ — Negative analog supply pins, nominally −5.2V.

$OVERFLOW_B$ — AD9016 only. Overflow data output for Data Bank "B." Logic HIGH indicates analog input is greater than $+V_{SENSE}$ when OVERFLOW INHIBIT pin is LOW (−5.2V).

D_{5B} — AD9016 only. Most significant bit (MSB) digital data output of Data Bank "B."

D_{1B}–D_{4B}	AD9016 only. D_{1B} through D_{4B} digital data outputs of Data Bank "B."
D_{0B}	AD9016 only. Least significant bit (LSB) digital data output of Data Bank "B."
DATA $READY_B$	AD9016 only. Output data of Bank "B" are valid at the rising edge of the DATA $READY_B$ pulse. Bank "B" carries every other sample of the A/D conversion; Bank "A" carries the remaining samples.
HYSTERESIS	The hysteresis control voltage varies the amount of hysteresis in the internal comparators. This pin normally floats at −3.17V; making pin more positive increases the hysteresis of the internal comparators.
MIDSCALE V_{REF}	The midpoint tap on the internal reference ladder; can be connected to an external voltage to improve integral linearity of the A/D converter.
ENCODE	ECL-compatible noninverted input of the encode command. The conversion cycle begins on the rising edge of the ENCODE signal.
$\overline{\text{ENCODE}}$	ECL-compatible inverted input of the encode command, used when a differential encode signal is used. $\overline{\text{ENCODE}}$ should be tied to a voltage corresponding to the midpoint of the encode signal when a single-ended encode signal is used.
$-V_{SENSE}$	Voltage sense line to the most negative reference voltage of the resistor ladder. The sense line is intended for connection to a high impedance node and has limited current capability. It is intended to be used to null offset at the bottom of the reference ladder.
$-V_{REF}$	The negative reference voltage applied to the internal resistor ladder.
D_0	AD9006 only. Least significant bit (LSB) of the output data.
D_1–D_4	AD9006 only. D_1 through D_4 digital data outputs.
D_5	AD9006 only. Most significant bit (MSB) of digital data output.
OVERFLOW	AD9006 only. Overflow data output. Logic HIGH indicates the analog input is greater than $+V_{SENSE}$ when OVERFLOW INHIBIT pin is LOW (−5.2V).
DATA READY	AD9006 only. Output data are valid at the rising edge of the DATA READY pulse.
$\overline{\text{DATA READY}}$	AD9006 only. Output data valid at the falling edge of the $\overline{\text{DATA READY}}$ pulse.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3dB.

Aperture Delay (t_A)
The delay between the rising edge of the ENCODE command (or falling edge of $\overline{\text{ENCODE}}$) and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Data Ready Output Delay (t_{DR})
The delay between the 50% point of the falling edge of the ENCODE command (or rising edge of $\overline{\text{ENCODE}}$) and the −1.3V point of the leading edge of the DATA READY pulse.

Differential Nonlinearity
The deviation of any code from an ideal 1LSB step.

Effective Number of Bits (ENOB)
Signal-to-noise ratio (see definition below) is expressed in dB; but can also be expressed in Effective Number of Bits (ENOB) if ENOB is related to full scale inputs as follows:

$$\text{ENOB} = (\text{SNR} - 1.78)/6.02$$

ENOB is calculated with a sine wave curve fit method.

In-Band Harmonics
The rms value of the fundamental divided by the rms value of the worst of the first six harmonics.

Integral Nonlinearity
This specification (often called "linearity error") is the deviation of the transfer function from a reference line and is expressed in either % or ppm of full scale range, or in fractions of 1LSB. In the AD9006 and AD9016 devices, this spec is measured in fractions of 1LSB and uses a best-fit straight line determined by a least square curve fit.

Output Delay (t_{OD})
The delay between the 50% point of the rising edge of the ENCODE command (or falling edge of $\overline{\text{ENCODE}}$) and the −1.3V point of output data.

Output Time Skew
Bit-to-bit time variations among Bits D_0 to D_5 and the overflow bit. In the AD9006 and AD9016 specifications, time skew includes HIGH-to-LOW and LOW-to-HIGH transitions of the digital output bits.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 6-bit accuracy after an analog input overvoltage signal of 150% is reduced to the valid range of the converter.

Pipeline Delay
This is equal to one clock cycle and is the delay between the 50% points on the rising edges of two successive ENCODE commands (or falling edges of $\overline{\text{ENCODE}}$ commands).

Power Supply Rejection Ratio
The ratio of the change in power supply voltage to a corresponding change in input offset voltage. In the AD9006 and AD9016 units, $+V_S$ (+5V) or $-V_S$ (−5.2V) are within ±5% of their nominal values for this test. Value shown in SPECIFICATIONS is worst case.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise", which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1dB below full scale.

Transient Response
The time required for the converter to achieve 6-bit accuracy when a full scale step function input is applied to the unit.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of a two-tone signal to the power of the strongest third-order IMD signal.

RECOMMENDED OPERATING CONDITIONS

Parameter	Input Voltage		
	Min	Nominal	Max
$+V_S$	+4.75	+5.00	+5.25
$-V_S$	−5.46	−5.20	−4.94
$+V_{REF}$	$-V_{REF}$	+1.0	+1.1
$-V_{REF}$	−1.1	−1.0	$+V_{REF}$
ANALOG INPUT	−1.0		+1.0

THEORY OF OPERATION

Refer to the block diagram of the AD9016 A/D converter.

"Flash" architecture used in the AD9006 and AD9016 units makes it unnecessary to use a track-and-hold (T/H) ahead of the converter in many applications. The analog input signal is impressed across 64 parallel comparator stages.

Bias points of these comparators are established by the voltages applied to the reference ladder via $+V_{REF}$, $MIDSCALE_{REF}$ and $-V_{REF}$.

The outputs of the comparators are applied to the decoding logic; from here, the data are applied to output latches as six bits of digital data and an overflow bit. The overflow bit can be used to stack converters to obtain additional bits of resolution and can also be used as a "flag" for indicating positive out-of-range inputs.

Capturing output data at the (guaranteed) encode rates of 470MSPS of the AD9016 is simplified by virtue of using two Data Ready pulses. Output data words alternate between Bank A and Bank B; this allows clocking demultiplexed data from the AD9016 at half the converter's sample rate.

The Data Ready pulses track the propagation delay of the output data and relieve the need to build an external clock circuit for tracking prop delay over the full operating temperature range.

Demultiplexed ports connected to Bank A and Bank B allow the user to capture output data with 100K ECL logic even when the converter is operating at 470MSPS. The AD9016 introduces only one pipeline delay in the processing of these digital output data, thereby reducing the number of clock cycles required to obtain the digital representation of the analog input at the appropriate output port.

The analog input voltage range is determined by the user-supplied voltage references: $+V_{REF}$ and $-V_{REF}$. The references can be adjusted between −1V and +1V. In all cases, $+V_{REF}$ should be greater than $-V_{REF}$; and the differential voltage between the references should not exceed 2.1V. MIDSCALE V_{REF} can be used to improve the integral linearity of the converter.

Another attractive feature of the analog input characteristics of the AD9016 is its low input capacitance of 8pF. In many other flash converters, this value is three or four times larger, making them difficult to drive at high input frequencies.

For those applications in which a single output port is preferred, the recommended choice is the AD9006 A/D converter.

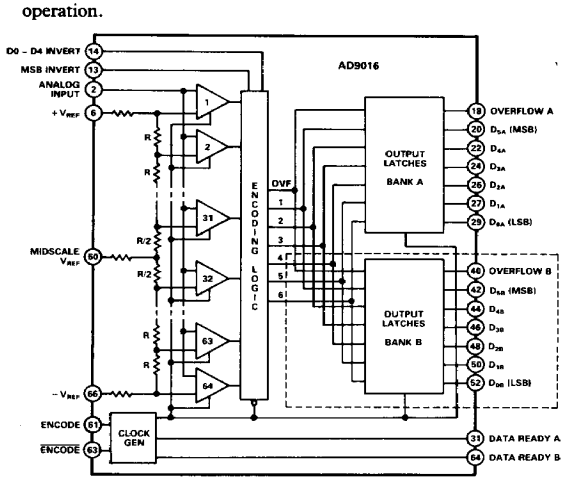
The AD9006 is identical to the AD9016 in performance specifications; it is best suited for systems in which demultiplexing is not performed immediately after the flash converter. As in the AD9016, the AD9006 produces Data Ready pulses on chip; these can be used to clock external latches.

There are two control pins for determining the format of the output data on the AD9006/AD9016. BIT INVERT (MSB) allows the user to invert the most significant bit ($D0_5$); and D_0–D_4 INVERT allows the five least significant bits to be inverted. The AD9006/AD9016 Truth Table elsewhere in the data sheet provides the necessary information to select among binary, inverted binary, twos complement and inverted twos complement coding schemes.

The OVERFLOW INHIBIT pin controls the overflow bit (called out as OVERFLOW BIT in the AD9006, and $OVERFLOW_A$ and $OVERFLOW_B$ in the AD9016). In normal operation, the OVERFLOW INHIBIT is connected to −5.2V, and OVERFLOW will be a digital HIGH whenever the analog input voltage exceeds the most positive comparator reference ($+V_{SENSE}$). The digital outputs (D_0– D_5) will be LOW, i.e., returned-to-zero operation.

This feature means two AD9006 devices can be cascaded or "stacked" to obtain seven-bit operation, as shown in the diagram below.

Connecting OVERFLOW INHIBIT to ground forces the overflow bit to remain low and disables the return-to-zero operation.

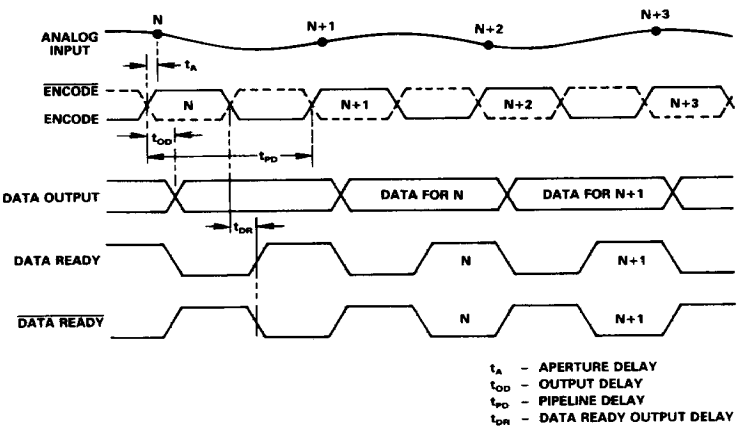


AD9016 Functional Block Diagram
(Dotted Area Not Included in AD9006)

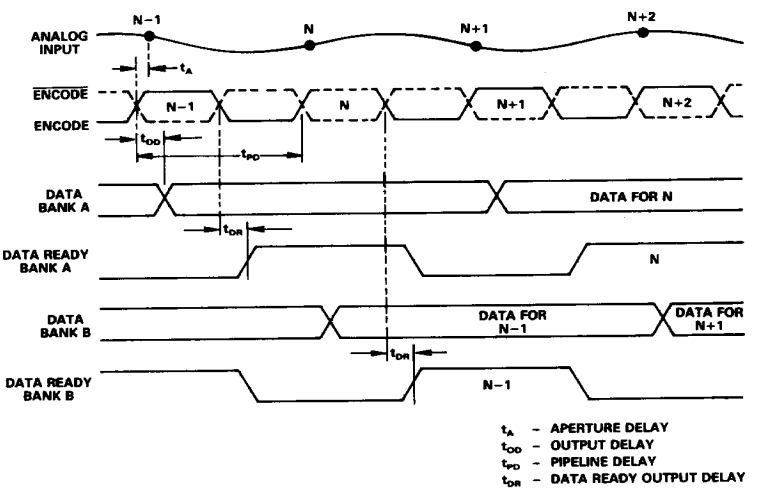
Timing for the AD9006 and AD9016 is shown in their respective timing diagrams. In both illustrations, the complementary encode command is shown in dashed lines.

The DATA READY and $\overline{\text{DATA READY}}$ pulses of the AD9006 correspond, respectively, to the DATA READY BANK A and DATA READY BANK B pulses of the AD9016. As shown in the SPECIFICATIONS table, Data Ready Output Delay is slightly different in the two units: 3.2ns in the AD9006 and 3.6ns in the AD9016.

Availability and timing of a DATA READY pulse help in retrieving data from either the AD9006 or the AD9016. When setting system timing, the user simply takes into account the (single) pipeline delay and the Data Ready Output Delay (3.2ns in the AD9006; 3.6ns in the AD9016) and uses the next DATA READY (or $\overline{\text{DATA READY}}$ in the AD9006) to strobe the desired output into external circuits.



AD9006 Timing Diagram



AD9016 Timing Diagram

APPLYING THE AD9006/AD9016

Setting Reference Levels

The AD9006/AD9016 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$. These two voltages are applied across the internal resistor ladder (nominally 80Ω) and determine the analog input range of the converter.

Care should be taken to assure that these references are driven from stable, low impedance sources. Reference connections should be capacitively coupled to ground to reduce interference generated by noise and/or digital switching.

Resistance between the reference connections and the point at which the first comparator threshold is connected causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled out using the $+V_{SENSE}$ and $-V_{SENSE}$ connections. These sense lines are intended for connection only to high impedance (low current) nodes such as the input of an op amp.

Applying a voltage greater than 2.1V across the internal resistor ladder will cause current densities to exceed rated values and may cause permanent damage to the AD9006/AD9016. The amount of current available at the reference connections must be limited.

One method of nulling the offset errors is shown in Figure 1.

The Analog Devices AD1403 voltage reference supplies a stable 2.5V reference for the circuit, and R_{LIMIT} determines the range over which the reference can be adjusted. R_1 adjusts the voltage at the top of the internal reference ladder through the AD642/2N3904 combination. Feedback from the $+V_{SENSE}$ line causes the op amp to compensate for offset which appears at the top comparator threshold. The transistor limits the amount of current drawn directly from the op amp; resistors at the base and emitter of the transistor stabilize its operation.

Voltage at the bottom of the reference ladder is controlled in essentially the same way, using R_2 to adjust the reference ladder voltage; and using feedback from the $-V_{SENSE}$ connection to null any offset between the reference and the threshold of the bottom comparator.

The midpoint of the comparator reference ladder (MIDSCALE V_{REF}) is shown tied to ground in Figure 1. This allows the user to adjust the voltage reference for minimum integral nonlinearity. This feature becomes important in applications with reduced analog input ranges because integral nonlinearity increases under these conditions.

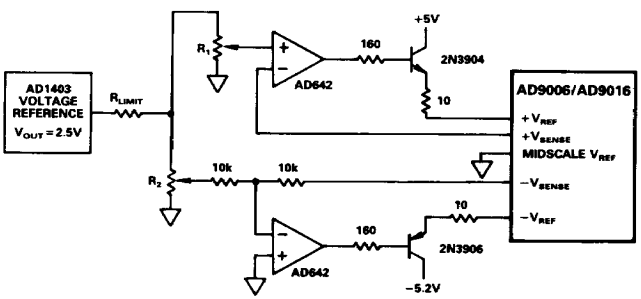


Figure 1. Reference Circuit

Driving the Analog Input

Careful design and layout of the AD9006/AD9016 have resulted in a typical input capacitance of 8pF (9.5pF max). This is low in comparison to most flash converters, but it is still a significant load at high input frequencies and must be taken into account when choosing a drive amplifier.

DC-coupled applications require the performance characteristics of a wide bandwidth, low distortion op amp such as the Analog Devices AD9611. AC-coupled applications at high frequencies may be better served by using a low distortion gain block for the driver.

Figure 2 illustrates possible connections for both approaches.

Regardless of which driving circuit is selected for the application, the overall dynamic performance of the amplifier is enhanced by inserting a small series resistor between the output of the amplifier and the analog input of the converter.

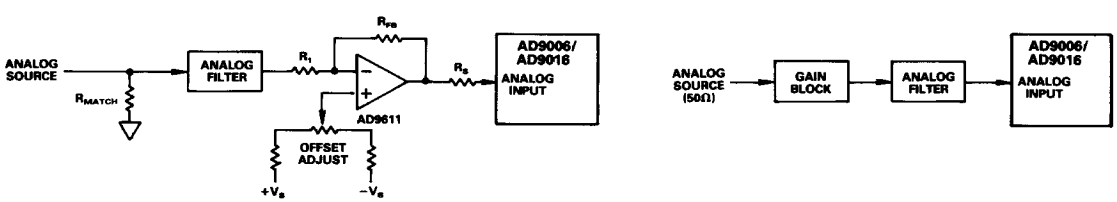


Figure 2. Analog Input Circuits

Clocking the Converter

The encode command circuits of the AD9006/AD9016 (ENCODE and $\overline{\text{ENCODE}}$) are designed to be driven by a differential ECL source.

A differential signal is recommended as the encode command to reduce jitter of the encode signal; increased jitter raises the noise floor of the converter. Full logic levels are preferred for triggering the clock circuits, but reduced levels can also be used. Caution should be exercised when using reduced-level encode commands because their slew rates will be decreased, which can raise the noise floor.

Refer again to the timing diagrams for the AD9006 and AD9016.

The rising edge of the ENCODE signal initiates the conversion process in the AD9006 unit. This same signal, delayed, becomes the DATA READY and complementary $\overline{\text{DATA READY}}$ pulses. Fast rise and fall times (<0.5ns) and "clean" edges are always required for encode commands, but are especially critical for high frequency analog signals.

In the AD9016, the leading edges of the DATA READY_A and DATA READY_B pulses are triggered by the trailing edge of an ENCODE command. Their trailing edges are triggered by the trailing edge of the next ENCODE command.

Although the AD9006/AD9016 is designed and tested to operate with a 50% duty cycle, the dynamic performance at high encode rates can be improved by changing the duty cycle.

Two possible methods of clocking the AD9006/AD9016 are shown in Figure 3. Users planning to implement these circuits need to be aware they may not function over the same temperature ranges possible with the converters.

Both ECL oscillators and saw filter oscillators are available as comercial products, with each type operating at some preselected frequency. The type of oscillator which is selected is a function of the desired operating frequency for the circuit being designed.

Layout and Power Supplies

Correct layout of high speed circuits is always critical, but is particularly important when both analog and digital signals are involved.

Analog signal paths should be kept as short as practical, and be properly terminated to avoid reflections and signal distortions. The analog input and voltage references should be kept away from digital signal paths; this reduces the possibility of capacitively coupling digital switching noise into the analog section of the circuit.

Digital signal paths should also be kept short, and digital run lengths should be matched because propagation delays through digital paths become significant at high data rates. Proper ECL terminations should be used at or near the packages containing successive gates.

Ideally, analog signal paths and digital signal paths should be routed as far away from one another as possible and should never closely parallel one another's paths. If they must cross, they should do so at right angles to avoid interference.

In any layout of high speed circuits, the layout of ground connections is the most important factor. To reduce noise and interference on the circuit ground, a double-sided copper-clad printed circuit board (PCB) is recommended. Every part of the board not used for components or conducting runs should be ground plane. Components are mounted on one side; the opposite side is used for power and signal connections.

It is especially important to retain the continuity of the ground plane under and around the AD9006/AD9016 converter. If the system design separates the digital and analog ground returns, both should be connected together and to ground close to the unit to form a continuous ground plane around the A/D section of the system.

Low noise, low ripple temperature-stable linear power supplies are the preferred choices for high speed circuits. Switching power supplies often seem to meet these criteria, including ripple specifications. *But ripple specs are generally expressed in terms of rms* – and the spikes generated in switchers can produce hard-to-filter, uncontrollable noise peaks with amplitudes of several hundred millivolts. Their high frequency components may be extremely difficult to keep out of the ground system.

If switching power supplies cannot be avoided for high speed designs, they should be *carefully* shielded and their outputs should be well filtered.

Figure 3. Clock Circuits

Every power supply line leading into a high speed PCB or data acquisition circuit must be carefully bypassed to its ground return to prevent noise from entering the circuit. Ceramic capacitors, ranging in value from 0.01μF to 0.1μF, should be used generously in the layout, mounted as closely as possible to the device or circuit being bypassed.

The capacitors which are used should have a high resonant frequency to insure they maintain their characteristics in the range of frequencies involved in the encoding process. Ceramic surface mount (chip) capacitors meet that requirement and are easily placed near the package connections.

At least one high quality tanatalum capacitor of 3μF– 20μF should be assigned to each power supply voltage, mounted as near as possible to the incoming power pins to minimize low frequency ripple.

Handling the AD9006/AD9016 Package

Several precautions have been included in the design of the AD9006/AD9016 converter to help reduce its sensitivity to electrostatic discharge (ESD). But the user should always use normal ESD precautions to help insure device reliability and avoid degrading the unit's performance.

Package options which are available include both leaded and leadless 68-pin ceramic chip carriers; these are shown in the data sheet as leaded ceramic chip carrier and leadless chip carrier (LC), respectively. Both of these packages have been specially designed to maintain the converter's high frequency parameters while operating over a standard military temperature range.

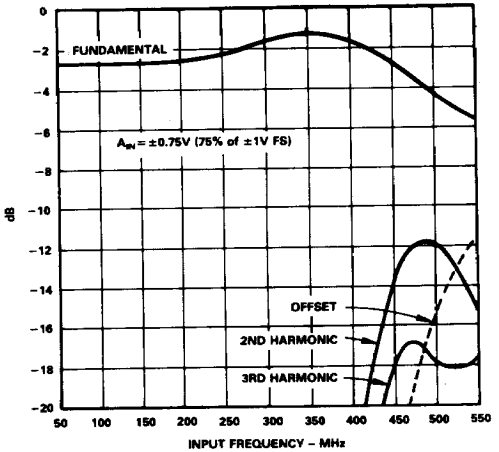
Regardless of package type, the top of the package (containing the model number and the Analog Devices logo) is internally connected to the device substrate and is designed to be used as a heat sink. The substrate is connected to $-V_S$ internally; therefore the top of the package should be allowed to "float" in voltage. The bottom of the package is not connected internally on the device.

High speed devices such as the AD9006/AD9016 converters should be soldered into final applications. There is a temptation to use sockets, but they can limit dynamic performance and should be used only for evaluation or prototype applications.

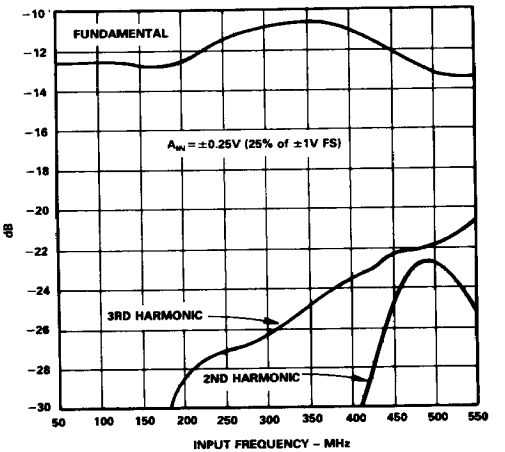
Step	Input Voltage (FS =±1.0V)	Binary True	Binary Inverted	Offset Twos Complement True	Offset Twos Complement Inverted
		MSB INVERT =1 D_0–D_4 INV =1	MSB INVERT =0 D_0–D_4 INV =0	MSB INVERT =0 D_0–D_4 INV =1	MSB INVERT =1 D_0–D_4 INV =0
00	−1.000	000000	111111	100000	011111
01	−0.968	000001	111110	100001	011110
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
31	−0.031	011111	100000	111111	000000
32	0.000	100000	011111	000000	111111
33	+0.031	100001	011110	000001	111110
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
62	+0.938	111110	000001	011110	100001
63	+0.969	111111	000000	011111	100000
63+	+1.000	(0)111111* (1)000000#	(0)000000* (1)111111#	(0)011111* (1)100000#	(0)100000* (1)011111#

*OVERFLOW INHIBIT ="1"; #OVERFLOW INHIBIT ="0."
The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT, D_0–D_4 INVERT and OVERFLOW INHIBIT are considered dc controls. They are tied to ground for logic "1" and $-V_S$ for logic "0"; their "trip point" occurs at approximately −1.3V.

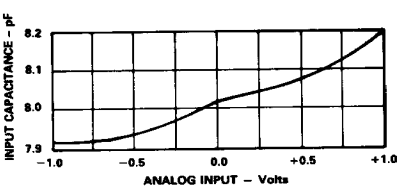
AD9006/AD9016 Truth Table



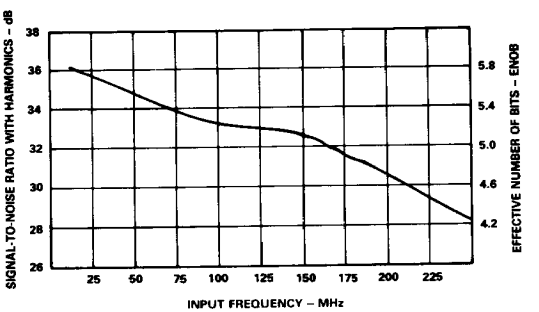
Harmonics vs. Input Frequency – Large Signal



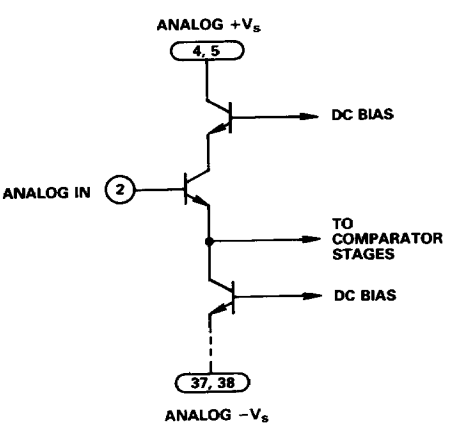
Harmonics vs. Input Frequency – Small Signal



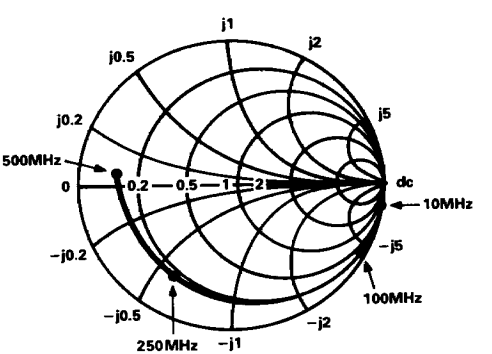
Input Capacitance vs. Input Voltage



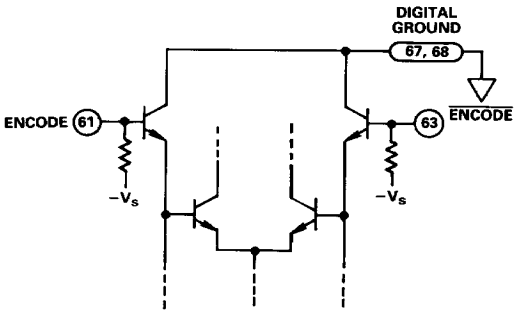
SNR and Effective Number of Bits (ENOB) vs. Input Frequency



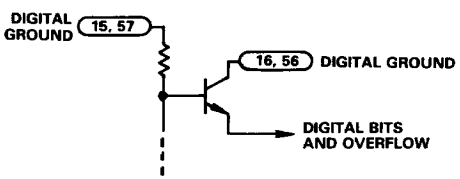
Equivalent Analog Input



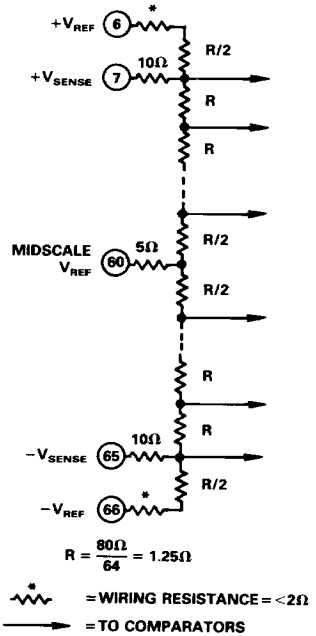
Normalized 50Ω Input Impedance vs. Input Frequency



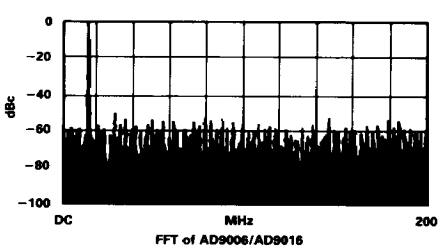
Encode and $\overline{\text{Encode}}$ Equivalent Circuits



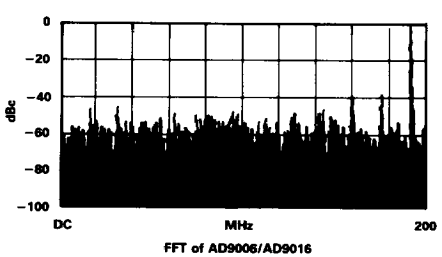
Equivalent Digital Outputs



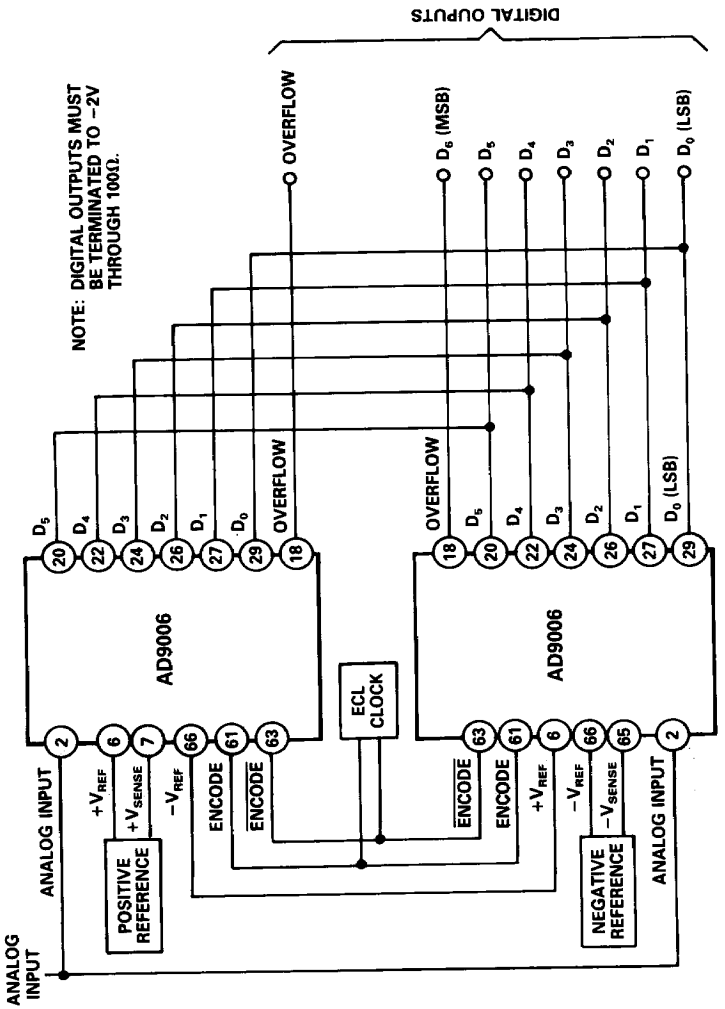
Reference Ladder



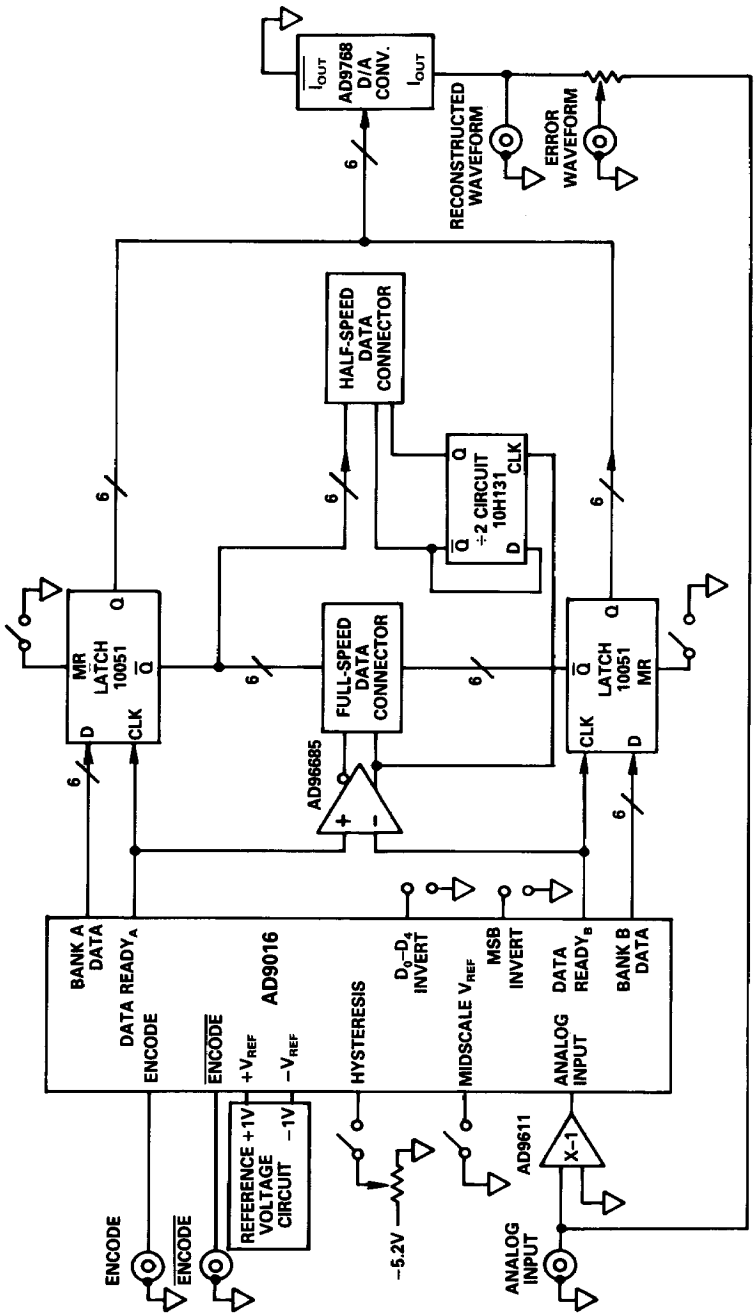
400MSPS: F_{IN} = 14.8MHz; V_{IN} = 1.0dB Below FS



400MSPS: F_{IN} = 192MHz; V_{IN} = 1.0dB Below FS



Connections for 7-Bit Operation



AD9016/PCB Block Diagram

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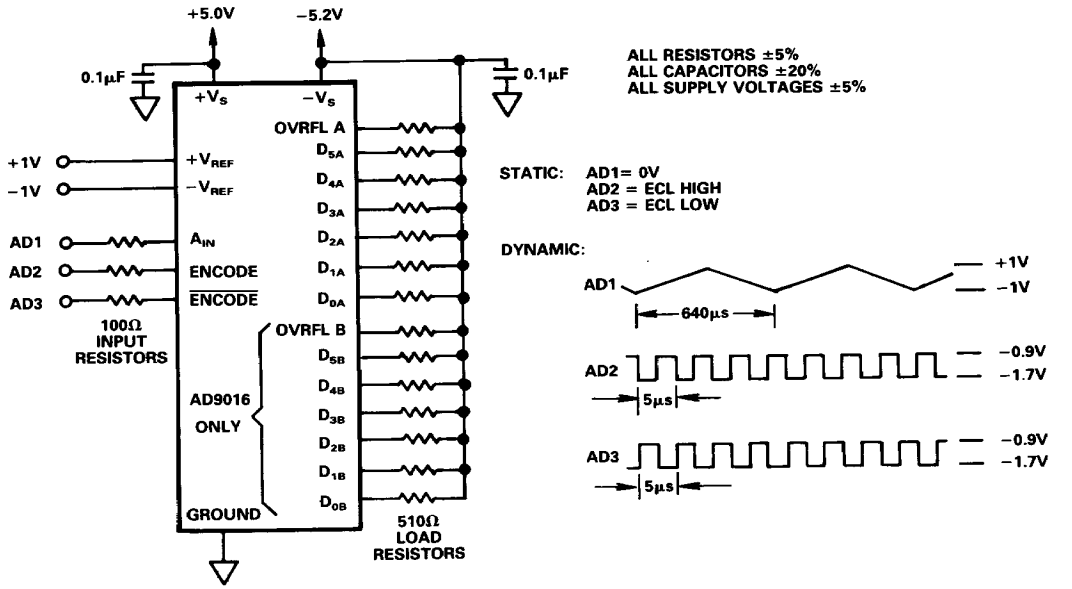

AD9006/AD9016 Burn-In Diagram