



32Mx72 DRAM DIMM

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
WPD32M72-60MDC	60ns	20ns	110ns	40ns
WPD32M72-70MDC	70ns	25ns	130ns	45ns

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only refresh capability
- LVTTL compatible inputs and outputs
- +3.3V $\pm$ 0.3V power supply
- 8192 cycles/64ms refresh
- JEDEC standard pinout
- ECC Optimized
- Gold edge connectors

GENERAL DESCRIPTION

The WPD32M72-XMDC is an 32M x 72 bit Dynamic RAM high density memory module. The module consists of thirty-six 16M x 4 bit DRAMs in 32-pin TSOP packages. The DRAMs are mounted in stacks of two on a 168-pin glass epoxy substrate. A 0.1 μ F decoupling capacitor is mounted for each DRAM. Selected inputs and outputs are buffered for improved performance and easier memory subsystem design.

The WPD32M72-XMDC is a Dual In-line Memory Module with gold edge connections, 3.3V power supply, 8K refresh, optimized for ECC, and intended for mounting into 168-pin edge connector sockets.

DRAM MCMS



PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{SS}	25	NC	49	V _{CC}	73	V _{CC}	97	DQ ₄₅	121	A ₉	145	NC
2	DQ ₀	26	V _{CC}	50	NC	74	DQ ₃₂	98	DQ ₄₆	122	A ₁₁	146	NC
3	DQ ₁	27	$\overline{WE}_0$	51	NC	75	DQ ₃₃	99	DQ ₄₇	123	NC	147	NC
4	DQ ₂	28	$\overline{CAS}_0$	52	DQ ₁₈	76	DQ ₃₄	100	DQ ₄₈	124	V _{CC}	148	NC
5	DQ ₃	29	NC	53	DQ ₁₉	77	PQ ₃₅	101	DQ ₄₉	125	NC	149	DQ ₆₁
6	V _{CC}	30	$\overline{RAS}_0$	54	V _{SS}	78	V _{SS}	102	V _{CC}	126	B ₀	150	DQ ₆₂
7	DQ ₄	31	$\overline{OE}_0$	55	DQ ₂₀	79	PD ₁	103	DQ ₅₀	127	V _{SS}	151	DQ ₆₃
8	DQ ₅	32	V _{SS}	56	DQ ₂₁	80	PD ₃	104	DQ ₅₁	128	NC	152	V _{SS}
9	DQ ₆	33	A ₀	57	DQ ₂₂	81	PD ₅	105	DQ ₅₂	129	$\overline{RAS}_3$	153	DQ ₆₄
10	DQ ₇	34	A ₂	58	DQ ₂₃	82	PD ₇	106	DQ ₅₃	130	NC	154	DQ ₆₅
11	DQ ₈	35	A ₄	59	V _{CC}	83	ID ₀	107	V _{SS}	131	NC	155	DQ ₆₆
12	V _{SS}	36	A ₆	60	DQ ₂₄	84	V _{CC}	108	NC	132	$\overline{PDE}$	156	DQ ₆₇
13	DQ ₉	37	A ₈	61	NC	85	V _{SS}	109	NC	133	V _{CC}	157	V _{CC}
14	DQ ₁₀	38	A ₁₀	62	NC	86	DQ ₃₆	110	V _{CC}	134	NC	158	DQ ₆₈
15	DQ ₁₁	39	A ₁₂	63	NC	87	DQ ₃₇	111	NC	135	NC	159	DQ ₆₉
16	DQ ₁₂	40	V _{CC}	64	NC	88	DQ ₃₈	112	NC	136	DQ ₅₄	160	DQ ₇₀
17	DQ ₁₃	41	NC	65	DQ ₂₅	89	DQ ₃₉	113	NC	137	DQ ₅₅	161	DQ ₇₁
18	V _{CC}	42	NC	66	DQ ₂₆	90	V _{CC}	114	$\overline{RAS}_1$	138	V _{SS}	162	V _{SS}
19	DQ ₁₄	43	V _{SS}	67	DQ ₂₇	91	DQ ₄₀	115	NC	139	DQ ₅₆	163	PD ₂
20	DQ ₁₅	44	$\overline{OE}_2$	68	V _{SS}	92	DQ ₄₁	116	V _{SS}	140	DQ ₅₇	164	PD ₄
21	DQ ₁₆	45	$\overline{RAS}_2$	69	DQ ₂₈	93	DQ ₄₂	117	A ₁	141	DQ ₅₈	165	PD ₆
22	DQ ₁₇	46	$\overline{CAS}_4$	70	DQ ₂₉	94	DQ ₄₃	118	A ₃	142	DQ ₅₉	166	PD ₈
23	V _{SS}	47	NC	71	DQ ₃₀	95	DQ ₄₄	119	A ₅	143	V _{CC}	167	ID ₁
24	NC	48	$\overline{WE}_2$	72	DQ ₃₁	96	V _{SS}	120	A ₇	144	DQ ₆₀	168	V _{CC}

continued on the next page

DRAM MCMS



PIN CONFIGURATION (continued)

Pin Names

Pin Name	Pin Function
A_0, B_0, A_1-A_{12}	Address Inputs (Buffered)
DQ_x	Data In/Out
$\overline{WE}_0, \overline{WE}_2$	Read/Write Input (Buffered)
$\overline{OE}_0, \overline{OE}_2$	Output Enable (Buffered)
$\overline{RAS}_0-\overline{RAS}_3$	Row Address Strobe
$\overline{CAS}_0, \overline{CAS}_4$	Column Address Strobe (Buffered)
PD_1-PD_8	Presence Detect (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID_0-ID_1	ID Bits
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Presence Detect

For 32Mx72 Bit Configuration with 16M x 4 Bit chips and 8K Refresh:

$PD_1=NC, PD_2=V_{SS}, PD_3=V_{SS}, PD_4=V_{SS}$

For Fast Page:

$PD_5=V_{SS}$

Speed:

Pin	60ns	70ns
PD_6	NC	V_{SS}
PD_7	NC	NC

For ECC:

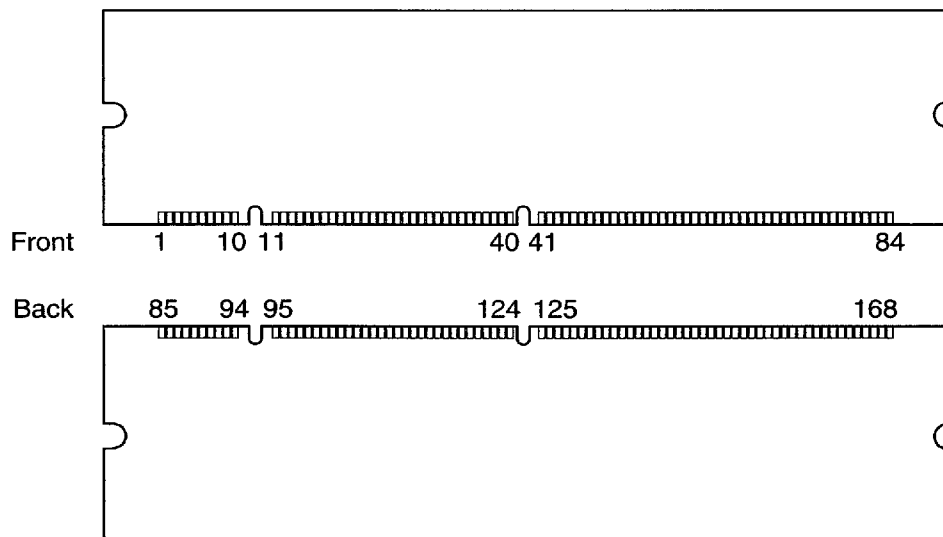
$PD_8=V_{SS}$

For x72 ECC:

$ID_0=V_{SS}$

For Normal Refresh Mode:

$ID_1=V_{SS}$



DRAM MCMS

**ABSOLUTE MAXIMUM RATINGS***

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA
Short Circuit Output Current (PD)	I_{OUTPD}	60	mA

- * Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS} , $T_A=0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+0.3^*$	V
Input Low Voltage	V_{IL}	-0.3**	—	0.8	V

- * $V_{CC}+1.3\text{V}$ at pulse width $\leq 15\text{ns}$ which is is measured at V_{CC}

- ** -1.3V at pulse width $\leq 15\text{ns}$ which is is measured at V_{SS}

DRAM MCMS

**DC AND OPERATION CHARACTERISTICS**

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* (RAS, CAS Cycling @ $t_{RC} = \text{min.}$)	WPD32M72-60 WPD32M72-70	I_{CC1}	—	1638 1458	mA mA
Standby Current (RAS=CAS= V_{IH})		I_{CC2}	—	36	mA
RAS-Only Refresh Current* (CAS= V_{IH} , RAS Cycling @ $t_{RC} = \text{min.}$)	WPD32M72-60 WPD32M72-70	I_{CC3}	—	1638 1458	mA mA
Fast Page Mode Current* (RAS= V_{IL} , CAS, Address Cycling @ $t_{PC} = \text{min.}$)	WPD32M72-60 WPD32M72-70	I_{CC4}	—	1098 1008	mA mA
Standby Current (RAS=CAS= $V_{CC} - 0.2V$)		I_{CC5}	—	18	mA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @ $t_{RC} = \text{min.}$)	WPD32M72-60 WPD32M72-70	I_{CC6}	—	1638 1458	mA mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC} + 0.3V$, all other pins not under test=0V)	All but RAS RAS	I_{IL}	-10 -45	10 45	μA μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq V_{CC}$)		I_{OL}	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)		V_{OH1}	2.4	—	V
Output Low Voltage Level ($I_{OL} = 2mA$)		V_{OL}	—	0.4	

* I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} , I_{CC6} and I_{CC3} , address can be changed maximum once while RAS= V_{IL} . In I_{CC4} , address can be changed maximum once within one fast page mode cycle time, t_{PC} .

CAPACITANCE ($T_A = 25^\circ C$)

Item	Symbol	Min	Max	Units
Input Capacitance (A_0, B_0)	C_{IN1}	—	13	pF
Input Capacitance (A_{1-9})	C_{IN1}	—	13	pF
Input Capacitance ($\overline{CAS}, \overline{WE}, \overline{OE}$)	C_{IN2}	—	13	pF
Input Capacitance (RAS)	C_{IN3}	—	63	pF
Input/Output Capacitance (DQ_x)	C_{IO1}	—	14	pF

DRAM MCMS

**AC CHARACTERISTICS** ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, See notes 1, 2, 3, and 4)

Parameter	Symbol	WPD32M72-60		WPD32M72-70		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		ns	
Access time from $\overline{\text{RAS}}$	t_{RAC}		60		70	ns	11, 12
Access time from $\overline{\text{CAS}}$	t_{CAC}		20		25	ns	11, 12
Access time from column address	t_{AA}		36		41	ns	11, 12
$\overline{\text{CAS}}$ to output in Low-Z	t_{CLZ}	2		2		ns	
Output buffer turn-off delay	t_{OFF}	2	20	2	25	ns	14
Transition time (rise and fall)	t_T	3	30	3	30	ns	2
$\overline{\text{RAS}}$ precharge time	t_{RP}	40		50		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	20		25		ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	58		68		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	15		20		ns	5
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	18	40	18	45	ns	6
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	13	24	13	29	ns	7
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	15		15		ns	
Row address set-up time	t_{ASR}	6		6		ns	
Row address hold time	t_{RAH}	8		8		ns	
Column address set-up time	t_{ASC}	4		4		ns	
Column address hold time	t_{CAH}	17		17		ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	36		41		ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	36		41		ns	
Read command set-up time	t_{RCS}	2		2		ns	
Read command hold referenced to $\overline{\text{CAS}}$	t_{RCH}	2		2		ns	13
Read command hold referenced to $\overline{\text{RAS}}$	t_{RRH}	3		3		ns	13
Write command hold time	t_{WCH}	17		17		ns	
Write command pulse width	t_{WP}	15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	20		25		ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	17		22		ns	
Data-in set-up time	t_{DS}	-2		-2		ns	10

continued on the next page

DRAM MCMS



AC CHARACTERISTICS (continued)

Parameter	Symbol	WPD32M72-60		WPD32M72-70		Unit	Notes
		Min	Max	Min	Max		
Data-in hold time	t_{DH}	20		20		ns	10
Refresh period	t_{REF}		64		64	ms	15
Write command set-up time	t_{WCS}	2		2		ns	9
CAS set-up time (C-B-R refresh)	t_{CSR}	15		15		ns	
CAS hold time (C-B-R refresh)	t_{CHR}	18		18		ns	
RAS precharge to CAS hold time	t_{RPC}	3		3		ns	
Access time from CAS precharge	t_{CPA}		40		45	ns	11, 12
Fast Page mode cycle time	t_{PC}	40		45		ns	
CAS precharge time (fast page)	t_{CP}	10		10		ns	
RAS pulse width (fast page)	t_{RASP}	60	100,000	70	100,000	ns	
WE to RAS precharge time (C-B-R refresh)	t_{WRP}	15		15		ns	
WE to RAS hold time (C-B-R refresh)	t_{WRH}	8		8		ns	
OE to D_{IN} delay time	t_{ODD}	20		25		ns	8
OE delay time from D_{IN}	t_{DZO}	-2		-2		ns	
CAS delay time from D_{IN}	t_{DZC}	-2		-2		ns	
Access time from OE	t_{OEA}		20		25	ns	11, 12
Output data hold time	t_{OH}	2		2		ns	
Output data hold time from OE	t_{OHO}	2		2		ns	
Output buffer turn-off delay from OE	t_{OEZ}	2	20	2	25	ns	14
CAS to D_{IN} delay time	t_{CDD}	20		25		ns	8
RAS hold time from CAS precharge	t_{CPRH}	40		45		ns	
Read-Modify-Write cycle time	t_{RWC}	158		188		ns	
RAS to WE delay time	t_{RWD}	83		98		ns	9
CAS to WE delay time	t_{CWD}	45		55		ns	9
Column address to WE delay time	t_{AWD}	59		69		ns	9
OE command hold time	t_{OEH}	15		20		ns	
Fast Page Mode Read-Modify-Write cycle	t_{PRWC}	83		98		ns	
WE delay time from CAS precharge	t_{CPW}	63		73		ns	9
PDE to valid presence detect data	t_{PD}		10		10	ns	11
PDE inactive to presence detects inactive	t_{PDOFF}	0	10	0	10	ns	16

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DRAM MCMS

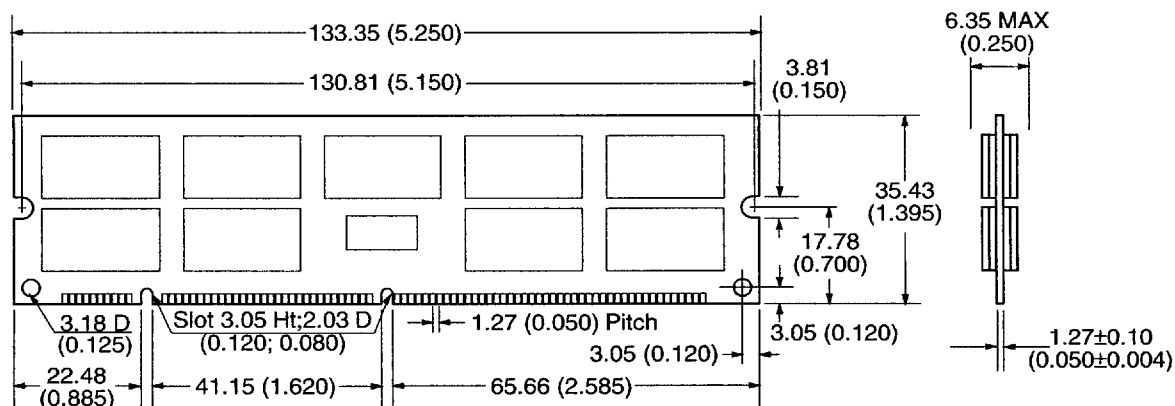


AC CHARACTERISTICS (continued)

Notes

1. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
2. An initial pause of 200 μs is required after power-up followed by 8 RAS-only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS before RAS refresh cycles instead of 8 RAS-only refresh cycles is required. The DRAM outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, RAS should rise coincident with the power supply voltage.
3. The specified timings include buffer, loading, and skew delay adders: 2ns minimum, 5ns (CAS, WE, OE) or 6ns (address) maximum delay, no pulse shrinkage to the DRAM device timings. The data and RAS signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume $t_r = 5\text{ns}$.
5. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
6. Operation within the $t_{RCD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. The $t_{RCD}(\text{max})$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled by t_{CAC} .
7. Operation within the $t_{RAD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. The $t_{RAD}(\text{max})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .
8. Either t_{CDD} or t_{ODD} must be satisfied.
9. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} , and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$, and $t_{CPW} \geq t_{CPW}(\text{min})$ (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell. If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
10. Data-in set-up and hold is measured from the latter of the two timings, $\overline{\text{CAS}}$ or $\overline{\text{WE}}$.
11. Measured with the specified current load and 100pF.
12. Access time is determined by the latter of t_{RAC} , t_{CAC} , t_{CPA} , t_{AA} , t_{OEA} .
13. Either t_{RCH} or t_{RRH} must be satisfied.
14. $t_{OFF}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
15. 8192 refreshes are required every 64ms.
16. $t_{PD OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

DRAM MCMS

**PACKAGE: 168-PIN DIMM** ± 0.13 (± 0.005) TOLERANCE UNLESS OTHERWISE SPECIFIED

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION**W P D 32M72 - X M D C X****LEAD FINISH:**

T = Tin Edge Connectors

Blank = Gold Edge Connectors

DEVICE GRADE:

C = Commercial

0 to +70°C

PACKAGE TYPE:

MD = 168 pin DIMM

ACCESS TIME In ns**ORGANIZATION, 32M x 72****DRAM****Plastic Module****WHITE MICROELECTRONICS**

DRAM MCMS