UCN-5832A AND UCN-5832C
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

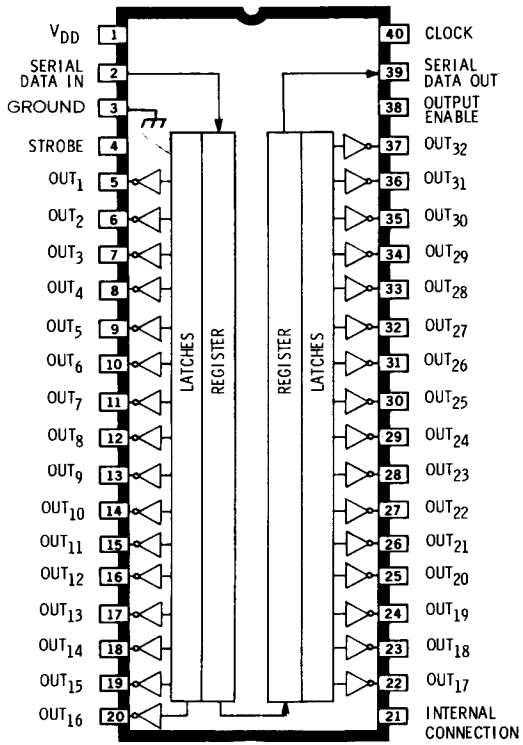
FEATURES

- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 40 V Current Sink Outputs
- Low Saturation Voltage

INTENDED PRIMARILY to drive thermal printheads, Types UCN-5832A and UCN-5832C have been optimized for low output-saturation voltage, high-speed operation, and pin/pad configurations most convenient for the tight space requirements of high-resolution printheads. The integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 150 mA peak current. A combination of bipolar and MOS technologies gives BiMOS II arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

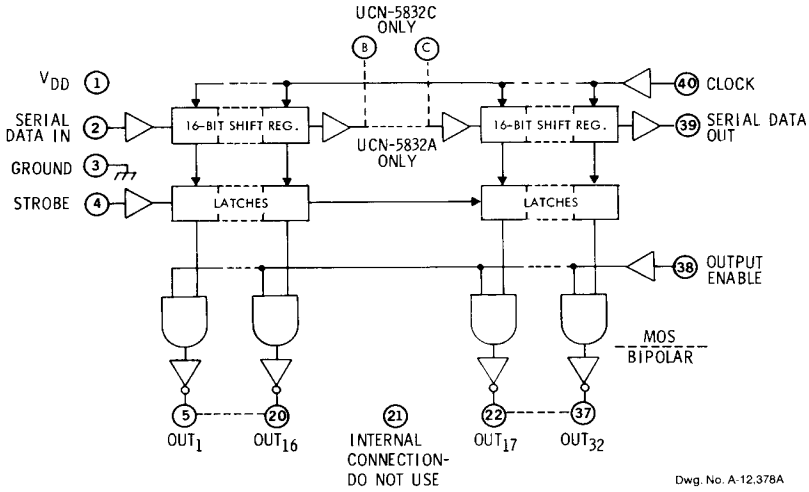
Type UCN-5832A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. Under normal operating conditions, all outputs of the packaged device will sustain 100 mA continuously without derating. Type UCN-5832C is an unpackaged, passivated, bare-back device in chip form. In this version, the shift register is divided into two 16-bit blocks for maximum flexibility. For either device, MOS serial outputs permit cascading for interface applications requiring additional drive lines.



Dwg. No. A-12,377A

A similar 32-bit serial-input latched source driver is available as UCN-5818A. High-voltage, high-current 8-bit devices are available in Series UCN-5820A.

FUNCTIONAL BLOCK DIAGRAM



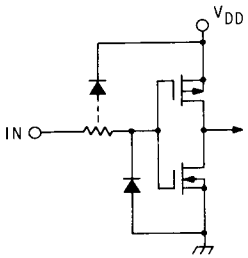
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT}	40 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT}	150 mA
Package Power Dissipation, P_D (UCN-5832A)	2.8 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 28 mW/°C above T_A = +25°C

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



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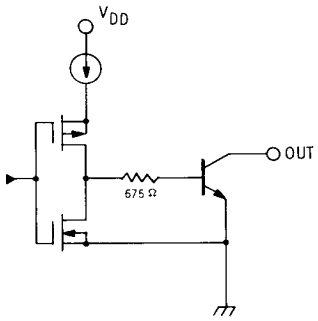
TYPICAL OUTPUT DRIVER



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ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 40$ V, $T_A = 70°C$	—	10	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50$ mA	—	275	mV
		$I_{OUT} = 100$ mA	250	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = 3.5$ V	—	1.0	μA
	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	−1.0	μA
Input Impedance	Z_{IN}	$V_{IN} = 3.5$ V	3.5	—	MΩ
Serial Data/Output Resistance	R_{OUT}		—	20	kΩ
Supply Current	I_{DD}	One output ON, $I_{OUT} = 100$ mA	—	5.0	mA
		All outputs OFF	—	50	μA
Output Rise Time	t_r	$I_{OUT} = 100$ mA, 10% to 90%	—	1.0	μs
Output Fall Time	t_f	$I_{OUT} = 100$ mA, 90% to 10%	—	1.0	μs

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

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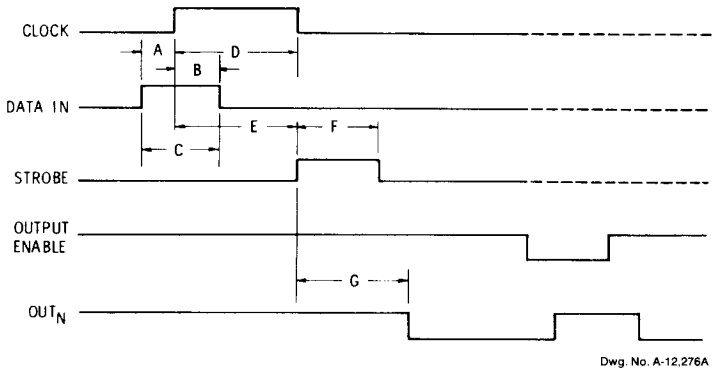


TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

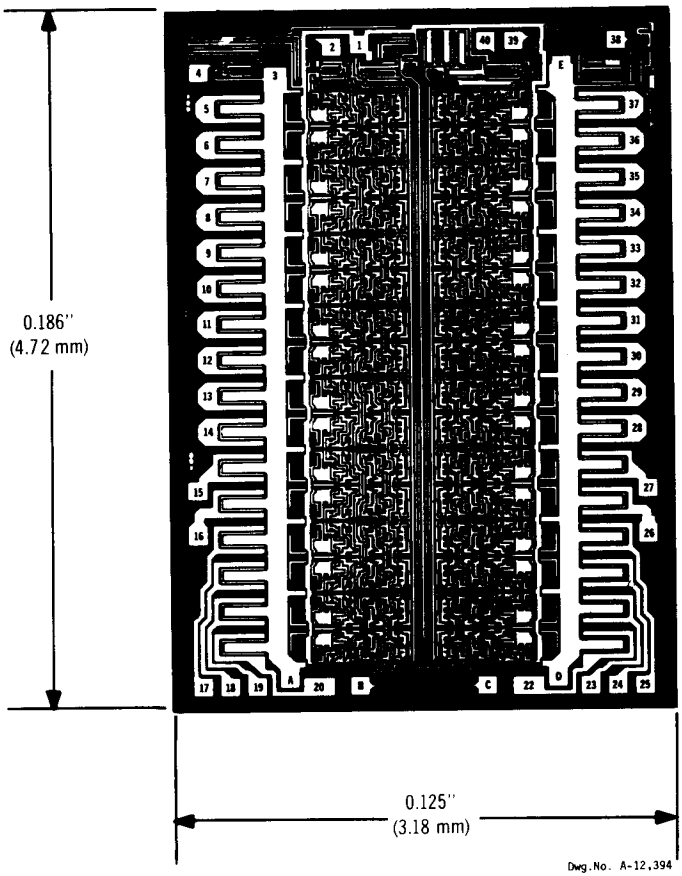
When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable Input	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
X	⎎	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$
					$X\ X\ X\ \ldots X\ X$	L	$H\ H\ H\ \ldots H\ H$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5832C



UCN-5832 chips are of silicon planar epitaxial construction. They are identical to those used for packaged devices. When assembled correctly, they should lead to a high final test yield. All chips are visually inspected for masking, diffusion, and scribing defects. Conformance to electrical parameters can be guaranteed (at additional charge) by performing measurements on packaged units assembled from a random sample taken from the lot.

The preferred method of sale for unpackaged die is in wafer form. These are identified as UCN-5832C*W* and are supplied in 4" (100 mm) wafers that have been tested (probed) in wafer form. Electrically defective devices are identified by ink dots during this operation. Wafers do not include visual die inspection. Orders for UCN-5832C*W* will be accepted only for complete wafers.

Because Sprague Electric Company does not control the customer packaging of UCN-5832C chips or UCN-5832C*W* wafers, Sprague Electric company assumes no liability for final electrical and reliability parameters.

	PAD DESIGNATIONS	
PAD	UCN-5832A	UCN-5832C
1	V_{DD}	V_{DD}
2	SERIAL DATA IN	SERIAL DATA IN_1
3	GROUND	GROUND*
4	STROBE	STROBE
5	OUT_1	OUT_1
6	OUT_2	OUT_2
7	OUT_3	OUT_3
8	OUT_4	OUT_4
9	OUT_5	OUT_5
10	OUT_6	OUT_6
11	OUT_7	OUT_7
12	OUT_8	OUT_8
13	OUT_9	OUT_9
14	OUT_{10}	OUT_{10}
15	OUT_{11}	OUT_{11}
16	OUT_{12}	OUT_{12}
17	OUT_{13}	OUT_{13}
18	OUT_{14}	OUT_{14}
19	OUT_{15}	OUT_{15}
A	—	GROUND*
20	OUT_{16}	OUT_{16}
B	—	SERIAL DATA OUT_{16}
21	INTERNAL CONNECTION—DO NOT USE	—
C	—	SERIAL DATA IN_{17}
22	OUT_{17}	OUT_{17}
D	—	GROUND*
23	OUT_{18}	OUT_{18}
24	OUT_{19}	OUT_{19}
25	OUT_{20}	OUT_{20}
26	OUT_{21}	OUT_{21}
27	OUT_{22}	OUT_{22}
28	OUT_{23}	OUT_{23}
29	OUT_{24}	OUT_{24}
30	OUT_{25}	OUT_{25}
31	OUT_{26}	OUT_{26}
32	OUT_{27}	OUT_{27}
33	OUT_{28}	OUT_{28}
34	OUT_{29}	OUT_{29}
35	OUT_{30}	OUT_{30}
36	OUT_{31}	OUT_{31}
37	OUT_{32}	OUT_{32}
38	OUTPUT ENABLE	OUTPUT ENABLE
E	—	GROUND*
39	SERIAL DATA OUT	SERIAL DATA OUT_{32}
40	CLOCK	CLOCK

*Bonding pads *A* or *3* and *D* or *E* must be connected to the substrate. For maximum output current capability, pads *A, D, E,* and *3* must all be bonded to the substrate.