

SERIES UCN-5820A

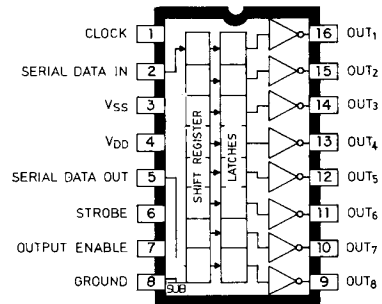
BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- 3.3 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Logic & Latches
- High-Voltage Current-Sink Outputs
- 16-Pin Dual In-Line Plastic Package

A COMBINATION of bipolar and MOS technology gives the Series UCN-5820A an interface flexibility beyond the reach of standard logic buffers and power driver arrays. The three devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers. Except for maximum driver output voltage ratings, the UCN-5821A, UCN-5822A, and UCN-5823A are identical.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL and DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.



DWG. NO. A-11,388B

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature and $V_{SS} = 0$ V

Output Voltage, V_{OUT} (UCN-5821A)	50 V
(UCN-5822A)	80 V
(UCN-5823A)	100 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	-0.3 V to $V_{DD} + 0.3$ V
Continuous Output Current, I_{OUT}	500 mA
Package Power Dissipation, P_D	1.67 W*
Operating Temperature Range, T_A	-20°C to +85°C
Storage Temperature Range, T_S	-55°C to +125°C

*Derate at the rate of 16.7 mW/°C above $T_A = +25^\circ\text{C}$

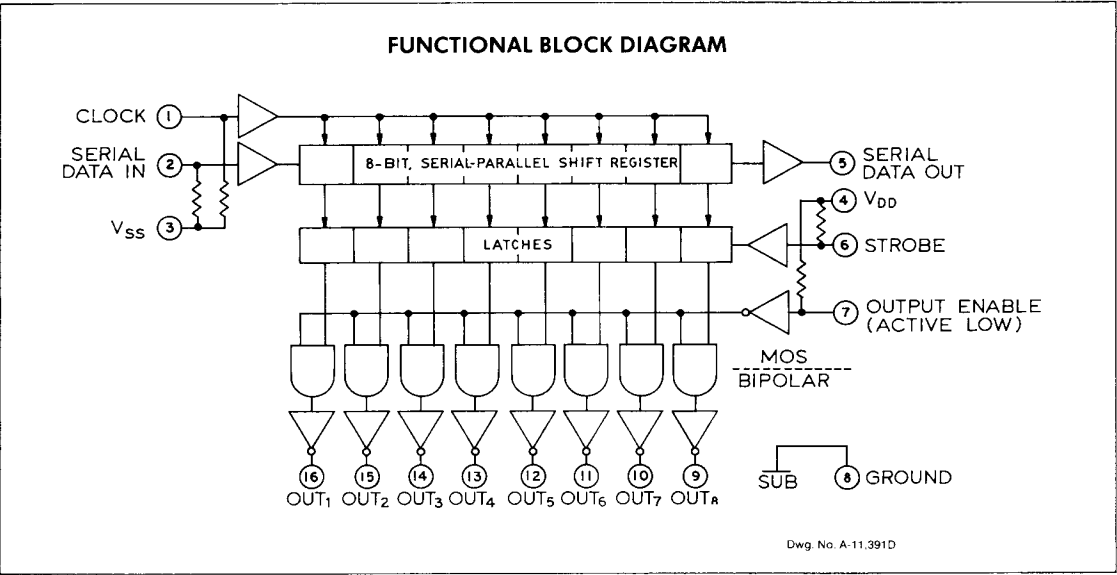
Number of Outputs ON ($I_{OUT} = 200$ mA $V_{DD} = 12$ V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	73%	62%	55%	47%	40%
7	83%	71%	62%	54%	46%
6	97%	82%	72%	63%	53%
5	100%	98%	87%	75%	63%
4	100%	100%	100%	93%	79%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

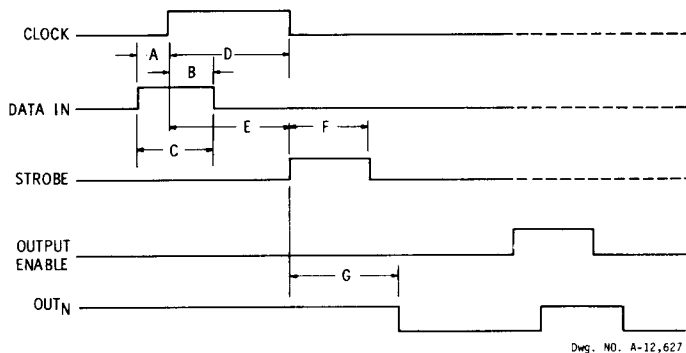
SERIES UCN-5820A
BiMOS 8-BIT SERIAL-INPUT LATCHED DRIVERS

ELECTRICAL CHARACTERISTICS at $T_A = +25^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	UCN-5821A	$V_{OUT} = 50\text{ V}$	—	50	μA
			$V_{OUT} = 50\text{ V}, T_A = +70^{\circ}\text{C}$	—	100	μA
		UCN-5822A	$V_{OUT} = 80\text{ V}$	—	50	μA
			$V_{OUT} = 80\text{ V}, T_A = +70^{\circ}\text{C}$	—	100	μA
		UCN-5823A	$V_{OUT} = 100\text{ V}$	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\text{ mA}$	—	1.1	V
			$I_{OUT} = 200\text{ mA}$	—	1.3	V
			$I_{OUT} = 350\text{ mA}, V_{DD} = 7.0\text{ V}$	—	1.6	V
			$V_{OUT} = 100\text{ V}, T_A = +70^{\circ}\text{C}$	—	100	μA
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 12\text{ V}$	10.5	—	V
			$V_{DD} = 10\text{ V}$	8.5	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 5.0\text{ V}$	3.5	—	V
			$V_{DD} = 12\text{ V}$	50	—	$\text{k}\Omega$
			$V_{DD} = 10\text{ V}$	50	—	$\text{k}\Omega$
Supply Current	$I_{DD(ON)}$	ALL	$V_{DD} = 5.0\text{ V}$	50	—	$\text{k}\Omega$
			One Driver ON, $V_{DD} = 12\text{ V}$	—	4.5	mA
			One Driver ON, $V_{DD} = 10\text{ V}$	—	3.9	mA
	$I_{DD(OFF)}$	ALL	One Driver ON, $V_{DD} = 5.0\text{ V}$	—	2.4	mA
			$V_{DD} = 5.0\text{ V}$, All Drivers OFF, All Inputs = 0 V	—	1.6	mA
			$V_{DD} = 12\text{ V}$, All Drivers OFF, All Inputs = 0 V	—	2.9	mA

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.





TIMING CONDITIONS

$(T_A = +25^\circ\text{C}, \text{Logic Levels are } V_{DD} \text{ and } V_{SS})$

	$V_{DD} = 5.0 \text{ V}$
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will con-

tinue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

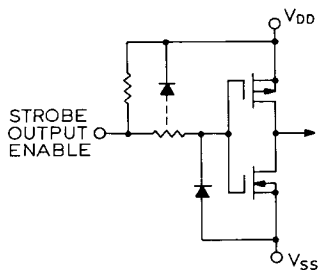
SERIES UCN-5820A
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SERIES UCN-5820A TRUTH TABLE

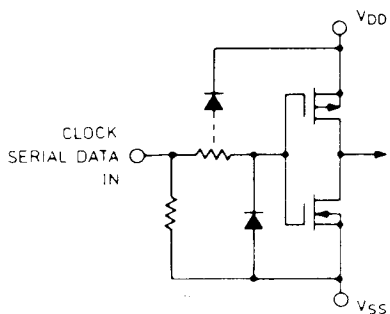
Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable	Output Contents					
		I ₁	I ₂	I ₃		I ₆	I ₇			L ₁	L ₂	L ₃		L ₆	L ₇		O ₁	O ₂	O ₃		O ₆	O ₇
H		H	R ₁	R ₂		R ₆	R ₇	R ₇														
L		L	R ₁	R ₂		R ₆	R ₇	R ₇														
X		R ₁	R ₂	R ₃		R ₆	R ₇	R ₇														
		X	X	X		X	X	X	L	R ₁	R ₂	R ₃		R ₆	R ₇		L					
		P ₁	P ₂	P ₃		P ₆	P ₇	P ₇	H	P ₁	P ₂	P ₃		P ₆	P ₇							
										X	X	X		X	X							

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

TYPICAL INPUT CIRCUITS

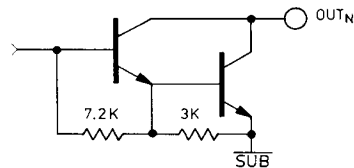


Dwg. No. A-12,058



Dwg. No. A-12,059

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,314