3 Electrical Characteristics

3.1 Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 3.8 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{DD} + 0.3 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
dc supply voltage, V_{CC} . . . . . 5 V
I/O Voltage with respect to GND . . . . . –0.5 V to V_{DD} + 0.3 V
I/O Voltage with respect to GND (see Note 2) . . . . . –0.5 V to V_{CC}+ 0.5 V
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Junction temperature range, T_J . . . . . 125°C
Case temperature range for 10 seconds, T_C . . . . . 260°C
Lead temperature range 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to GND.
2. Applies to the following signals: PCIAD(0–31), $\overline{\text{PCICBE}}$(0–3), PCIPAR, $\overline{\text{PCIFRAME}}$, $\overline{\text{PCIFRAME}}$, $\overline{\text{PCIIRDY}}$, $\overline{\text{PCISTOP}}$, $\overline{\text{PCILOCK}}$, $\overline{\text{PCIIDSEL}}$, $\overline{\text{PCIDEVSEI}}$, $\overline{\text{PCIREQ}}$, $\overline{\text{PCIGNT}}$, $\overline{\text{PCIINTA}}$, PCICIK, PCIFIFOINDIS, PCIFIFOOUTDIS, $\overline{\text{PCIRST}}$, DDC, $\overline{\text{AUXWAIT}}$, VCLK, MCLK, and RDACDAT (0–7).

3.2 Recommended Operating Conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
Supply voltage, V_{CC}	4.75	5.0	5.25	V
High-level input voltage, V_{IH}	2.0		V_{DD}+0.8	V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature range, T_A	0		70	°C

3.3 Electrical Characteristics

PARAMETER		TEST CONDITIONS	TVP4010–60			TVP4010–80			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
L	Inductance				18.4			18.4	nH
I_{CC}	Supply current (running Direct3D game)	V_{CC} = 3.3 V		0.5			0.7		A

3.3.1 PCI

PARAMETER		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage			0.8	V
V_{IH}	High-level input voltage	2.0			V
V_{OL}	Low-level output voltage			0.5	V
V_{OH}	High-level output voltage	2.4			V
I_{IL}	Low-level input current			–20	μA
I_{IH}	High-level input current			20	μA
C_I	Input capacitance			10	pF
$C_{I(CLK)}$	Input capacitance, PCI clock			10	pF
$C_{I(DSEL)}$	Input capacitance, PCI IDSEL			8	pF

3.3.2 Non-PCI

PARAMETER		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage			0.8	V
V_{IH}	High-level input voltage	2.0			V
V_{OL}	Low-level output voltage			0.5	V
V_{OH}	High-level output voltage	2.4			V
I_{IL}	Low-level input current			1	μA
I_{IH}	High-level input current			1	μA
$I_{IH(PD)}$	High-level input current, pulldown			250	μA
$I_{IL(PU)}$	Low-level input current, pullup			250	μA
C_I	Input capacitance			10	pF

3.4 Operating Characteristics

			MIN	TYP	MAX	UNIT
C_L	Capacitive load	MADD(0–9)	80	80	80	pF
		PCIAD(0–31), PCICBE(0–3), PCIPAR, PCIFRAME, PCIIRDY, PCITRDY, PCISTOP, PCIIDSEl, PCIDEVSEl, PCIREQ, PCIGNT, PCIINTA, MBANK(0–3), MBYTE(0–7), MCAS(0–1), MDSF(0–1), MEMCKE, MEMCKOUT(0–1), MRAS(0–1), MWE(0–1), RAMDACR, RAMDACW, RDACADD(0–3), RDACDAT(0–7)	50	50	50	pF
		MDAT(60–63)	40	40	40	pF
		AUXREAD, AUXWRITE, RESETOUT, ROM, ROMWE, VIDBLANK, VIDCTL(0–1), VIDPIX(0–31)	30	30	30	pF
		VIDHSYNC, VIDVSYNC	20	20	20	pF

3.5 Timing Requirements

PARAMETER		TVP4010–60			TVP4010–80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{c1}	Cycle time, PCICLK	30			30			ns
t_{w1}	Pulse duration, PCICLK high	12			12			ns
t_{w2}	Pulse duration, PCICLK low	12			12			ns
t_{c2}	Cycle time, MCLK	16.7			12.5			ns
t_{w3}	Pulse duration, MCLK high	6.5			5			ns
t_{w3}	Pulse duration, MCLK low	6.5			5			ns
t_{c3}	Cycle time, VCLK	12.5			12.5			ns
t_{w4}	Pulse duration, VCLK high	5			5			ns
t_{w5}	Pulse duration, VCLK low	5			5			ns

3.5.1 PCI Clock Referenced Input Timing

PARAMETERS			MIN	TYP	MAX	UNIT
t_{su1}	Setup time	PCIAD(0–31), $\overline{\text{PCICBE}}$(0–3), PCIPAR, $\overline{\text{PCIFRAME}}$, PCIIRDY, $\overline{\text{PCITRDY}}$, $\overline{\text{PCISTOP}}$, PCIIDSEL, $\overline{\text{PCIDEVSEl}}$	7			ns
		$\overline{\text{PCIGNT}}$	10			ns
		$\overline{\text{PCIRST}}$ (see Note 1)	7			ns
		RDACDATA(0–7)	13			ns
t_{h1}	Hold time	PCIAD(0–31), $\overline{\text{PCICBE}}$(0–3), PCIPAR, $\overline{\text{PCIFRAME}}$, $\overline{\text{PCIIRDY}}$, $\overline{\text{PCITRDY}}$, $\overline{\text{PCISTOP}}$, PCIIDSEL, $\overline{\text{PCIDEVSEl}}$	0			ns
		$\overline{\text{PCIGNT}}$	0			ns
		$\overline{\text{PCIRST}}$ (see Note 1)	0			ns
		RDACDATA(0–7)	2			ns

NOTE 1: $\overline{\text{PCLRST}}$ is resynchronized internally. The timings given, when met, ensure that the reset is detected in the current cycle.

3.5.2 PCI Clock Referenced Output Timing

PARAMETERS			MIN	TYP	MAX	UNIT
t_{su2}	Setup time	PCIAD(0–31), $\overline{\text{PCICBE}}$(0–3), PCIPAR, $\overline{\text{PCIFRAME}}$, PCIIRDY, $\overline{\text{PCITRDY}}$, $\overline{\text{PCISTOP}}$, PCIIDESL, $\overline{\text{PCIDEVSEl}}$	2		11	ns
		$\overline{\text{PCIREQ}}$	2		12	ns
		$\overline{\text{PCIINTA}}$ (see Note 2)	2		12	ns

NOTE 2: Timings given are for falling edges of the open drain signal. Rise times are dependent on the value of the external pull-up resistors.

3.5.3 RAMDAC Timing, 33 MHz PCI Clock

	PARAMETER	MIN	TYP	MAX	UNITS
t_{w6}	Pulse duration, $\overline{\text{RAMDACW}}$ low		120		ns
t_{su3}	Setup time, address		30		ns
t_{h2}	Hold time, address		30		ns
t_{su4}	Setup time, data		30		ns
t_{h3}	Hold time, data		30		ns
t_{a1}	Access time, data from $\overline{\text{RAMDACR}}$		100		ns
t_{d1}	Delay time, $\overline{\text{RAMDACR}}$ high to data bus three-state		30		ns

3.5.4 AUX Timings, 33 MHz PCI Clock

	PARAMETER	MIN	TYP	MAX	UNITS
t_{w7}	Pulse duration, $\overline{\text{AUXREAD}}$ low		150		ns
t_{d2}	Delay time, strobe low to $\overline{\text{AUXWAIT}}$ asserted		30		ns
t_{d3}	Delay time, $\overline{\text{AUXWAIT}}$ high to $\overline{\text{AUXWRITE}}$ high		30		ns
t_{d4}	Delay time, $\overline{\text{AUXWAIT}}$ high to read data valid		0		ns
t_{a2}	Access time, data from $\overline{\text{AUXREAD}}$		130		ns
t_{d2}	Delay time, $\overline{\text{AUXREAD}}$ high to data bus three-state		30		ns

3.5.5 MEMCKOUT Referenced Input Timing

	PARAMETERS	TVP4010–60			TVP4010–80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{su5}	Setup time, MDAT(0–63) (see Note 3)	1			1			ns
t_{h5}	Hold time, MDAT(0–63) (see Note 3)	3			2			ns

NOTE 3: All timings below are with respect to MEMCKOUT, which is a delayed version of MCLK.

3.5.6 MEMCKOUT Referenced Output Timing

	PARAMETER	TVP4010–60			TVP4010–80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{su6}	Setup time, all memory control, data and address lines (see Note 3)			13.5			9	ns