LH28F020SUN-L12
2 Mbit (256 Kbit x 8)
3.3V (V_{PP}=5V) FLASH MEMORY

FEATURES

- 16 Independently Lockable Blocks
- 100,000 Erase Cycles per Block
- 5V Write/Erase Operation (5V V_{PP}, 3.3V V_{CC})
- 256 Kbit x 8 Bit Configuration
- Min. 2.7V Read Capability
  - 160 ns Maximum Access Time (V_{CC}=2.7V)
- Automated Byte Write/Block Erase
  - Command User Interface
  - Status Register
- 32-Lead, 2.7mm x 14.1mm x 20.6mm SOP Package
- System Performance Enhancement
  - Erase Suspend for Read
  - Two-Byte Write
  - Full Chip Erase
- Data Protection
  - Hardware Erase/Write Lockout during Power Transitions
  - Software Erase/Write Lockout
- Independently Lockable for Write/Erase on Each Block (Lock Block & Protect Set/ Reset)
- 80 µA (Max.) I_{CC} in CMOS Standby
- State-of-the-Art 0.55 µm ETOX™* Flash Technology

Sharp's LH28F020SUN-L12 2-Mbit Flash Memory is a revolutionary architecture which enables the design of truly mobile, high performance, personal computing and communication products. With innovative capabilities, 3.3V low power operation and very fast read/write performance, the LH28F020SUN-L12 is also the ideal choice for designing embedded mass storage flash memory systems.

The LH28F020SUN-L12 is a very high density, highest performance non-volatile read/write solution for solid-state storage applications. Its independently lockable 16 symmetrical blocked architecture (16-Kbyte each) extended cycling, low power operation, very fast write and read performance and selective block locking provide a highly flexible memory component suitable for high density memory cards, Resident Flash Arrays etc. The LH28F020SUN-L12's 5.0V/3.3V power supply operation enables the design of memory cards which can be read in 3.3V system and written in 5.0V/3.3V systems. Its x8 architecture allows the optimization of memory to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. Manufactured on Sharp's 0.55 µm ETOX™ process technology, the LH28F020SUN-L12 is the most cost-effective, high-density 3.3V flash memory.

* ETOX is a trademark of Intel corporation.

1.0 INTRODUCTION

The data sheet is intended to give an overview of the chip feature-set and of the operating AC/DC specifications.

1.1 Product Overview

The LH28F020SUN-L12 is a high performance 2-Mbit (2,097,152 bit) block erasable non-volatile random access memory organized as 256 Kbit x 8. The LH28F020SUN-L12 includes sixteen 16 KB (16,384) blocks. A chip memory map is shown in Figure 3.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and results in greater product reliability and ease of use.

Among the significant enhancements of the LH28F020SUN-L12:

- 3V Read, 5V Write/Erase Operation (5V V_{PP}, 3V V_{CC})
- Low Power Capability (2.7V V_{CC} Read)
- Improved Write Performance
- Dedicated Block Write/Erase Protection
- Command-Controled Memory Protection Set/Reset Capability

The LH28F020SUN-L12 will be available in a 32-lead, 2.7mm thick, 14.1mm x 20.6mm SOP package. This form factor and pinout allow for very high board layout densities.

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows Byte Writes and Block Erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the LH28F008SA 8-Mbit Flash memory.

A Superset of commands have been added to the basic LH28F008SA command-set to achieve higher write performance and provide additional capabilities. These new commands and features include:

- Software Locking of Memory Blocks
- Memory Protection Set/Reset Capability
- Two-Byte Serial Writes in 8-bit Systems
- Erase All Unlocked Blocks

Writing of memory data is performed typically within 20 µsec. A Block Erase operation erases one of the 16 blocks in typically 0.8 sec, independent of the other blocks.

LH28F020SUN-L12 allows to erase all unlocked blocks. It is desirable in case of which you have to implement Erase operation max. 16 times.

LH28F020SUN-L12 enables Two-Byte serial Write which is operated by three times command input. This feature can improve system write performance by up to typically 17 µsec per byte.

All operations are started by a sequence of Write commands to the device. Status Register (described in detail later) provide information on the progress of the requested operation.

Same as the LH28F008SA, LH28F020SUN-L12 requires an operation to complete before the next operation can be requested, also it allows to suspend block erase to read data from any other block, and allow to resume erase operation.

The LH28F020SUN-L12 provides user-selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM-Executable OS or Application Code. Each block has an associated non-volatile lock-bit which determines the lock status of the block. In addition, the LH28F020SUN-L12 has a software controled master Write Protect circuit which prevents any modifications to memory blocks whose lock-bits are set.

When the device power-up, Write Protect Set/Confirm command must be written. Otherwise, all lock bits in the device remain being locked, can't perform the Write to each block and single Block Erase. Write Protect Set/Confirm command must be written to reflect the actual lock status. However, when the device power-on, Erase All Unlocked Blocks can be used. If used, Erase is performed with reflecting actual lock status, and after that Write and Block Erase can be used.

The LH28F020SUN-L12 contains Status Register to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the LH28F008SA Flash memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the LH28F020SUN-L12 from a LH28F008SA-based design.

The LH28F020SUN-L12 is specified for a maximum access time of 120 nsec (t_{ACC}) at 3.3V operation (3.0 to 3.6V) over the commercial temperature range (0 to +70°C). A corresponding maximum access time of 160 nsec (t_{ACC}) at 2.7V (0 to +70°C) is achieved for reduced power consumption applications.

The LH28F020SUN-L12 incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching).

In APS mode, the typical I_{CC} current is 4 mA at 3.3V.

A chip reset mode of operation is enabled when whole CE#, WE# and OE# hold low more than 5 µsec. In this mode, all operations are aborted, WSM is reset and CSR register is cleared. When the device power up, this chip reset operation must be executed to initialize the control circuit, put the device in chip reset mode to protect data against noise. Especially, to assume data protection against switching noise at power up, above chip reset sequence must be executed. If CE# and or WE# and or OE# and or goes high, chip reset mode will be finished. It needs more than 620ns from one of the CE#, WE# or OE# goes high until output data are valid.

A CMOS Standby mode of operation is enabled when CE# transitions high with all input control pins at CMOS levels. In this mode, the device draws an I_{CC} standby current of 80 µA.

Please do not excute reprogramming 0 for the bit which has already been programed 0. Overwrite operation may generate unerasable bit. In case of reprogramming 0 to the data whitch has been programmed 1.

- program 0 for the bit in which you want to change data from 1 to 0.
- program 1 for the bit which has already been programmed 0.

For example, changing data from 10111101 to 10111100 requires 11111110 programming.

2.0 DEVICE PINOUT

The LH28F020SUN-L12 32-Lead SOPpinout configuration is shown in Figure 2.

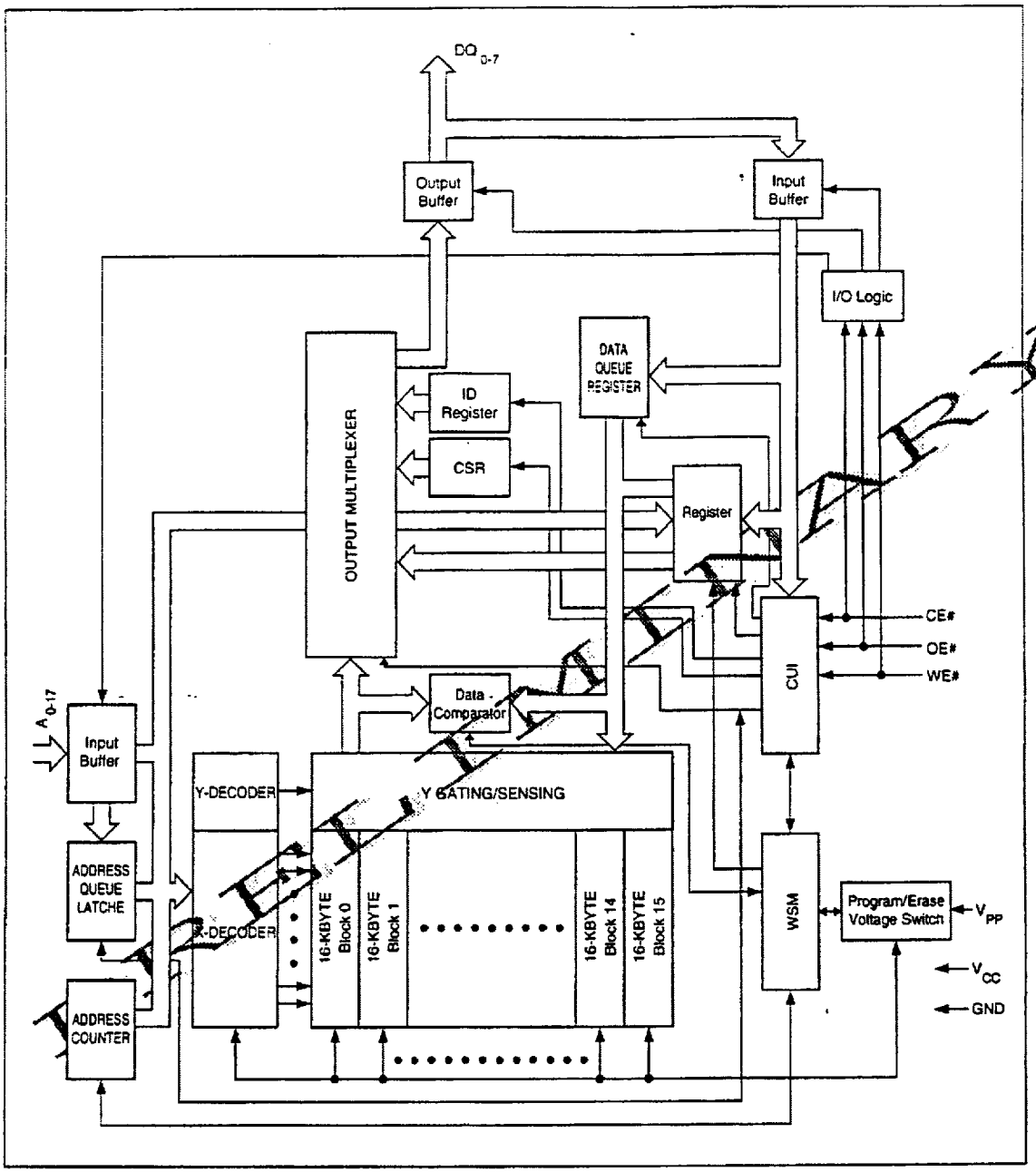


Figure 1. LH28F020SUN-L12 Block Diagram

2.1 Lead Descriptions

Symbol	Type	Name and Function
A_0-A_{13}	INPUT	**BYTE-SELECT ADDRESSES:** Select a byte within one 16-Kbyte block. These addresses are latched during Data Writes.
A_{14}-A_{17}	INPUT	**BLOCK-SELECT ADDRESSES:** Select 1 of 16 Erase blocks. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ_0-DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate Read mode. Floated when the chip is de-selected or the outputs are disabled.
CE#	INPUT	**CHIP ENABLE INPUTS:** Activate the device's control logic, input buffers, decoders and sense amplifiers. CE# must be low to select the device.
OE#	INPUT	**OUTPUT ENABLE:** Gates device data through the output buffers when low. The outputs float to tri-state off when OE# is high.
WE#	INPUT	**WRITE ENABLE:** Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. WE# is active low, and latches both address and data (command or array) on its rising edge.
V_{PP}	SUPPLY	**ERASE/WRITE POWER SUPPLY (5.0V ± 0.5V):** For erasing memory array blocks or writing words/bytes/pages into the flash array.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3V ± 0.3V):** Do not leave any power pins floating.
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.

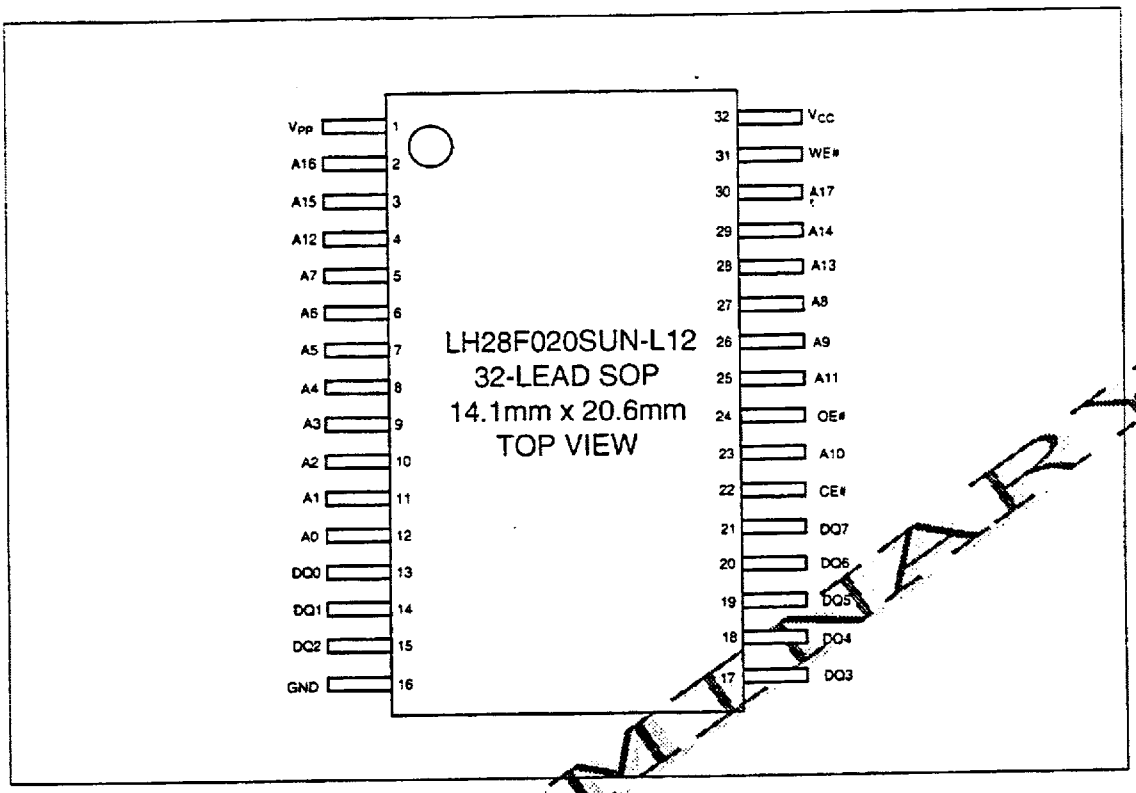


Figure 2. SOP Configuration

3.0 MEMORY MAPS

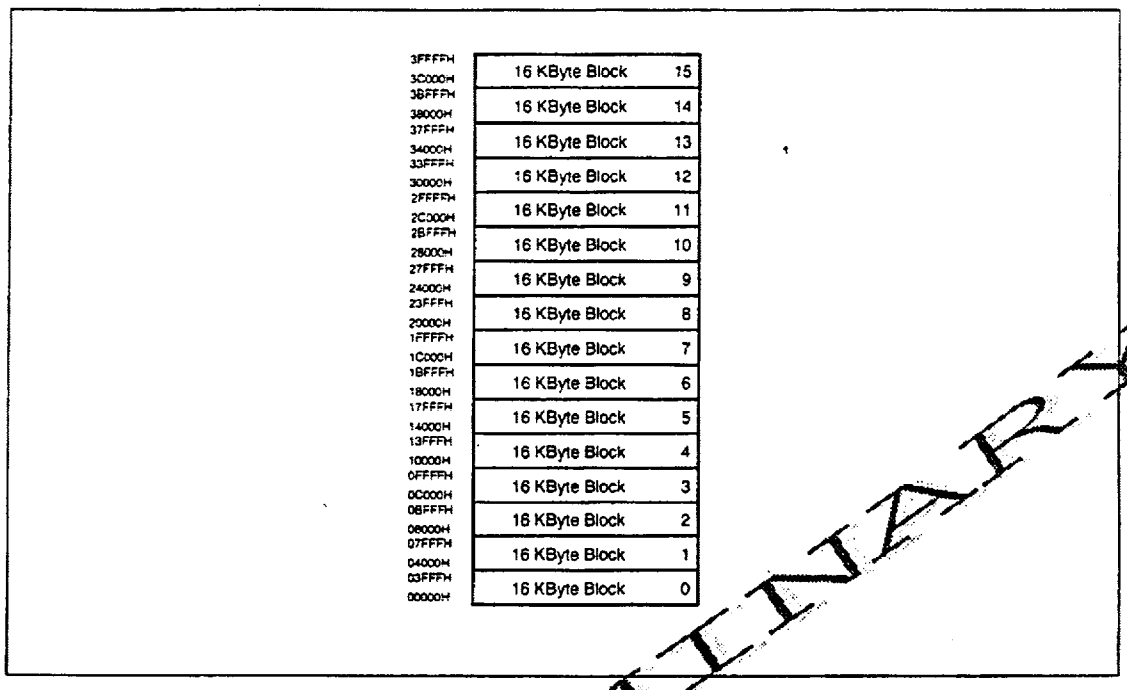


Figure 3. LH28F020SUN-L12 Memory Map

4.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

4.1 Bus Operations

Mode	Notes	CE#	OE#	WE#	A_0	DQ_{0-7}
Read	1	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Output Disable	1	V_{IL}	V_{IH}	V_{IH}	X	High Z
Standby	1	V_{IH}	X	X	X	High Z
Manufacturer ID	2	V_{IL}	V_{IL}	V_{IH}	V_{IL}	B0H
Device ID	2	V_{IL}	V_{IL}	V_{IH}	V_{IH}	31H
Write	1,3	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}

NOTES:
1. X can be V_{IH} or V_{IL} for address or control pins, which is either V_{OL} or V_{OH}.
2. A_0 at V_{IL} provide manufacturer ID codes. A_0 at V_{IH} provide device ID codes. All other addresses are set to zero.
3. Commands for different Erase operations, Data Write operations of Lock-Block operations can only be successfully completed when $V_{PP} = V_{PPH}$.

4.2 LH28F008SA-Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH	Read	AA	AD
Intelligent Identifier	1	Write	X	90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	70H	Read	X	CSRD
Clear Status Register	3	Write	X	50H			
Byte Write		Write	X	40H	Write	WA	WD
Alternate Byte Write		Write	X	10H	Write	WA	WD
Block Erase/Confirm	4	Write	X	20H	Write	BA	D0H
Erase Suspend/Resume	4	Write	X	B0H	Write	X	D0H

ADDRESS
AA = Array Address
BA = Block Address
IA = Identifier Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
CSRD = CSR Data
ID = Identifier Data
WD = Write Data

NOTES:
1. Following the intelligent identifier command, two Read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters Data Write, Erase or Suspend operations.
3. Clears CSR.3, CSR.4 and CSR.5. See Status register definitions.
4. While device performs Block Erase, if you issue Erase Suspend command (B0H), be sure to confirm ESS (Erase-Suspend-Status) is set to 1 on compatible status register. In the case, ESS bit was not set to 1, also completed the Erase (ESS=0, WSMS=1), be sure to issue Resume command (D0H) after completed next Erase command. Beside, when the Erase Suspend command is issued, while the device is not in Erase, be sure to issue Resume command (D0H) after the next erase completed.

4.3 LH28F020SUT-L15 -Performance Enhancement Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
		Op	Add	Data	Op	Add	Data	Op	Add	Data
Protect Set/Confirm	1,2,6	Write	X	57H	Write	0FFH	D0H			
Protect Reset /Confirm	3,6	Write	X	47H	Write	0FFH	D0H			
Lock Block/Confirm	1,2,4	Write	X	77H	Write	BA	D0H			
Erase All Unlocked Blocks	1,2	Write	X	A7H	Write	X	D0H			
Two-Byte Write	1,2,5	Write	X	FBH	Write	A0	WD(L,H)	Write	WA	WD(H,L)

ADDRESS
BA = Block Address
WA = Write Address

DATA
AD = Array Data
WD (L,H) = Write Data (Low, High)
WD (H,L) = Write Data (High, Low)

X = Don't Care

NOTES:
1. After initial device power-up, or chip reset is completed, the block lock status bits default to the locked state independent of the data in the corresponding lock bits. In order to upload the lock bit status, it requires to write Protect Set/Confirm command.
2. To reflect the actual lock-bit status, the Protect Set/Confirm command must be written after Lock Block/Confirm command.
3. When Protect Reset/Confirm command is written, all blocks can be written and erased regardless of the state of the lock-bits.
4. The Lock Block/Confirm command must be written after Protect Reset/Confirm command was written.
5. A_0 is automatically complemented to load second byte of data. A value determines which WD is supplied first: $A_0 = 0$ looks at the WDL, $A_0 = 1$ looks at the WDH.
6. Second bus cycle address of Protect Set/Confirm and Protect Reset/Confirm command is 0FFH. Specifically A_9-$A_8 = 0$, A_7-$A_0 = 1$, others are don't care.

4.4 Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

CSR.6 = ERASE-SUSPEND STATUS (ESS)
1 = Erase Suspended
0 = Erase in Progress/Completed

CSR.5 = ERASE STATUS (ES)
1 = Error in Block Erasure
0 = Successful Block Erase

CSR.4 = DATA-WRITE STATUS (DWS)
1 = Error in Data Write
0 = Data Write Successful

CSR.3 = V_{PP} STATUS (VPPS)
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

NOTES:

WSMS bit must be checked to determine completion of an operation (Erase Suspend, Erase or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.

If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.

The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Data Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

CSR.2-0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use and should be masked out when polling the CSR.

5.0 2M FLASH MEMORY SOFTWARE ALGORITHMS

5.1 Overview

With the advanced Command User Interface, its Performance Enhancement commands and Status Registers, the software code required to perform a given operation may become more intensive but it will result in much higher write/erase performance compared with current flash memory architectures.

The software flowcharts describing how a given operation proceeds are shown here. Figures 5-1 through 5-3 depict flowcharts using the 2nd generation flash device in the LH28F008SA-compatible mode. Figures 5-4 through 5-9 depict flowcharts using the 2nd generation flash device's performance enhancement commands mode.

When the device power-up or reset is completed, all blocks come up locked. Therefore, Byte Write, Two Byte Serial Write and Block Erase can not be performed in each block. However, at that time, Erase All Unlocked Block is performed normally, if used, and reflect actual lock status, also the unlocked block data is erased. When the device power-up or reset is completed, Set Write Protect command must be written to reflect actual block lock status.

Reset Write Protect command must be written before Write Block Lock command. To reflect actual block lock status, Set Write Protect command is succeeded.

The Compatible Status Register (CSR) is used to determine which blocks are locked. In order to see Lock Status of certain block, a Byte Write command (WA=Block Address, WD=FFH) is written to the CUI, after issuing Set Write Protect command. If CSR7, CSR5 and CSR4 (WSMS, ES and DWS) are set to "1"s, the block is locked. If CSR7 is set to "1", the block is not locked.

Reset Write Protect command enables Write/Erase operation to each block.

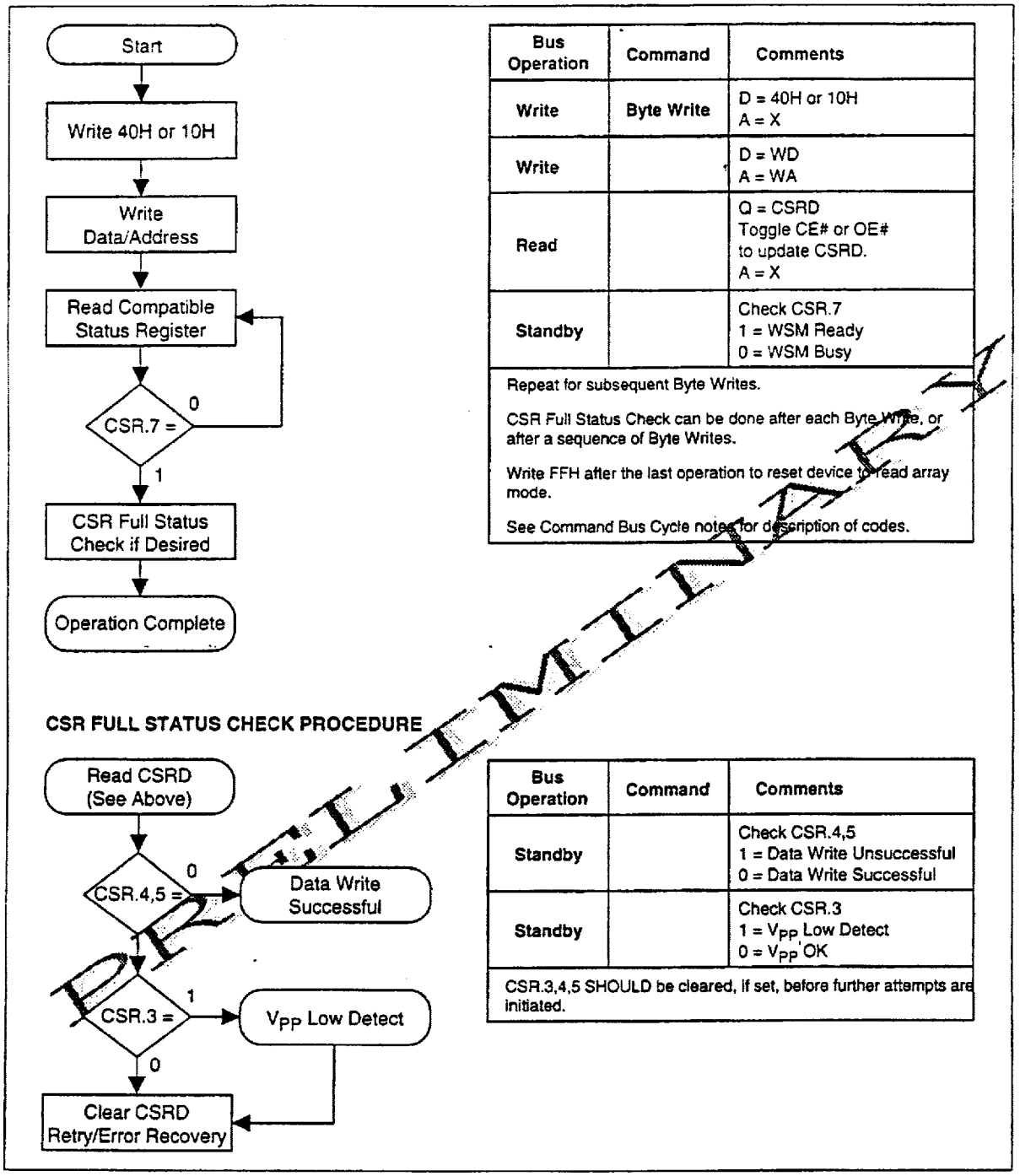
In the case of Block Erase is performed, the block lock information is also erased. Block Lock command and Set Write Protect command must be written to prohibit Write/Erase operation to each block.

There are unassigned commands. It is not recommended that the customer use any command other than the valid commands specified in Chapter 4 "Command Bus Definitions". Sharp reserved the right to redefine these codes for future functions.

5.2 2M Flash Memory Algorithm Flowcharts

The following flowcharts describe the 2nd generation flash device modes of operation:

Figure 5-1	Byte Writes with Compatible Status Register
Figure 5-2	Block Erase with Compatible Status Register
Figure 5-3	Erase Suspend to Read Array with Compatible Status Register
Figure 5-4	Block Locking
Figure 5-5	Updating Data in a Locked Block
Figure 5-6	Two-Byte Serial Writes with Compatible Status Registers
Figure 5-7	Erase All Unlocked Blocks with Compatible Status Registers
Figure 5-8	Set Write Protect
Figure 5-9	Reset Write Protect



Bus Operation	Command	Comments
Write	Byte Write	D = 40H or 10H A = X
Write		D = WD A = WA
Read		Q = CSRD Toggle CE# or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent Byte Writes.

CSR Full Status Check can be done after each Byte Write, or after a sequence of Byte Writes.

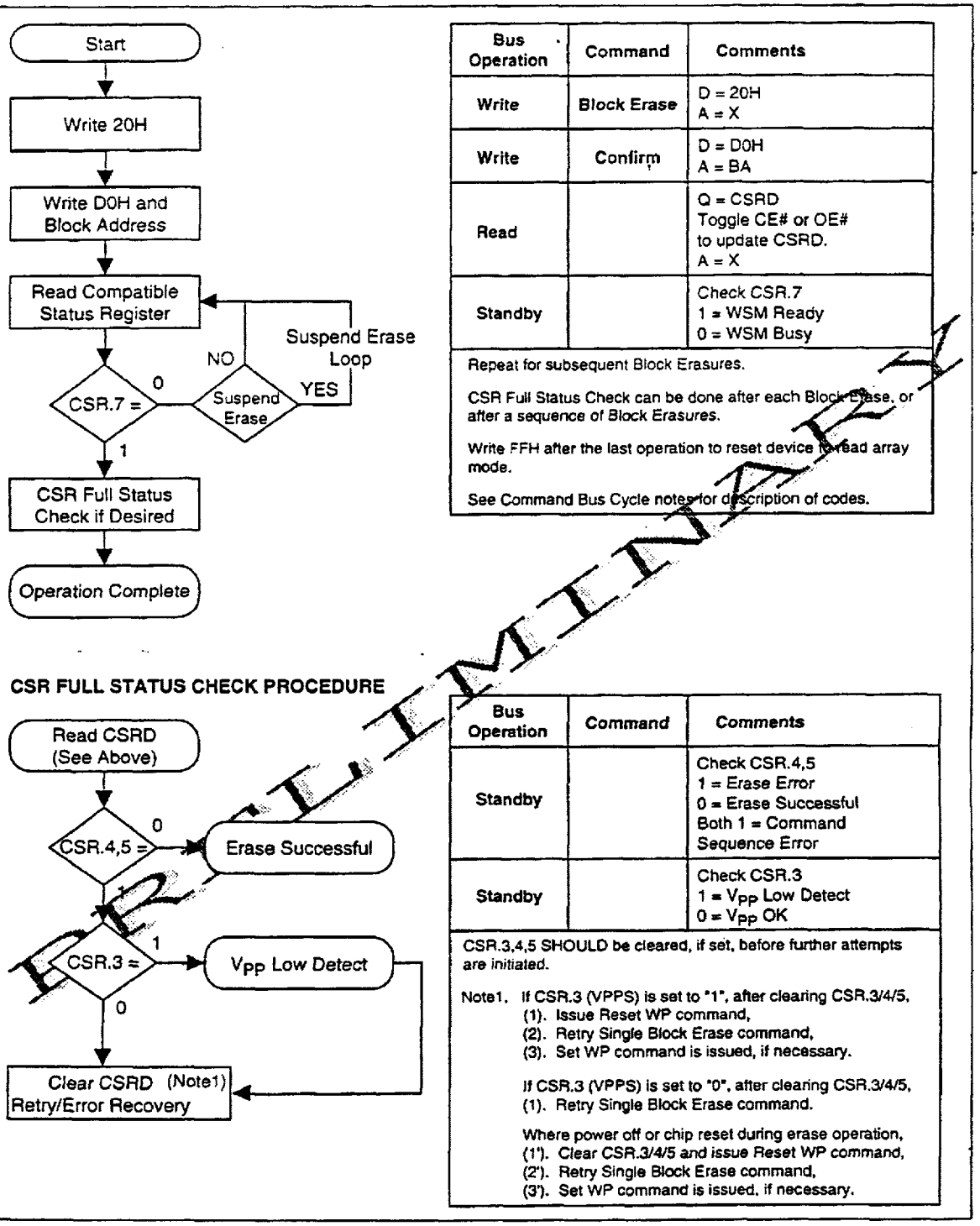
Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

Bus Operation	Command	Comments
Standby		Check CSR.4,5 1 = Data Write Unsuccessful 0 = Data Write Successful
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK

CSR.3,4,5 SHOULD be cleared, if set, before further attempts are initiated.

Figure 5-1. Byte Writes with Compatible Status Register



Bus Operation	Command	Comments
Write	Block Erase	D = 20H A = X
Write	Confirm	D = D0H A = BA
Read		Q = CSRD Toggle CE# or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent Block Erasures.

CSR Full Status Check can be done after each Block Erase, or after a sequence of Block Erasures.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

Bus Operation	Command	Comments
Standby		Check CSR.4,5 1 = Erase Error 0 = Erase Successful Both 1 = Command Sequence Error
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK

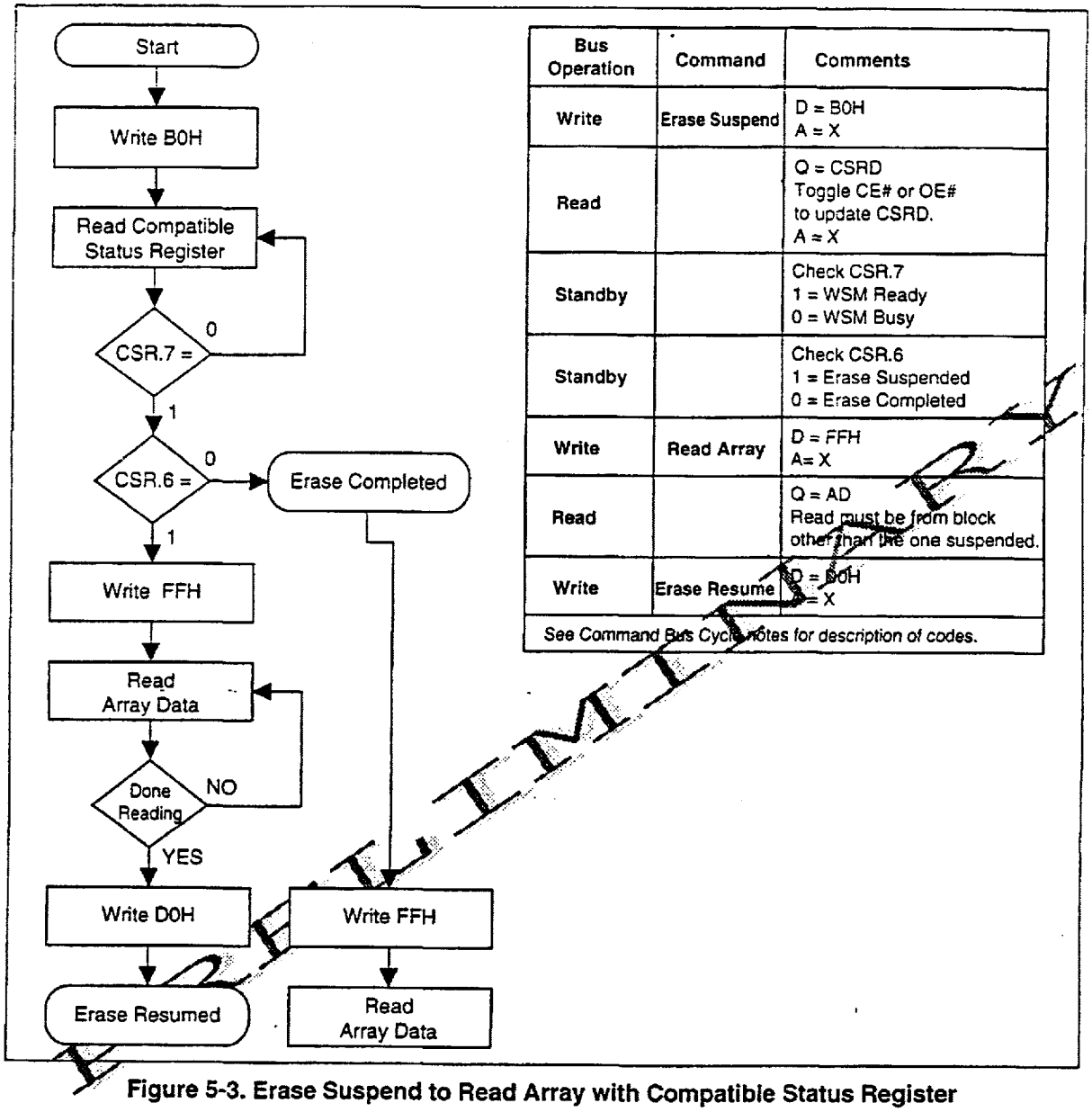
CSR.3,4,5 SHOULD be cleared, if set, before further attempts are initiated.

Note1. If CSR.3 (VPPS) is set to "1", after clearing CSR.3/4/5,
(1). Issue Reset WP command,
(2). Retry Single Block Erase command,
(3). Set WP command is issued, if necessary.

If CSR.3 (VPPS) is set to "0", after clearing CSR.3/4/5,
(1). Retry Single Block Erase command.

Where power off or chip reset during erase operation,
(1'). Clear CSR.3/4/5 and issue Reset WP command,
(2'). Retry Single Block Erase command,
(3'). Set WP command is issued, if necessary.

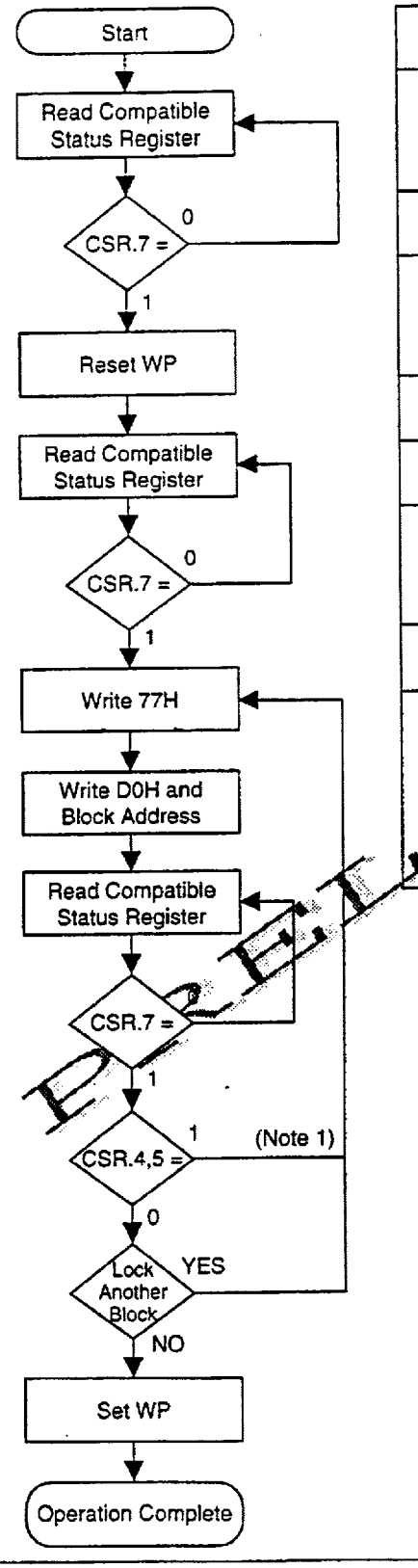
Figure 5-2. Block Erase with Compatible Status Register



Bus Operation	Command	Comments
Write	Erase Suspend	D = B0H A = X
Read		Q = CSRD Toggle CE# or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check CSR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	D = FFH A= X
Read		Q = AD Read must be from block other than the one suspended.
Write	Erase Resume	D = D0H A = X

See Command Bus Cycle Notes for description of codes.

Figure 5-3. Erase Suspend to Read Array with Compatible Status Register



Bus Operation	Command	Comments
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	Reset Write Protect	After Write D = 47H A = X, Write D = D0H A = 0FFH
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	Lock Block	D = 77H A = X
Write	Confirm	D = D0H A = BA
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	Set Write Protect	After Write D = 57H A = X, Write D = D0H A = 0FFH

Note 1. See CSR Full Status Check for Data-Write operation.

If CSR.4,5 is set, as it is command sequence error, SHOULD be cleared before further attempts are initiated.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Definitions for description of codes.

Figure 5-4. Block Locking

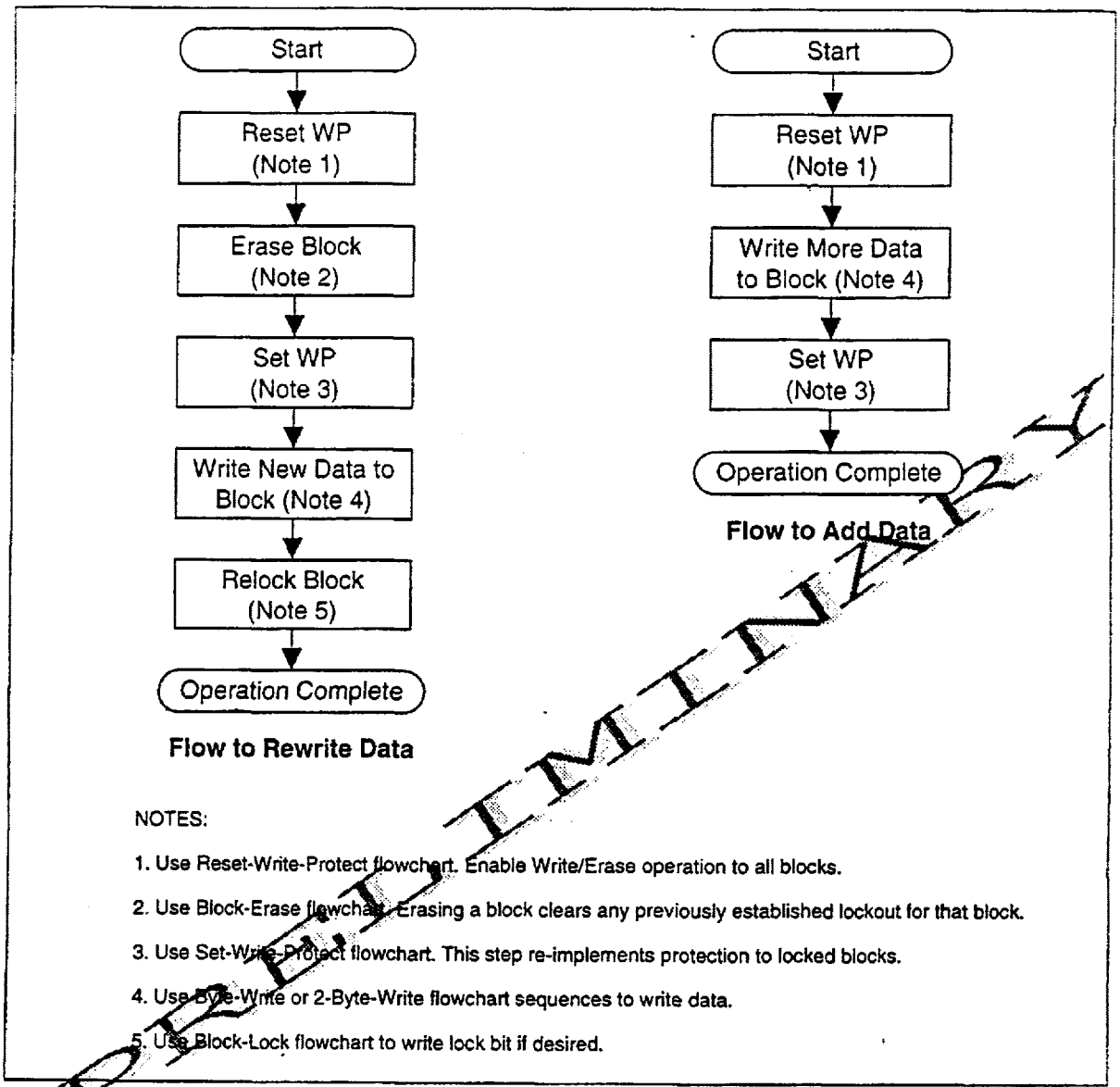
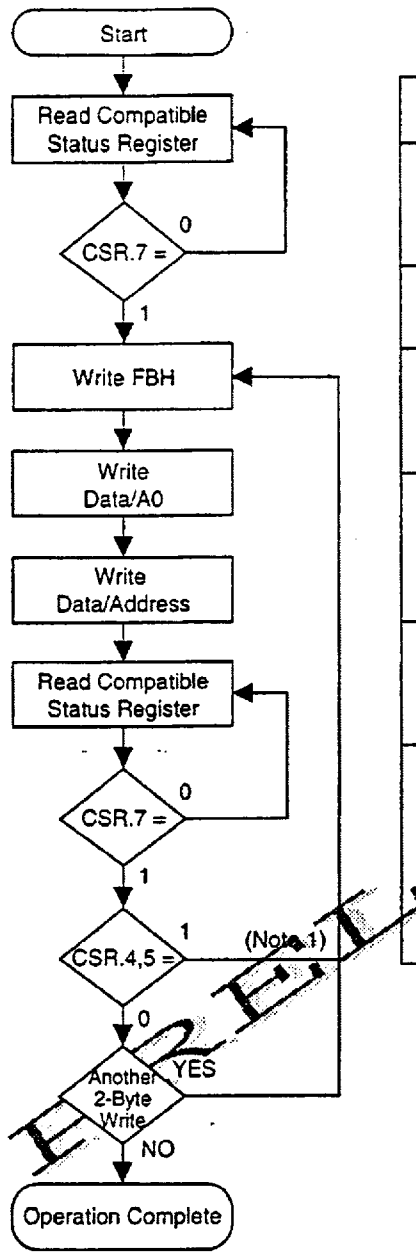


Figure 5-5. Updating Data in a Locked Block



Bus Operation	Command	Comments
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	2-Byte Write	D = FBH A = X
Write		D = WD A0 = 0 loads low byte of Data Register. A0 = 1 loads high byte of Data Register. Other Addresses = X
Write		D = WD A = WA Internally, A0 is automatically complemented to load the alternate byte location of the Data Register.
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy

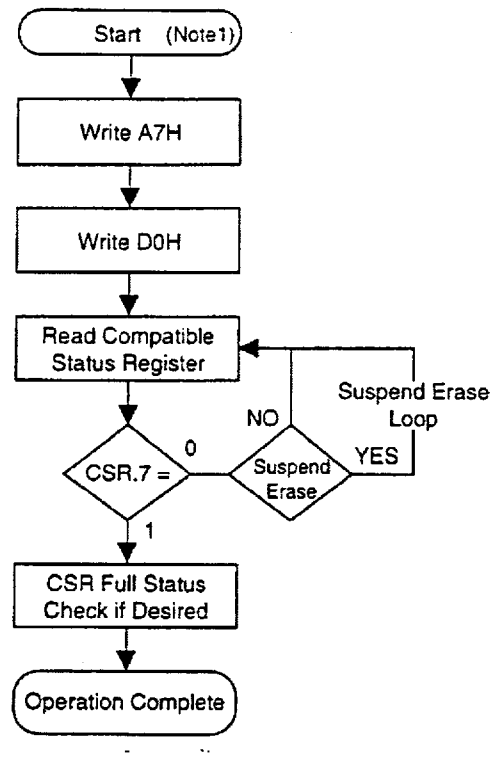
Note 1. If CSR.4,5 is set, as it is command sequence error, SHOULD be cleared before further attempts are initiated.

CSR Full Status Check can be done after each 2-Byte Write, or after a sequence of 2-Byte Writes.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

Figure 5-6. Two-Byte Serial Writes with Compatible Status Registers



Bus Operation	Command	Comments
Write	Erase All Unlocked Block	D = A7H A = X
Write	Confirm	D = D0H A = X
Read		Q = CSRD Toggle CE# or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

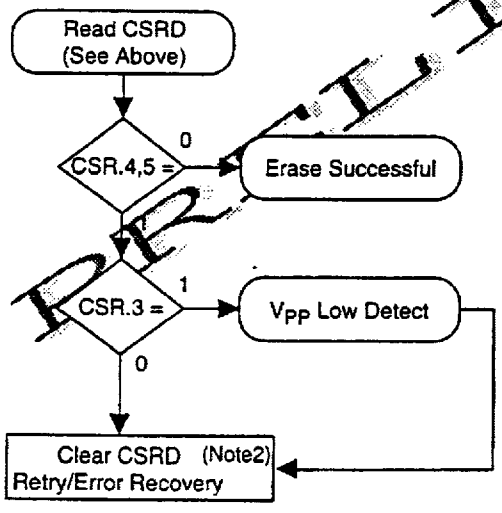
CSR Full Status Check can be done after Erase All Unlocked Block, or after a sequence of Erasures.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

Note1. Where power off or chip reset during erase operation,
(1). Clear CSR.3/4/5 and issue Reset WP command,
(2). Retry Erase All Unlocked Block Erase command to erase all blocks, or issue Single Block Erase to erase all of the unlocked blocks in sequence,
(3). Set WP command is issued, if necessary.

CSR FULL STATUS CHECK PROCEDURE



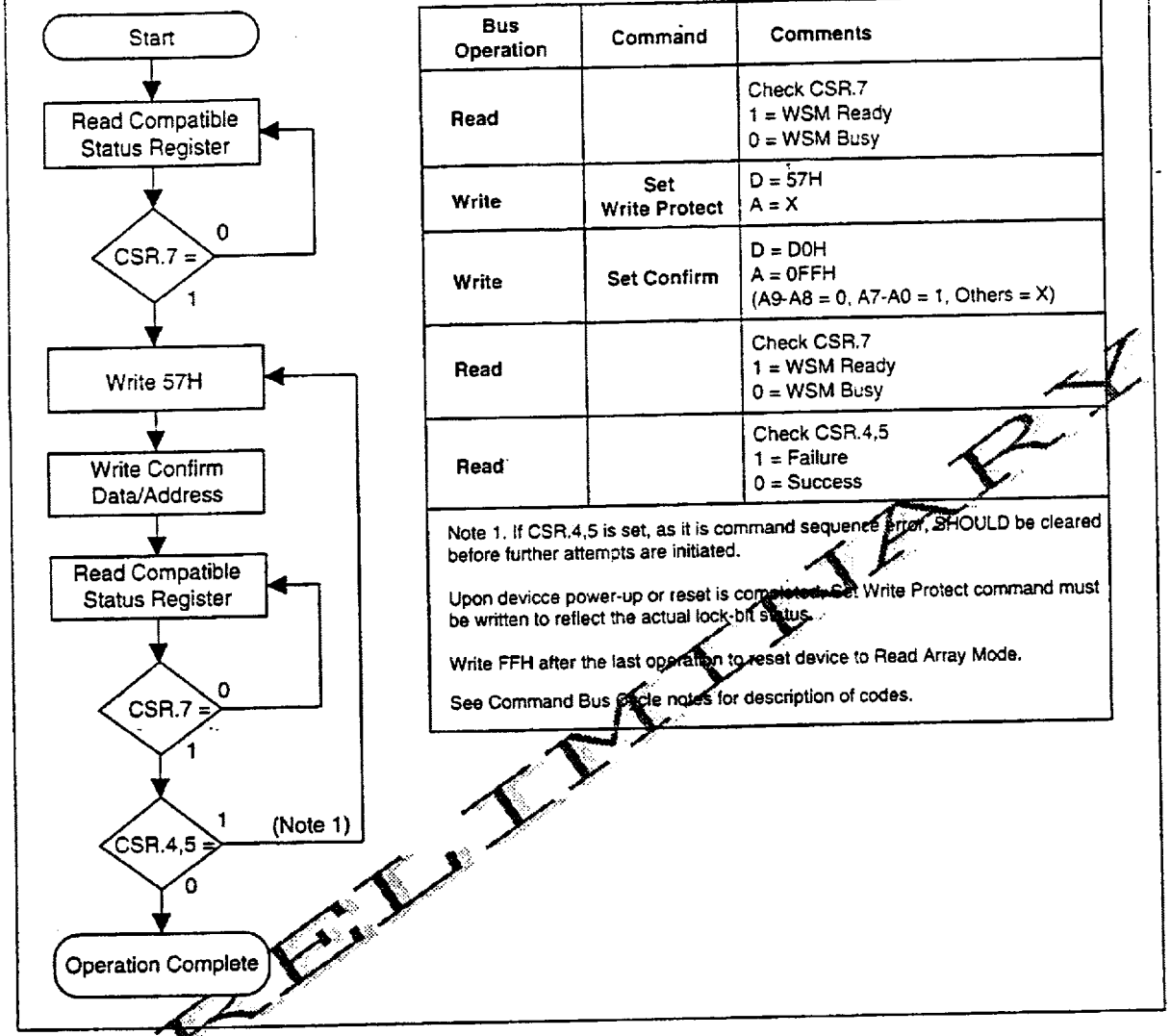
Bus Operation	Command	Comments
Standby		Check CSR.4,5 1 = Erase Error 0 = Erase Successful Both 1 = Command Sequence Error
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK

CSR.3,4,5 SHOULD be cleared, if set, before further attempts are initiated.

Note 2. If CSR.3 (VPPS) is set to "1", after clearing CSR.3/4/5,
(1). Issue Reset WP command,
(2). Retry Erase All Unlocked Block Erase command to erase all blocks, or issue Single Block Erase to erase all of the unlocked blocks in sequence,
(3). Set WP command is issued, if necessary.

If CSR.3 (VPPS) is set to "0", after clearing CSR.3/4/5,
(1). Retry Erase All Unlocked Block Erase command.

Figure 5-7. Erase All Unlocked Blocks with Compatible Status Registers



Bus Operation	Command	Comments
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Write	Set Write Protect	D = 57H A = X
Write	Set Confirm	D = D0H A = 0FFH (A9-A8 = 0, A7-A0 = 1, Others = X)
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Read		Check CSR.4,5 1 = Failure 0 = Success

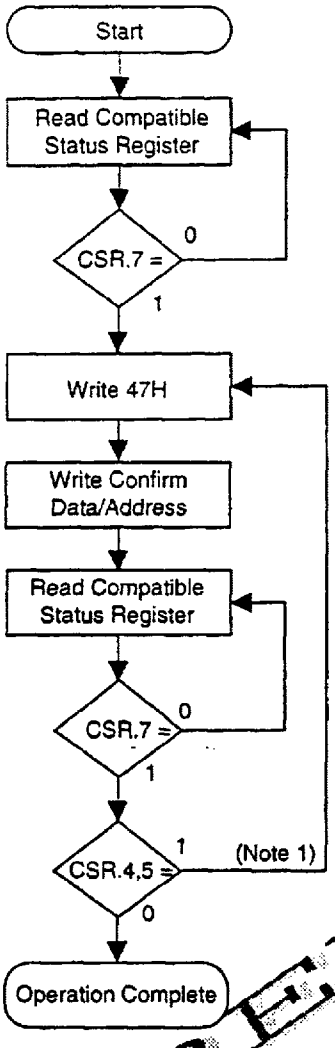
Note 1. If CSR.4,5 is set, as it is command sequence error, SHOULD be cleared before further attempts are initiated.

Upon devicce power-up or reset is completed, Set Write Protect command must be written to reflect the actual lock-bit status.

Write FFH after the last operation to reset device to Read Array Mode.

See Command Bus Cycle notes for description of codes.

Figure 5-8. Set Write Protect



Bus Operation	Command	Comments
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Write	Reset Write Protect	D = 47H A = X
Write	Reset Confirm	D = D0H A = 0FFH (A9-A8 = 0, A7-A0 = 1, Others = X)
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Read		Check CSR.4,5 1 = Unsuccessful 0 = Success

Note 1. If CSR.4,5 is set, as it is command sequence error, SHOULD be cleared before further attempts are initiated.

Reset Write Protect command enables Write/Erase operation to all blocks.

Write FFH after the last operation to reset device to Read Array Mode.

See Command Bus Cycle notes for description of codes.

Figure 5-9. Reset Write Protect

6.0 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to + 80°C
Storage Temperature ..... - 65°C to + 125°C

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	- 0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2	- 0.2	7.0	V	
V	Voltage on any Pin (except V_{CC}, V_{PP}) with Respect to GND	2	- 0.5	Vcc +0.5	V	
I	Current into any Non-Supply Pin			± 30	mA	
I_{OUT}	Output Short Circuit Current	3		100	mA	

NOTES:
1. Operating temperature is for commercial product defined by this specifications.
2. Minimum DC voltage is - 0.5V on input/output pins. During transitions, this level may undershoot to - 2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Capacitance

Symbol	Parameter	Note	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	7	10	pF	T_A = 25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	9	12	pF	T_A = 25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1		50	pF	For V_{CC} = 3.3V ± 0.3V
	Equivalent Testing Load Circuit Vcc ± 10%			2.5	ns	50Ω transmission line delay

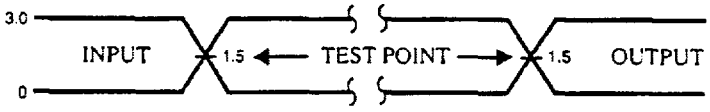
NOTE:
1. Sampled, not 100% tested.

6.3 Timing Nomenclature

For 3.3V systems use 1.5V cross point definitions.
Each timing parameter consists of 5 characters. Some common examples are defined below:

t_{CE} t_{ELQV} time(t) from CE# (E) going low (L) to the outputs (Q) becoming valid (V)
t_{OE} t_{GLQV} time(t) from OE# (G) going low (L) to the outputs (Q) becoming valid (V)
t_{ACC} t_{AVQV} time(t) from address (A) valid (V) to the outputs (Q) becoming valid (V)
t_{AS} t_{AVWH} time(t) from address (A) valid (V) to WE# (W) going high (H)
t_{DH} t_{WHDX} time(t) from WE# (W) going high (H) to when the data (D) can become undefined (X)

	Pin Characters		Pin States
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	CE# (Chip Enable)	X	Driven, but not necessarily valid
G	OE# (Output Enable)	Z	High Impedance
W	WE# (Write Enable)		
V	Any Voltage Level		
3V	V_{CC} at 3.0V Minimum		



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10 ns.

Figure 4. Transient Input/Output Reference Waveform (V_{CC} = 3.3V)

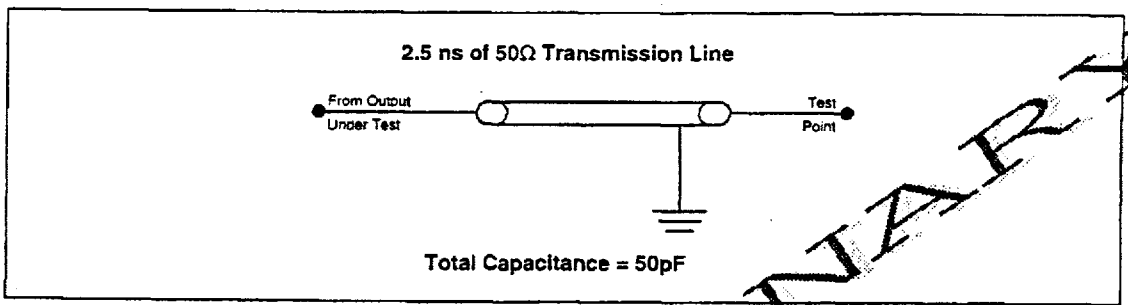


Figure 5. Transient Equivalent Testing Load Circuit (V_{CC} = 3.3V)

6.4 DC Characteristics

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			± 1	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1			± 10	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,4			80	µA	V_{CC} = V_{CC} Max, CE# = V_{CC} ± 0.2V
				0.3	4	mA	V_{CC} = V_{CC} Max, CE# = V_{IH}
$I_{CCR}1$	V_{CC} Read Current	1,3,4			35	mA	V_{CC} = V_{CC} Max, CMOS: CE# = GND ± 0.2V Inputs = GND ± 0.2V or V_{CC} ± 0.2V, TTL: CE# = V_{IL}, Inputs = V_{IL} or V_{IH}, f = 10 MHz, I_{OUT} = 0 mA
$I_{CCR}2$	V_{CC} Read Current	1,3,4		10	20	mA	V_{CC} = V_{CC} Max, CMOS: CE# = GND ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V, TTL: CE# = V_{IL} Inputs = V_{IL} or V_{IH}, f = 5 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Write Current	1		8	18	mA	Byte/Two-Byte Serial Write in Progress
I_{CCE}	V_{CC} Block Erase Current	1		6	12	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		3	6	mA	CE# =V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby Current	1			± 10	µA	V_{PP} ≤ V_{CC}

DC Characteristics (Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{PPR}	V_{PP} Read Current	1			200	µA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Write Current	1		15	35	mA	$V_{PP} = V_{PPH}$, Byte/Two-Byte Serial Write in Progress
I_{PPE}	V_{PP} Erase Current	1		20	40	mA	$V_{PP} = V_{PPH}$, Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1			200	µA	$V_{PP} = V_{PPH}$, Block Erase Suspended
V_{IL}	Input Low Voltage		- 0.3		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage				0.4	V	$V_{CC} = V_{CC}$ Min and I_{OL} = 4 mA
$V_{OH}1$	Output High Voltage		2.4			V	I_{OH} = - 2 mA, $V_{CC} = V_{CC}$ Min
$V_{OH}2$			V_{CC} - 0.2			V	I_{OH} = - 100 µA, $V_{CC} = V_{CC}$ Min
V_{PPL}	V_{PP} during Normal Operations		0.0		5.5	V	
V_{PPH}	V_{PP} during Write/ Erase Operations		4.5	5.0	5.5	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		1.4			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3V, V_{PP} = 5.0V, T = 25°C.
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Automatic Power Saving (APS) reduces I_{CCR} to less than 4 mA in Static operation.
4. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.

6.5 AC Characteristics - Read Only Operations[1]

V_{CC} = 3.3V ± 0.3V, T_A =0°C to +70°C

Symbol	Parameter	Notes	Min	Max	Units
t_{AVAV}	Read Cycle Time		120		ns
t_{AVGL}	Address Setup to OE# Going Low	3	0		ns
t_{AVQV}	Address to Output Delay			120	ns
t_{ELQV}	CE# to Output Delay	2		120	ns
t_{GLQV}	OE# to Output Delay	2		45	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# to Output in High Z	3		50	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# to Output in High Z	3		30	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns

NOTES:
1. See AC Input/Output Reference Waveforms for timing measurements. Figure 4.
2. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.

6.5 AC Characteristics - Read Only Operations[1] (Continued)

V_{CC} = 2.85V ± 0.15V, T_A =0°C to -70°C

Symbol	Parameter	Notes	Min	Max	Units
t_{AVAV}	Read Cycle Time		160		ns
t_{AVGL}	Address Setup to OE# Going Low	3	0		ns
t_{AVQV}	Address to Output Delay			160	ns
t_{ELQV}	CE# to Output Delay	2		160	ns
t_{GLQV}	OE# to Output Delay	2		55	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# to Output in High Z	3		60	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# to Output in High Z	3		50	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns

NOTES:
1. See AC Input/Output Reference Waveforms for timing measurements, Figure 4.
2. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.

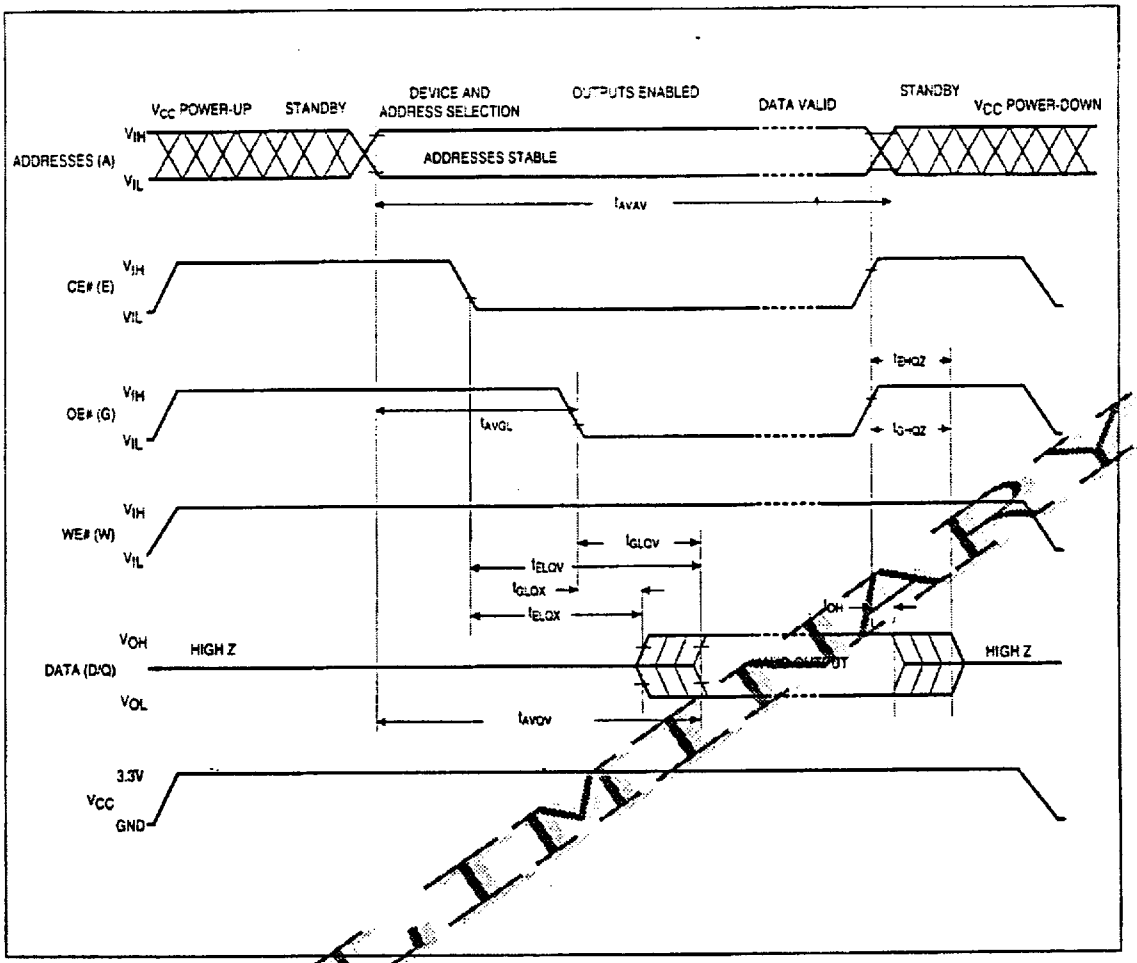


Figure 6. Read Timing Waveforms

6.6 Power-Up and Reset Timings

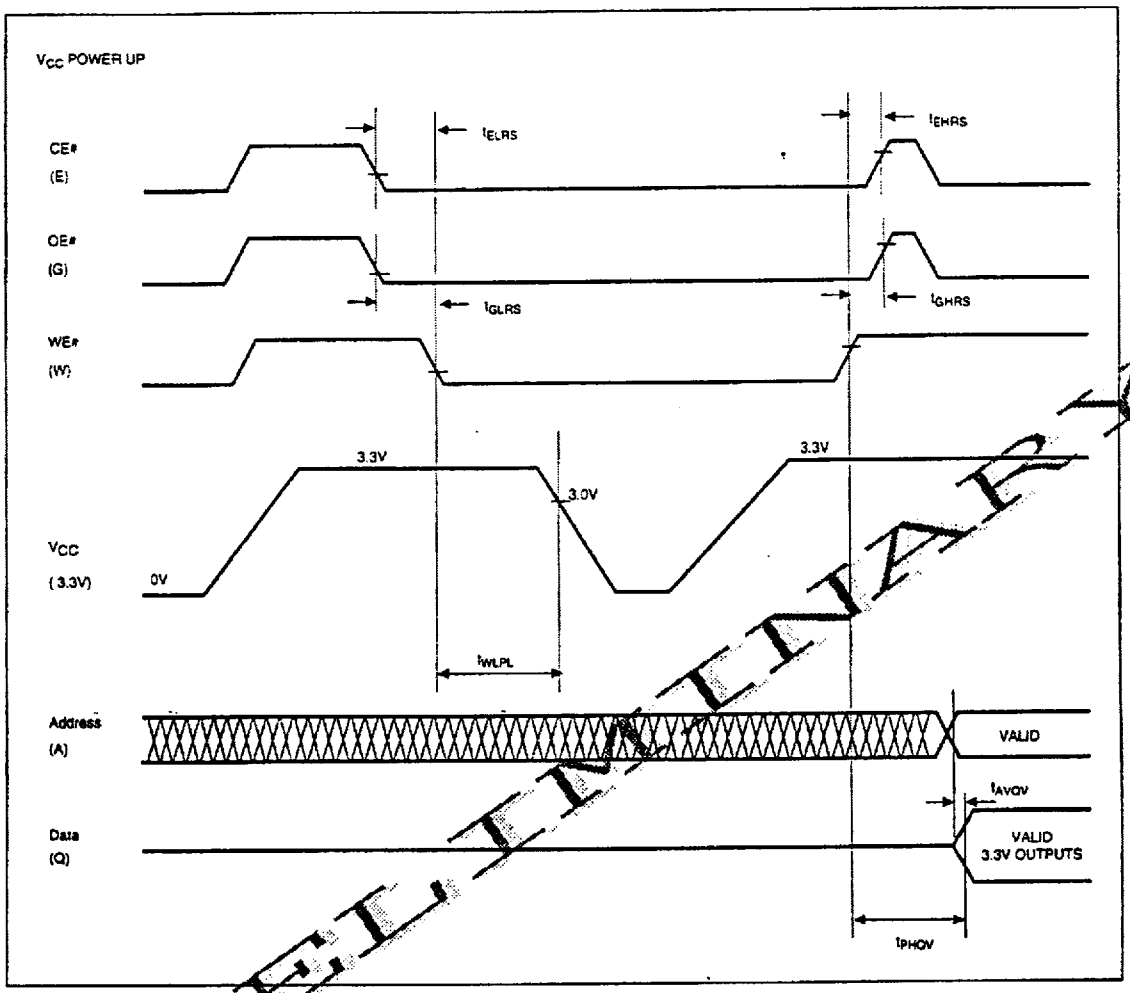


Figure 7. V_{CC} Power-Up and Reset Waveforms

Symbol	Parameter	Note	Min	Max	Unit
t_{WLPL}	WE# Low to V_{CC} at 3.0V Minimum	1	5		µs
t_{AVQV}	Address Valid to Data Valid for V_{CC} = 3.3V ± 0.3V	2		120	ns
t_{PHQV}	WE# High to Data Valid for V_{CC} = 3.3V ± 0.3V	2		620	ns
t_{ELRS}	CE# Setup to WE# Going Low		100		ns
t_{GLRS}	OE# Setup to WE# Going Low		100		ns
t_{EHRS}	CE# Hold from WE# Going High		100		ns
t_{GHRS}	OE# Hold from WE# Going High		100		ns

NOTES:
CE# and OE# are switched low after Power-Up.

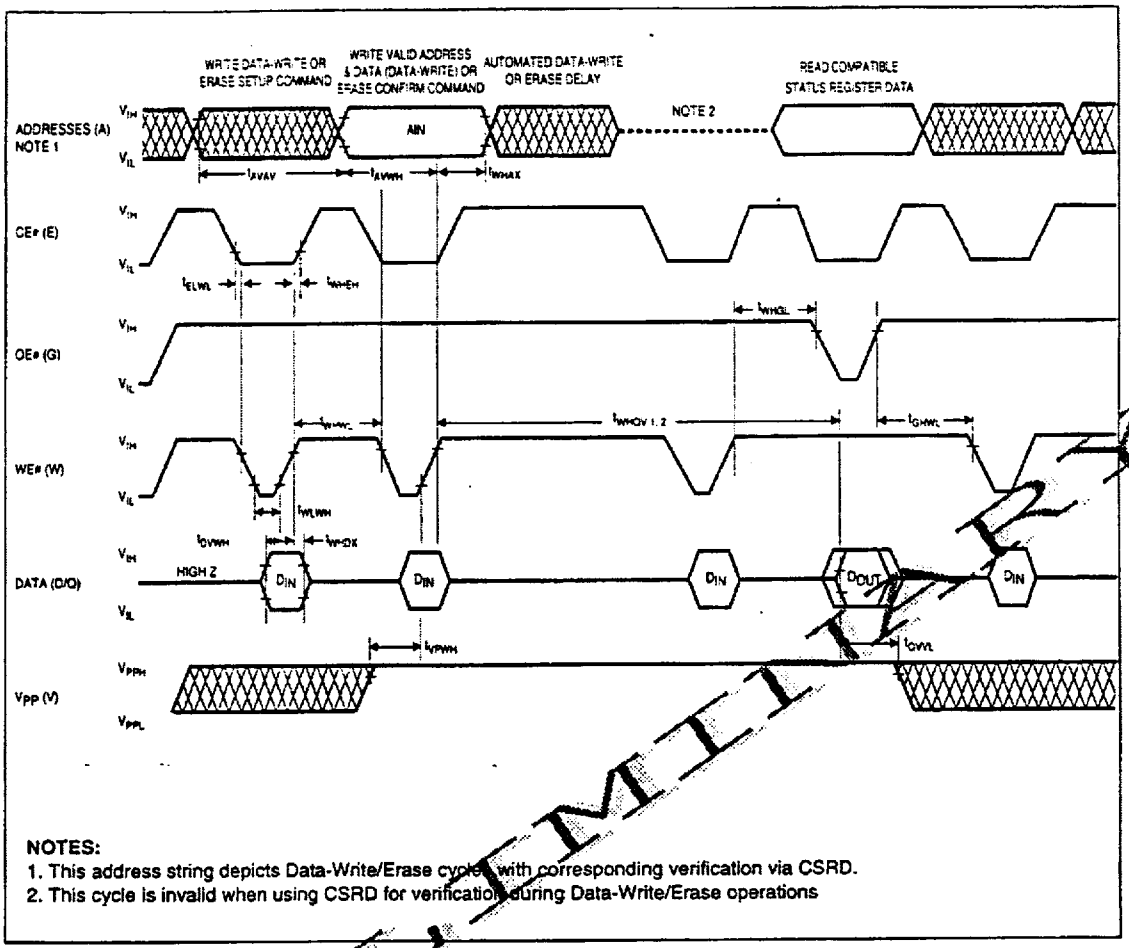
1. Chip reset is enabled when the low state of all CE#, OE# and WE# exceeds 5 µs. Especialy when you will power on the chip, excute an above chip reset sequence for a protection from noise.
2. These values are shown for 3.3V V_{CC} operation. Refer to the AC Characteristics Read Only Operations also.

6.7 AC Characteristics for WE# - Controlled Command Write Operations[1]

V_{CC} = 3.3 ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{AVAV}	Write Cycle Time		120			ns
t_{VPWH}	V_{PP} Setup to WE# Going High	3	100			ns
t_{ELWL}	CE# Setup to WE# Going Low		10			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	100			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	100			ns
t_{WLWH}	WE# Pulse Width		100			ns
t_{WHDX}	Data Hold from WE# High	2	5			ns
t_{WHAX}	Address Hold from WE# High	2	5			ns
t_{WHEH}	CE# Hold from WE# High		5			ns
t_{WHWL}	WE# Pulse Width High		60			ns
t_{GHWL}	Read Recovery before Write		0			ns
t_{WHGL}	Write Recovery before Read		95			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register Data		0			µs
$t_{WHQV}1$	Duration of Byte Write Operation	4,5	8	20		µs
$t_{WHQV}2$	Duration of Block Erase Operation	4	0.3			s

NOTES:
1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Byte write operations are typically performed with 1 programming Pulse.
6. Address and Data are latched on the rising edge of WE# for all Command Write operations.



NOTES:
1. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
2. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations

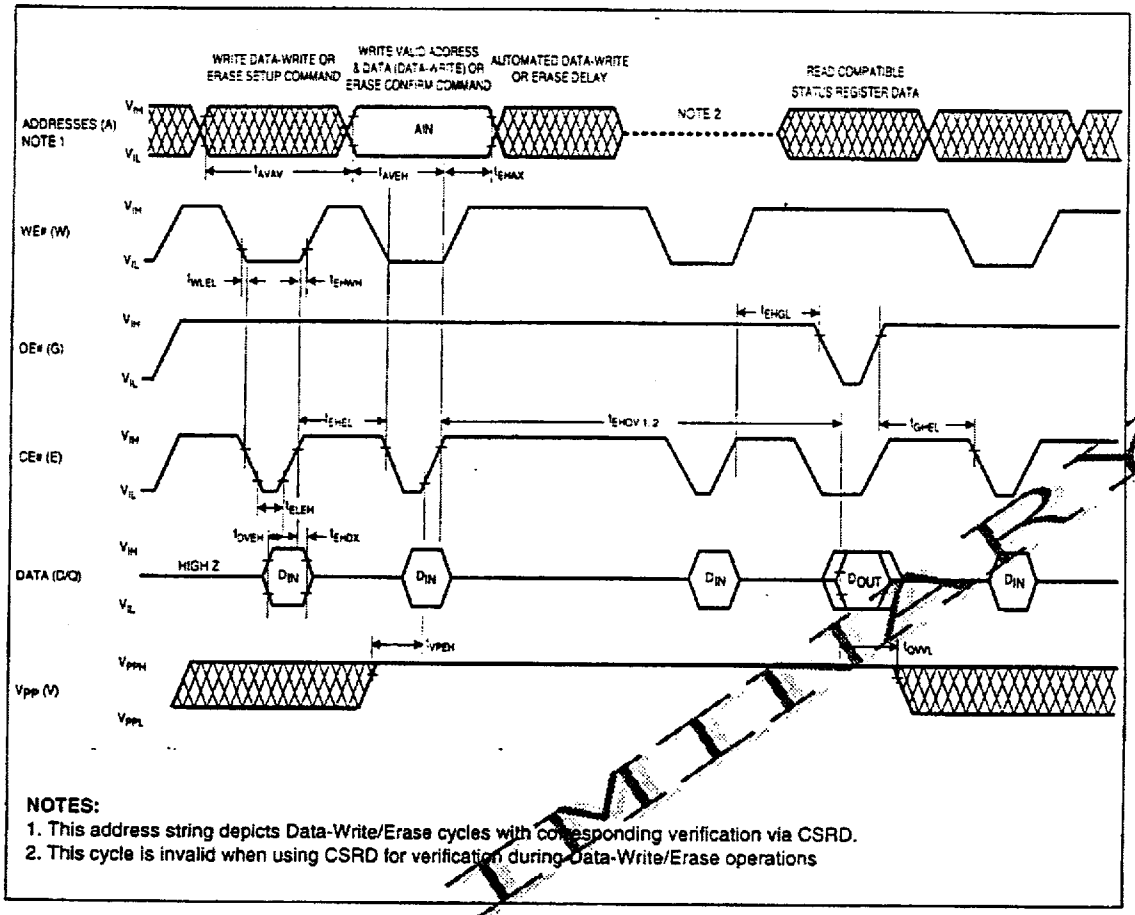
Figure 8. AC Waveforms for Command Write Operations

6.8 AC Characteristics for CE# - Controlled Command Write Operations[1]

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{AVAV}	Write Cycle Time		120			ns
t_{VPEH}	V_{PP} Setup to CE# Going High	3	100			ns
t_{WLEL}	WE# Setup to CE# Going Low		0			ns
t_{AVEH}	Address Setup to CE# Going High	2,6	100			ns
t_{DVEH}	Data Setup to CE# Going High	2,6	100			ns
t_{ELEH}	CE# Pulse Width		100			ns
t_{EHDX}	Data Hold from CE# High	2	5			ns
t_{EHAX}	Address Hold from CE# High	2	5			ns
t_{EHWH}	WE# Hold from CE# High		5			ns
t_{EHEL}	CE# Pulse Width High		60			ns
t_{GHEL}	Read Recovery before Write		0			ns
t_{EHGL}	Write Recovery before Read		95			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register Data		0			µs
t_{EHQV1}	Duration of Byte Write Operation	4,5	8	20		µs
t_{EHQV2}	Duration of Block Erase Operation	4	0.3			s

NOTES:
1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of CE# for all Command Write Operations.



NOTES:
1. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
2. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations

Figure 9. Alternate $\overline{CE}$ Waveforms for Command Write Operations

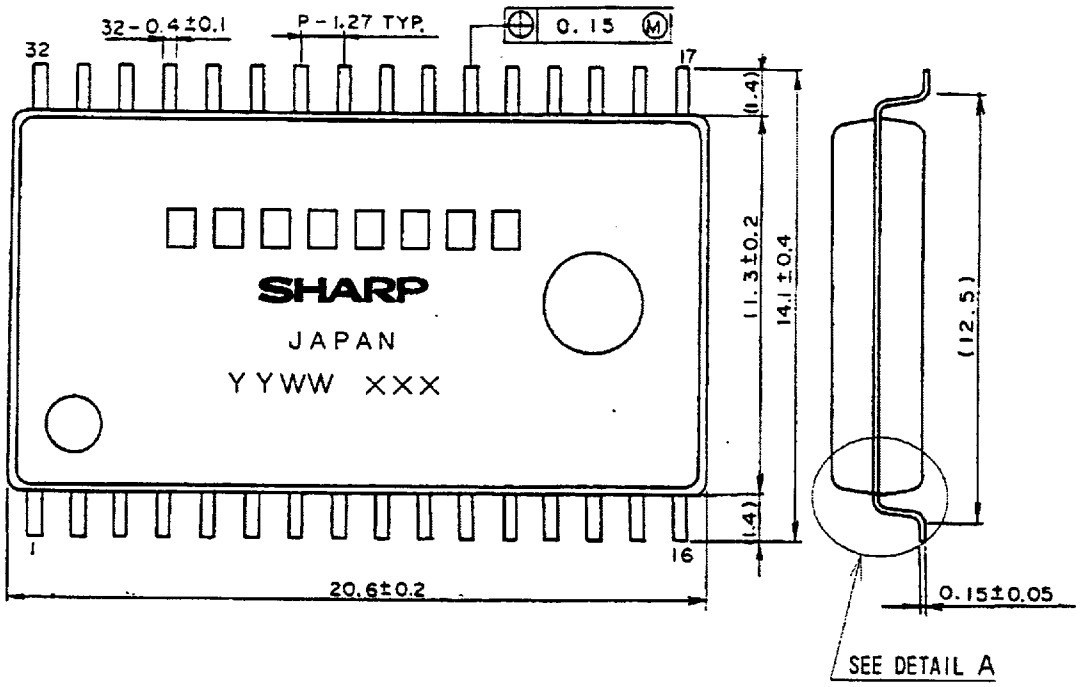
6.9 Erase and Byte Write Performance

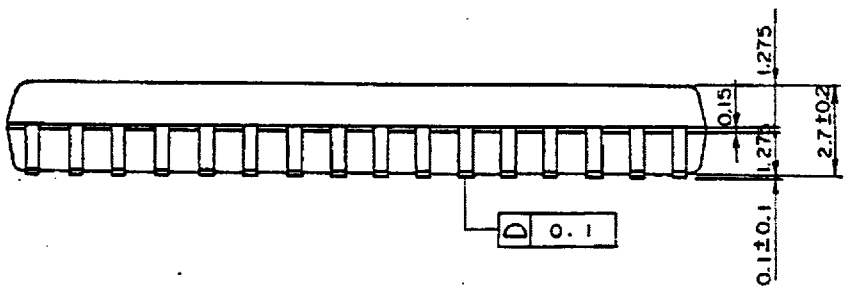
V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
$t_{WHRH}1$	Byte Write Time	2		20		µs	
$t_{WHRH}2$	Two-Byte Serial Write Time	2		34		µs	
$t_{WHRH}3$	16KB Block Write Time	2		0.33	1.3	s	Byte Write Mode
$t_{WHRH}4$	16KB Block Write Time	2		0.3	1.1	s	Two-Byte Serial Write Mode
	Block Erase Time (16KB)	2		0.8	10	s	
	Full Chip Erase Time	2,3		9-15		s	

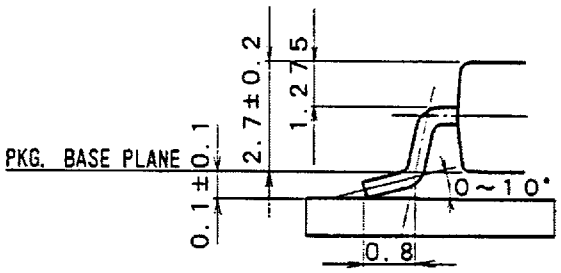
NOTES:
1. 25°C, V_{PP} = 5.0V.
2. Excludes System-Level Overhead.
3. Depends on the number of protected blocks.

SHARP



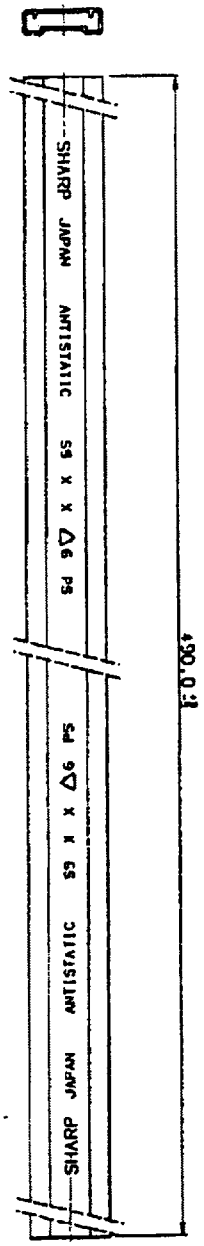


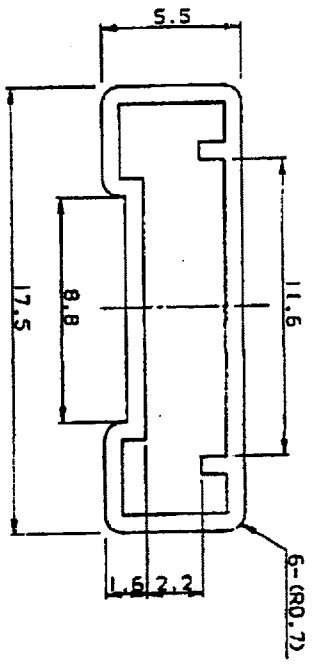
DETAIL A



名称 NAME	SOP32-P-525	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE プラスチックパッケージ外形寸法は、バリをさまないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1021	単位 UNIT	mm	

SHARP





注記 ：マガジン(スリーブ)両側のストッパーは、ゴムストッパーとする。
指示無き寸法公差は全て±０．４ｍｍとする。

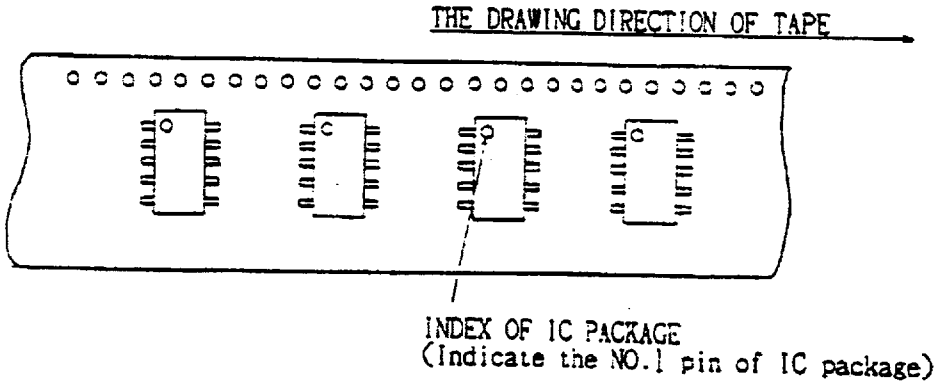
NOTES : Stopper which is set at the both ends of magazine (sleeve) is made of rubber.
All tolerances are ±0.4mm unless otherwise specified.

名称 NAME	SOP32SPK-A2	備考 NOTE
DRAWING NO.	CV654	
単位 UNIT	mm	

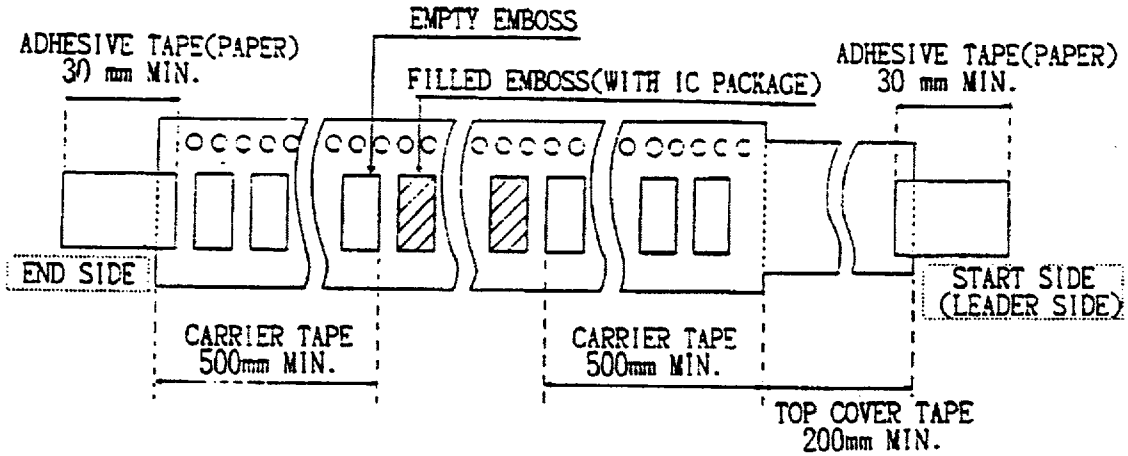
SHARP

EMBOSS TAPING TYPE (E2)

IC TAPING DIRECTION

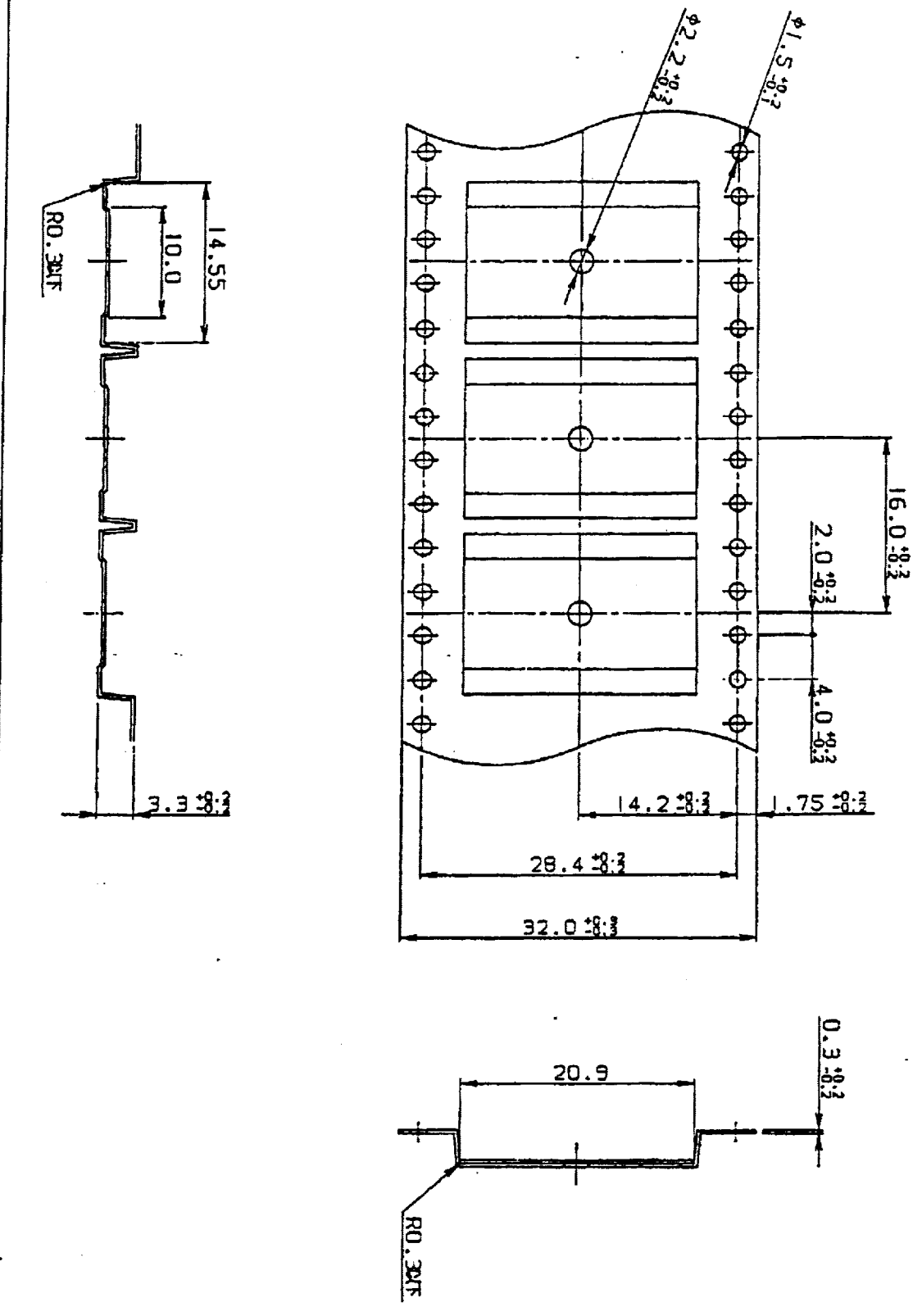


LEADER SIDE AND END SIDE OF TAPE



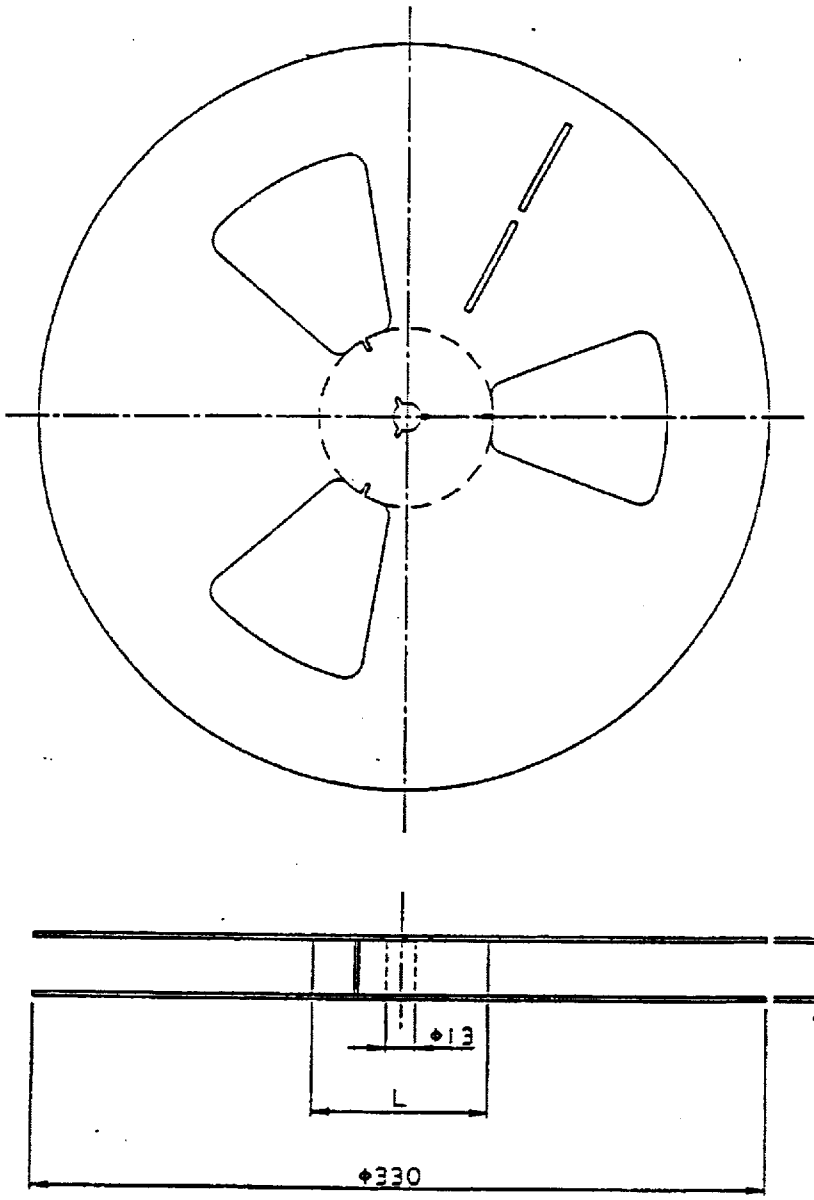
名称 NAME	EMBOSS TAPING TYPE (E2)			備考 NOTE
DRAWING NO.	CV522	単位 UNIT	mm.	

SHARP



名称 NAME	EC32SPTS-16			備考 NOTE
DRAWING NO.	CV584	単位 UNIT	mm	

SHARP



PKG	W (mm)	L (mm)	REEL NUMBER
SOP14-P-225	16.4	φ80	ECR16
SOP16-P-225	〃	〃	〃
SOP24-P-450	24.4	〃	ECR24
SOP28-P-450	〃	〃	〃
SOP32-P-525	32.4	φ100	ECR32
SOP44-P-600	44.8	φ100	ECR44-H

名称 NAME	REEL FOR EMBOSS CARRIER TAPING			備考 NOTE
DRAWING NO.	CV521	単位 UNIT	mm	