AMD

AMD-766™

Peripheral Bus Controller

Revision Guide

Publication # **23615** Rev: **C**
Issue Date: **June 2001**

Revision History

Date	Rev	Description
April 2001	B	Initial public release.
June 2001	C	Added errata #22.

AMD-766™ Peripheral Bus Controller Revision Guide

The purpose of the *AMD-766™ Peripheral Bus Controller Revision Guide* is to communicate updated product information on the AMD-766™ peripheral bus controller to designers of computer systems and software developers. This guide consists of four major sections:

- **Product Marking Identification:** This section, which starts on page 3, provides product types, product revisions, OPNs (Ordering Part Numbers), and product marking information.
- **Product Errata:** This section, which starts on page 4, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification. A product errata may cause the behavior of the AMD-766 peripheral bus controller to deviate from the published specifications.
- **Revision Determination:** This section starts on page 26.
- **Technical and Documentation Support:** This section, which starts on page 27, provides a listing of available technical support resources. It also lists corrections, modifications, and clarifications to listed documents.

Revision Guide Policy

Occasionally, AMD identifies deviations from or changes to the specification of the AMD-766 peripheral bus controller. These changes are documented in the *AMD-766™ Peripheral Bus Controller Revision Guide* as errata. Descriptions are written to assist system and software designers in using the AMD-766 and corrections to AMD's documentation on the AMD-766 peripheral bus controller are included. This revision guide documents currently characterized product errata, but is not intended to document all errata that may be found in the controller.

1 Product Marking Identification

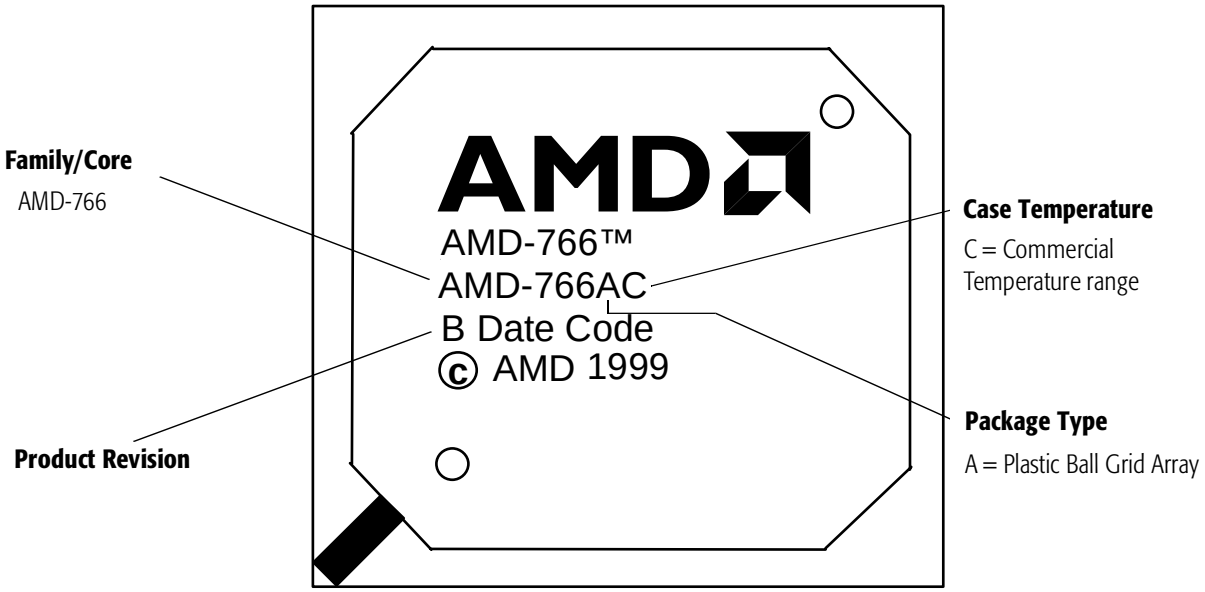

Table 1. Valid Ordering Part Number Combinations

OPN	Package Type	Operating Voltage	Case Temperature (max.)
AMD-766AC	272-pin PBGA	3.0V-3.6V	85° C

Notes:

Valid combinations are configurations that are or will be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

2 Product Errata

This section documents AMD-766 peripheral bus controller product errata. The errata are divided into categories to assist referencing particular errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2 cross-references the revisions of the controller to each erratum. An "X" indicates that the erratum applies to the stepping. The absence of an "X" indicates that the erratum does not apply to the stepping. Shading within the table indicates an addition or modification from the previous release of this document.

Note: *There can be missing errata numbers. Errata that have been resolved from early revisions of the controller have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 2. Cross-Reference of Product Revision to Errata

Erratum Number and Description	Revision Number			
	A0	A1	A2	B0
1 Sleep Button and Power Button are not Debounced Correctly	X	X	X	
2 IDE IOR Phy Select	X	X	X	
3 IDE ATA-100 Specified Data Hold Time not Met	X	X	X	
4 VDD_RTC Draws Excessive Current	X	X		
5 DMA Page Table not Updated for LPC Bus	X	X	X	
6 DMA Terminal Count Status Register is Set Too Early	X	X	X	
7 BIOS Write Lock Error	X	X	X	
8 PCI Bus Parking While a Cycle is Taking Place	X	X	X	X
9 Target-Driven PCI Data Bus After PCI Turnaround Cycle	X	X	X	X
10 PCI Special Cycles Being Delayed	X	X	X	X
11 Programmable Interval Timer does not Support Unspecified Modes	X	X	X	X
12 Programmable Interval Timer does not Support Mode 1 and Mode 5	X	X	X	X
13 Programmable Interval Timer does not Accept Back-to-Back Writes to the Initial Count Register	X	X	X	X
14 Programmable Interval Timer2 does not Load Correct Value into the Initial Count Register	X	X	X	X
15 IDE Read / Write Prefetch Hangs PCI Bus	X	X	X	X
17 EIDE Controller Bus Master Base Address Register is 256-Byte Aligned	X	X	X	X
18 USB OHCI Register Specification Differences	X	X	X	X
19 UDMA-100 Performance Does not Meet Industry-Standard Benchmarks	X	X	X	X
20 USB HccaDoneHead WriteBack Bug	X	X	X	X
21 WHQL SSID, SSVID Non-Conformance	X	X	X	X
22 Multiprocessor System May Hang While in FULL APIC Mode and IOAPIC Interrupt is Masked				X

1 Sleep Button and Power Button are not Debounced Correctly

Products Affected. A0, A1, A2

Normal Specified Operation. Whenever the sleep or power button are depressed the corresponding status PM00, bit[SLPBTN_STS] or PM00, bit[PWRBTN_STS] should be set.

Non-conformance.The first sleep button event from a system reset sets PM00, bit[SLPBTN_STS]. After this bit is cleared by software, the next sleep button event does not set this bit. The PM00, [PWRBTN_STS] bit behaves in the same fashion.

Potential Effect on System. System will not go to sleep more than once when using sleep button.

Suggested Workaround. Reset the system to allow PM00 [SLPBTN_STS] and PM00 [PWRBTN_STS] to be set.

Resolution Status. Fix planned in B0.

2 IDE IOR Phy Select

Products Affected. A0, A1, A2

Normal Specified Operation. The IDE IO cell should be connected to the 3-bit Phy select signals so that IDE data hold times are selectable.

Non-conformance. The IDE IO cell was tied to ground instead of the 3-bit Phy select signal. This selects the slowest mode and causes probems for UDMA operations which require fast mode. In A1 stepping a partial fix was implemented to tie the three-bit Phy select signal to fast mode.

Potential Effect on System. UDMA modes will not operate.

Suggested Workaround. Use A1 stepping.

Resolution Status. Fix planned for B0.

3 IDE ATA-100 Specified Data Hold Time not Met

Products Affected. A0, A1, A2

Normal Specified Operation. ATA-100 Rev0.6, specifies Ultra DMA data hold time, T_{DVHIC}, at 9ns.

Non-conformance. The hold time requirement on data from strobe for UDMA modes 0-4 was increased from 6ns to 9ns in ATA-100 Rev0.6 specification. AMD-766 peripheral bus controller uses CLK100 cycle for all these modes which is inadequate to meet the 9ns hold time requirement.

Potential Effect on System. None detected.

Suggested Workaround. None.

Resolution Status. Fix planned for B0.

4 VDD_RTC Draws Excessive Current

Products Affected. A0, A1

Normal Specified Operation. In MOFF state the RTC circuit should consume approximately 2 micro-Amps of current.

Non-conformance. AMD-766 peripheral bus controller consumes 2 mA of current in MOFF state which is 1000 times more than the specified current.

Potential Effect on System. 3.3VDC motherboard batteries will discharge below operating voltage. This will result in CMOS settings not being saved.

Suggested Workaround. None.

Resolution Status. Fix planned for A2.

5 DMA Page Table not Updated for LPC Bus

Products Affected. A0, A1, A2

Normal Specified Operation. DMA page table entries need to be updated when switching between DMA devices on LPC bus.

Non-conformance. When a DMA channel change occurs the previous DMA page table is used. Once a first DMA transfer is completed after reset, the internal DMA page table pointer gets stuck pointing to the initial entry.

Potential Effect on System. Cannot use two DMA devices back to back.

Suggested Workaround. None.

Resolution Status. Fix planned for B0.

6 DMA Terminal Count Status Register is Set Too Early

Products Affected. A0, A1, A2

Normal Specified Operation. The "terminal count reached" status bit should be set only when the terminal count condition is reached.

Non-conformance. Terminal count status bit for each channel gets set one transfer count early.

Potential Effect on System. None.

Suggested Workaround. None.

Resolution Status. Fix planned for B0.

7 BIOS Write Lock Error

Products Affected. A0, A1, A2

Normal Specified Operation. When Function 0, offset 48 bit [RWR] is set to zero, writes to BIOS space should not be allowed.

Non-conformance. When Function 0, offset 48 bit [RWR] is set to zero, writes to BIOS space should not be allowed. However, range FFBE_FFFF:FFB0_0000 at the bottom of the 5MB BIOS space is not covered by this bit. Also this range is not covered by any of the OAR locking registers thus this region is always accesible when read.

Potential Effect on System. Possible BIOS security hole.

Suggested Workaround. None.

Resolution Status. Fix planned for B0.

8 PCI Bus Parking While a Cycle is Taking Place

Products Affected. A0, A1, A2, B0

Normal Specified Operation. The AMD-766 peripheral bus controller must not drive PCI C/BE# lines while entering PCI bus park mode.

Non-conformance. If the Northbridge parks the PCI bus on the AMD-766 peripheral bus controller while the Northbridge is executing a PCI cycle, the AMD-766 will drive the C/BE# lines for one PCI clock.

Potential Effect on System. None. The AMD Northbridge should always park on itself (default).

Suggested Workaround. None.

Resolution Status. No fix planned.

9 Target-Driven PCI Data Bus After PCI Turnaround Cycle

Products Affected. A0, A1, A2, B0

Normal Specified Operation. The target of a PCI read cycle drives the PCI data bus after the turnaround cycle has completed. This is to limit the amount of time that the PCI address and data bus floats.

Non-conformance. When the AMD-766 peripheral bus controller is a target for a PCI read cycle, the AMD-766 does not drive the PCI data bus until it is ready to supply the data.

Potential Effect on System. None.

Suggested Workaround. None.

Resolution Status. No fix planned.

10 PCI Special Cycles Being Delayed

Products Affected. A0, A1, A2, B0

Normal Specified Operation. Whenever a PCI special cycle is directed to the AMD-766 peripheral bus controller, the data phase can be delayed by 16 PCI clocks after assertion of FRAME# control signal.

Non-conformance. When a PCI special cycle is directed to the AMD-766 peripheral bus controller the data phase must be valid by the third PCI clock after the assertion of FRAME# control signal. If the PCI data is delayed longer than three PCI clocks past assertion of FRAME#, the AMD-766 peripheral bus controller will respond improperly.

Potential Effect on System. None. The AMD-761™ system controller (Northbridge) always presents valid data for PCI special cycle two PCI clocks after assertion of FRAME#.

Suggested Workaround. None.

Resolution Status. No fix planned.

11 Programmable Interval Timer does not Support Unspecified Modes

Products Affected. A0, A1, A2, B0

Normal Specified Operation. The Programmable Interval Timer (P.I.T.) in the AMD-766 controller only accepts specified modes of 0 through 5 as documented in industry-standard 82C54 documentation.

Non-conformance. Some commercially available diagnostic programs such as WinCheckit98 may improperly program the timer for unspecified modes 6 or 7. Other existing Southbridge devices tolerate these unspecified modes and default to a known mode of operation.

Potential Effect on System. If the AMD-766 controller P.I.T. is programmed to an unspecified mode such as mode 6 or mode 7 the system will hang.

Suggested Workaround. Do not program the AMD-766 controller P.I.T. to unspecified modes.

Resolution Status. No fix planned.

12 Programmable Interval Timer does not Support Mode 1 and Mode 5

Products Affected. A0, A1, A2, B0

Normal Specified Operation. The Programmable Interval Timer (P.I.T.) in the AMD-766 controller should accept specified modes of 0 through 5 as documented in industry-standard 82C54 documentation.

Non-conformance. The AMD-766 controller P.I.T. was designed not to support the specified external GATE0, GATE1, and GATE2 signals. This lack of external access makes P.I.T. modes 1 and 5 unusable.

Potential Effect on System. None.

Suggested Workaround. Do not program the AMD-766 controller P.I.T. to mode 1 or mode 5.

Resolution Status. No fix planned.

13 Programmable Interval Timer does not Accept Back-to-Back Writes to the Initial Count Register

Products Affected. A0, A1, A2, B0

Normal Specified Operation. The Programmable Interval Timer (P.I.T.) in the AMD-766 controller should latch all writes to the initial count register CR for mode 2 as documented in industry-standard 82C54 documentation.

Non-conformance. The AMD-766 controller P.I.T. initial count register does not correctly latch a new initial count value before the previously loaded terminal count has been reached. If only the initial count register CR is written this new value will not be latched.

Potential Effect on System. None.

Suggested Workaround. Write a complete control word to the control word register located at PORT 43h. Then write a new initial count value "CR" for the selected counter to PORT 40h or PORT 41h or PORT 42h. This process will cause the counters to be loaded immediately with correct count values..

Resolution Status. No fix planned.

14 Programmable Interval Timer2 does not Load Correct Value into the Initial Count Register

Products Affected. A0, A1, A2, B0

Normal Specified Operation. The Programmable Interval Timer (P.I.T.) in the AMD-766 controller should latch all writes to the initial count register for mode 0 as documented in industry-standard 82C54 documentation.

Non-conformance. The AMD-766 controller P.I.T. TIMER2 initial count register does not correctly latch a new initial count value when the following sequence is used:

Step 1 Disable TIMER2 by writing to PORT61[TMR2EN].

Step 2 Program TIMER2 into mode 0 and as 16-bit binary count.

Step 3 Program the initial count register CR as 0100h.

Step 4 Re-enable TIMER2 by writing to PORT61[TMR2EN].

The AMD-766 P.I.T. counter will only latch the lower 8 bits of the initial count value. For example if CR is loaded with count 0100h then the value of FF00h is loaded into initial count register CR. This errata only exists in TIMER2.

Potential Effect on System. None.

Suggested Workaround. None.

Resolution Status. No fix planned.

15 IDE Read / Write Prefetch Hangs PCI Bus

Products Affected. A0, A1, A2, B0

Normal Specified Operation. When IDE Read / Write prefetch is enabled and the IDE transfer mode is PIO the AMD-766 IDE controller should transfer IDE data to the PCI bus.

Non-conformance. If an IDE transfer in UDMA mode occurs before a PIO Prefetch transfer, the PIO transfer mode disk drive data will not be transferred from the IDE bus to the PCI bus.

Potential Effect on System. The AMD-766 IDE controller causes PCI bus retry cycles to occur forever. The system may hang or not boot to the operating system.

Suggested Workaround. Do not enable IDE Read / Write Prefetch in BIOS setup. The Current BIOS setup default for IDE Read / Write Prefetch is disabled.

Resolution Status. No fix planned.

17 EIDE Controller Bus Master Base Address Register is 256-Byte Aligned

Products Affected. A0, A1, A2, B0

Normal Specified Operation. The IDE controller function in the AMD-766 peripheral bus controller contains a PCI configuration space offset at C1A20 "EIDE Controller Bus Master Control Registers Base Address." These bits specify a 16-byte I/O address that maps to an EIDE register set (IBMx) that is compliant with the SFF 8038I rev 1.0 specification "Bus Master Programming Interface for IDE ATA Controllers."

Non-conformance. The IDE controller function in the AMD-766 peripheral bus controller has implemented a 256-byte I/O address alignment instead of the 16-byte I/O address alignment.

Potential Effect on System. None. All known software supports 16-byte and 256-byte I/O address boundaries.

Suggested Workaround. None.

Resolution Status. No fix planned.

18 USB OHCI Register Specification Differences

Products Affected. A0, A1, A2, B0

Normal Specified Operation. The USB function in the AMD-766 peripheral bus controller was designed according to the Open Host Controller Interface Specification for USB (Open HCI), Release 1.0a.

The Open HCI specifies the following internal registers :

HcDoneHead is specified as read-only.
HcFmNumber is specified as read-only.
HFmInterval bit 30 is specified in this register as part of the FSMPS field.
HceStatus the CmdData bit is specified as read/write.
HceControl the GateA20Sequence bit is specified as read/write.

Non-conformance. The USB function in the AMD-766 peripheral bus controller has implemented the above USB registers as follows:

HcDoneHead is implemented as read/write.
HcFmNumber is implemented as read/write.
HFmInterval bit 30 is not implemented, always returns zero.
HceStatus the CmdData bit is implemented as read-only.
HceControl the GateA20Sequence bit is implemented as read-only.

Potential Effect on System. None.

Suggested Workaround. None.

Resolution Status. No fix planned.

19 UDMA-100 Performance Does not Meet Industry-Standard Benchmarks

Products Affected. A0, A1, A2, B0

Normal Specified Operation. When the IDE controller is programmed for UDMA-100 mode, the expected data transfer rate is 100 Mbytes per second (MBPS).

Non-conformance. If the IDE controller is programmed for UDMA-100 mode, the observed data transfer rate is on the order of 78 MBPS.

Potential Effect on System. No functional failures occur. This errata only affects IDE UDMA-100 performance.

Suggested Workaround. None.

Resolution Status. No fix planned.

20 USB HccaDoneHead WriteBack Bug

Products Affected. A0, A1, A2, B0

Normal Specified Operation. At each start of frame a write to the HCCA memory space is initiated to update the frame number. If a TD was retired the DoneHead pointer is also written to HCCA. Once the DoneHead is written back, no writebacks to the DoneHead in HCCA are allowed until the DoneHead interrupt status bit is cleared.

Non-conformance. The issue arises when an SOF writeback is pending and the DoneHead interrupt status is cleared with additional TD retired requiring another DoneHead writeback. The list processor updates its current writeback request transfer size to include the next DoneHead pointer, but the bus master only accepts the size of the original request. The result is the list processor thinks the DoneHead was written back and clears the pointer, but the bus master did not complete the transfer and the pointer is lost. Microsoft is aware of the problem and is evaluating a software patch to the driver.

Potential Effect on System. None have been observed. In the worst case, a transfer does not fully complete if the above criteria occurs. The above criteria must occur within a one-PCLK window for this to be observed.

Suggested Workaround. None. Most commercially available OHCI USB controller products do not implement this fix. No observations have ever occurred in validation testing or USB plugfests.

Resolution Status. No fix planned.

21 WHQL SSID, SSVID Non-Conformance

Products Affected. A0, A1, A2, B0

Normal Specified Operation. Subsystem registers in the PCI header are located at offset 2Ch–2Dh (subsystem vendor ID—SSVID), and 2Eh–2Fh (subsystem ID—SSID). PC99 requires that these registers exist for all non-bridge function spaces. These registers are required to be read-only.

Non-conformance. The AMD-766 peripheral bus controller did not implement these registers for the non-bridge function spaces within the device (i.e. the IDE, USB, and System Management function spaces).

Potential Effect on System. Fails WHQL testing. No other system effects.

Suggested Workaround. None needed. Most commercially available Southbridge products do not implement these registers.

Resolution Status. No fix planned.

22 Multiprocessor System May Hang While in FULL APIC Mode and IOAPIC Interrupt is Masked

Products Affected. B0

Normal Specified Operation. The AMD-766 peripheral bus controller is designed to support FULL APIC mode in multiprocessor systems for system management events. If an interrupt is masked in the AMD-766 APIC controller then the corresponding interrupt message should not be sent to the processor via the 3- wire APIC bus.

Non-conformance. The AMD-766 peripheral bus controller will send a interrupt message via the 3-wire APIC bus regardless if the interrupt is masked or not.

Potential Effect on System. Since the processor had previously masked the APIC interrupt it is not expecting to receive future APIC messages for the masked interrupt. The APIC controller will continuously send the interrupt message via the 3-wire bus until a processor accepts the message, causing the system to hang.

A system hang has been observed when executing a server shutdown command in Novell Netware versions 5.0 or 5.1 while using a serial mouse. During the server shutdown sequence, software writes an invalid CPU ID to the IOAPIC redirection table and the system does not complete the shutdown.

Note: No failure has been observed when using a PS/2 mouse.

Suggested Workaround. None.

Resolution Status. No fix planned.

3 Revision Determination

Table 3 summarizes the AMD-766™ peripheral bus controller PCI revision ID register for function 0 at offset 8 to determine the version of silicon.

Table 3. AMD-766™ peripheral bus controller Revision IDs

Sequence	Revision	Function 0h Offset 8h
1	A0	01h
2	A1	01h
3	A2	01h
4	B0	02h
5	Reserved	03h
6	Reserved	04h

4 Technical and Documentation Support

4.1 Documentation Support

The following documents provide additional information regarding the operation of the AMD-766 peripheral bus controller:

- *AMD-761™ System Controller Data Sheet*, order# 24088
- *AMD-762™ System Controller Data Sheet*, order# 24416
- *AMD-766™ Peripheral Bus Controller Data Sheet*, order# 23167
- *AMD Athlon™ System Bus Specification*, order# 21902
- *AMD Athlon™ Processor BIOS, Software, and Debug Tools Developers Guide*, order# 21656
- *AMD Athlon™ Processor Model 4 Data Sheet*, order# 23792
- *AMD Athlon™ MP Processor Model 6 Data Sheet*, order# 24685

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