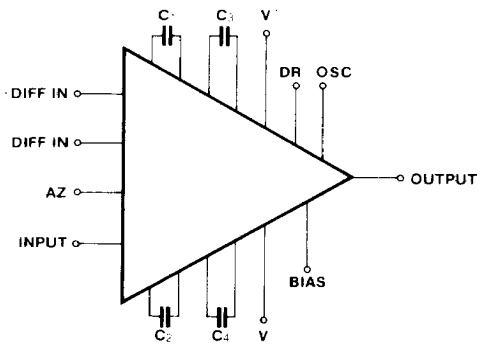
# AM-7605/AM-7606

## Commutating Auto-Zero (CAZ) Instrumentation Amplifier

### FEATURES

- **Exceptionally low input offset voltage — 2μV**
- **Low long term input offset voltage drift — 0.2μV/year**
- **Low input offset voltage temperature drift — 0.05μV/°C**
- **Wide common mode input voltage range — 0.3V above supply rail**
- **High common mode rejection ratio — 100 dB**
- **Excellent low supply voltage — Down to ±2V**
- **Short circuit protection on outputs for ±5V operation**
- **Static-protected inputs — no special handling required**




### GENERAL DESCRIPTION

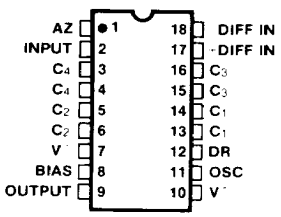
The AM-7605/AM-7606 commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace almost any of today's expensive hybrid or monolithic instrumentation amplifiers for low frequency applications from DC to 10 Hz. This is made possible by the unique construction of this new device, which takes an entirely new design approach to low frequency amplifiers.

Unlike conventional amplifier designs which employ three op amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key feature of the CAZ principle involves automatic compensation for long term drift phenomena and temperature effects.

The AM-7605/AM-7606 is a monolithic CMOS chip which consists of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section serves to insure that at all times the differential input source is being sensed and applied to the CAZ amp section. The CAZ instrumentation amp section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The AM-7605/AM-7606 is intended for low-frequency operation in applications such as strain gauges, which require voltage gains from 1 to 1000 and bandwidths from DC to 10 Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. The no-adjustment feature, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments temperature, humidity, toxicity, radiation, etc.: where equipment service is difficult.

### PIN CONFIGURATION




### ORDERING INFORMATION

| COMPENSATION | MODEL | OPER. TEMP. RANGE | PACKAGE |
|---|---|---|---|
| COMP. | AM-7605C | 0 to + 70°C | 18 pin Cerdip |
| | AM-7605R | −25 to + 85°C | |
| | AM-7605M | −55 to + 125°C | |
| UNCOMP. | AM-7606C | 0 to + 70°C | 18 pin Cerdip |
| | AM-7606R | −25 to + 85°C | |
| | AM-7606M | −55 to + 125°C | |

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 (TEL: (617) 339-9341 TWX 710-346-1953 TLX 951340

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (sum of both positive and negative supply voltages $V^+$ to $V^-$) ..... 18 Volts
Positive Supply Voltage (GND to $V^+$) ..... 18 Volts
Negative Supply Voltage (GND to $V^-$) ..... 18 Volts
DR Input Voltage ..... ($V^+$ +0.3) to ($V^+$ −8) Volts
Input Voltage ($C_1$, $C_2$, $C_3$, $C_4$, +DIFF IN, −DIFF IN, −INPUT, BIAS, OSC) (Note 2) ..... ($V^+$+0.3) to ($V^-$−0.3) Volts
Differential Input Voltage (+DIFF IN to −DIFF IN) (Note 3) ..... +($V^+$+0.3) to ($V^-$−0.3) Volts
Duration of Output Short Circuit (Note 4) ..... Unlimited
Continuous Total Power Dissipation (at or below 25°C free-air temperature) (Note 5) ..... 500 mW
Operating Temperature Range:
C ..... 0 to +70°C
R ..... −25°C to +85°C
M ..... −55°C to +125°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering 60 seconds) ..... 300°C

**Note 1** — Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent device failure. These are stress ratings only, and functional operation of devices under conditions other than those indicated in the Table of Electrical Characteristics is not recommended. Exposure to absolute maximum rating conditions for extended periods of time can cause device failures.

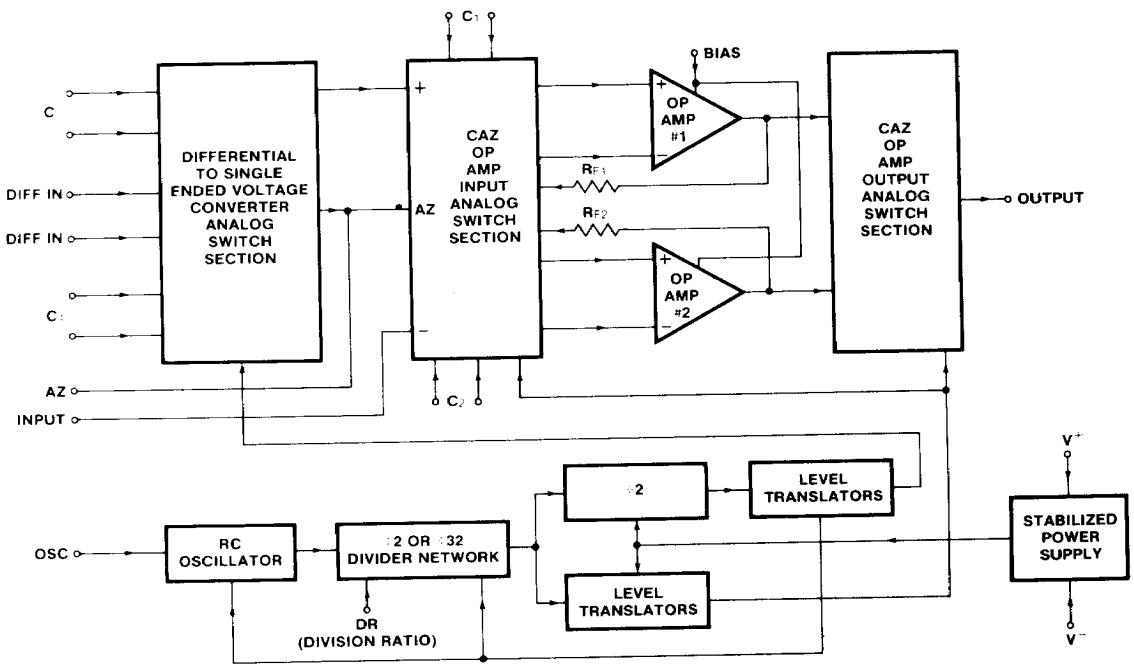
**Note 2** — An SCR structure is inherent in the CMOS process used in the fabrication of these devices. If voltages in excess of $V^+$+0.3 volts to $V^-$ 0.3 volts are connected to either inputs or outputs, destructive latchup can occur. For this reason it is recommended that no inputs from sources not on the same power supply or supplies be applied before the AM-7605/AM-7606 supplies are established, and that if multiple supplies are used the AM-7605/AM-7606 supplies be activated first.

**Note 3** — No restrictions are placed on the differential input voltages on either the +DIFF IN or −DIFF IN inputs so long as these voltages do not exceed the power supply voltages by more than 0.3V.

**Note 4** — The outputs may be shorted to ground (GND) or to either supply ($V^+$ or $V^-$). Temperatures and/or supply voltages must be limited to insure that the dissipation ratings are not exceeded.

**Note 5** — For operation above 25°C free-air temperature, derate 4mW/°C from 500 mW above 25°C.

## BLOCK DIAGRAM



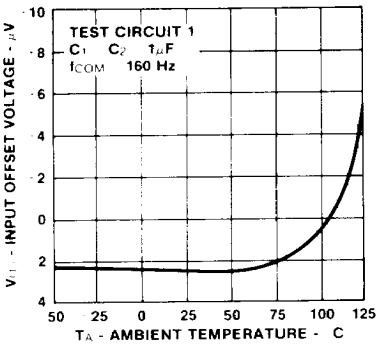
# AM-7605/AM-7606

## OPERATING CHARACTERISTICS

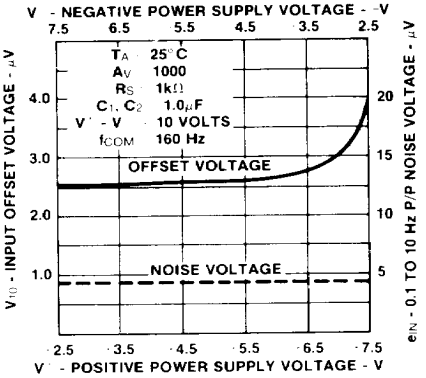
Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to $V^+$ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified.

| PARAMETER | SYMBOL | CONDITIONS | | VALUE MIN | VALUE TYP | VALUE MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | $R_S \leq 1k\Omega$ | Low Bias Setting | | ±2 | | μV |
| | | | Med Bias Setting | | ±2 | ±5 | μV |
| | | | High Bias Setting | | ±7 | | μV |
| | | MIL version over temp. | Med Bias Setting | | | ±20 | μV |
| Average Input Offset Voltage Temperature Coefficient | $TCV_{OS}$ | Low or Med Bias Settings | −55°C ≤ $T_A$ ≤ −25°C | | 0.01 | 0.1 | μV/°C |
| | | | −25°C ≤ $T_A$ ≤ +85°C | | 0.01 | 0.1 | μV/°C |
| | | | +25°C ≤ $T_A$ ≤ +125°C | | 0.05 | 0.15 | μV/°C |
| Long Term Input Offset Voltage Stability | $V_{OS\ Time}$ | Low or Med Bias Settings | | | 0.5 | | μV/Year |
| Common Mode Input Range | CMVR | | | 5.3 | | ±5.3 | V |
| Common Mode Rejection Ratio | CMRR | $C_{OSC}$ = 0, DR connected to $V^-$, $C_3$ = $C_4$ = 1μF | | | 94 | | dB |
| | | $C_{OSC}$ = 1μF, DR connected to GND, $C_3$ = $C_4$ = 1μF | | | 100 | | dB |
| | | $C_{OSC}$ = 1μF, DR connected to GND, $C_3$ = $C_4$ = 10μF | | | 104 | | dB |
| Power Supply Rejection Ratio | PSRR | | | | 110 | | dB |
| -INPUT Bias Current | $I_{NTB}$ | Any bias setting, $f_C$ = 160Hz (Includes charge injection currents | | | 0.15 | 1.5 | nA |
| Equivalent Input Noise Voltage peak-to-peak | $e_{np-p}$ | Band Width 0.1 to 10Hz | Low Bias Mode | | 4.0 | | μV |
| | | | Med Bias Mode | | 4.0 | | μV |
| | | | High Bias Mode | | 5.0 | | μV |
| Equivalent Input Noise Voltage | $e_{np-p}$ | Band Width 0.1 to 1.0Hz | All Bias Modes | | 1.7 | | μV |
| Voltage Gain | $A_V$ | $R_L$ = 100kΩ | Low Bias Setting | 90 | 105 | | dB |
| | | | Med Bias Setting | 90 | 105 | | dB |
| | | | High Bias Setting | 80 | 100 | | dB |
| Maximum Output Voltage Swing | $V_{OUT}$ | $R_L$ = 1MΩ | | | ±4.9 | | V |
| | | $R_L$ = 100kΩ | | | ±4.8 | | V |
| | | $R_L$ = 10kΩ | Positive Swing | +4.4 | | | V |
| | | | Negative Swing | | | −4.5 | V |
| Band Width of Input Voltage Translator | GBW | $C_3$ = $C_4$ = 1μF | All Bias Modes | | 10 | | Hz |
| Nominal Commutation Frequency | $f_{COM}$ | $C_{OSC}$ = 0pF | DR Connected to $V^-$ | | 160 | | Hz |
| | | | DR Connected to GND | | 2560 | | Hz |
| Nominal Input Converter Commutation Frequency | $f_{COM1}$ | $C_{OSC}$ = 0pF | DR Connected to $V^-$ | | 80 | | Hz |
| | | | DR Connected to GND | | 1280 | | Hz |
| Bias Voltage to define Current Modes | $V_{BA}$ | Low Bias Setting | | $V^-$ +0.3 | | $V^-$ +0.3 | V |
| | $V_{BM}$ | Med Bias Setting | | $V^-$ +1.4 | | $V^-$ +1.4 | V |
| | $V_{BL}$ | High Bias Setting | | $V^-$ +0.3 | | $V^-$ +0.3 | V |
| Bias (Pin 8) Input Current | $I_{BIAS}$ | | | | ±30 | | pA |
| Division Ratio Input Current | $I_{DR}$ | $V^-$ ≤ 8.0 ≤ $V_{DR}$ ≤ $V^+$ +0.3 volt | | | ±30 | | pA |
| DR Voltage to define Oscillator division ratio | $V_{DRH}$ | Internal oscillator division ratio 32 | | $V^-$ +0.3 | | $V^-$ +0.3 | V |
| | $V_{DRL}$ | Internal oscillator division ratio 2 | | $V^-$ +8 | | $V^-$ +1.4 | V |
| Effective Impedance of Voltage Translator Analog Switches | $R_{AS}$ | | | | 30 | | kΩ |
| Supply Current | $I_S$ | High Bias Setting | | 4 | 7 | 15 | mA |
| | | Med Bias Setting | | 0.6 | 1.7 | 5 | mA |
| | | Low Bias Setting | | 0.25 | 0.6 | 1.5 | mA |
| Operating Supply Voltage Range | $V^+$-$V^-$ | High Bias Setting | | 5 | | 10 | V |
| | | Med or Low Bias Setting | | 4 | | 10 | V |

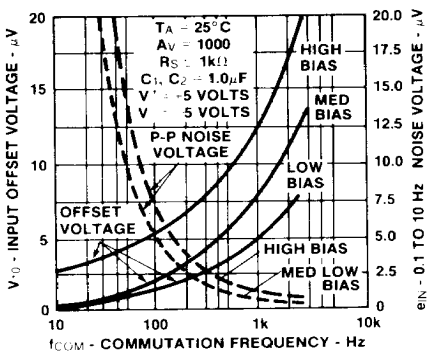
### INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



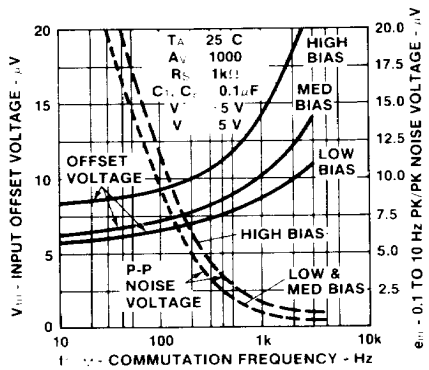

### INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



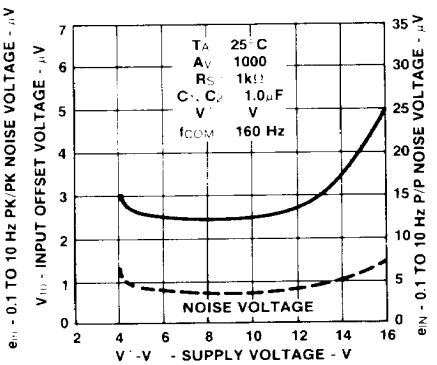

### INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY ($C_1$, $C_2$ = 1µF)



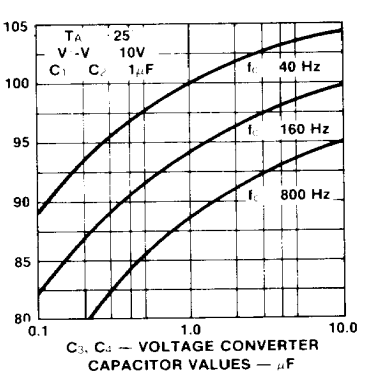

### INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY ($C_1$, $C_2$ = 0.1 µF)



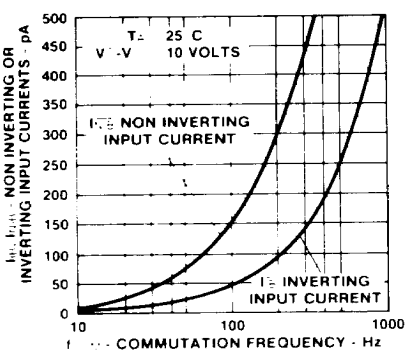

### INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V -V )



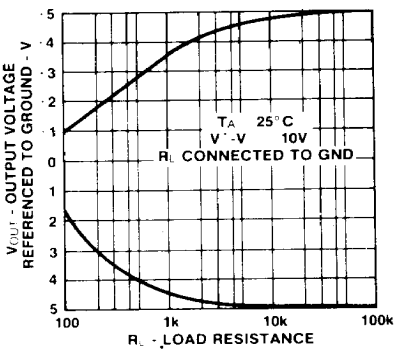

### COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER CAPACITORS



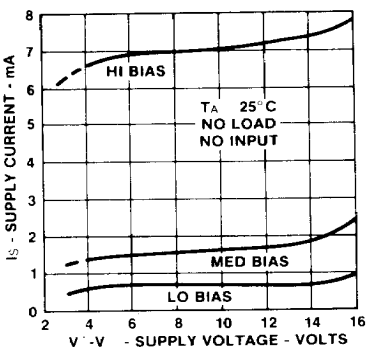

### INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



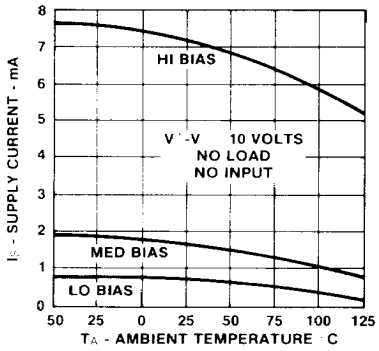

### MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



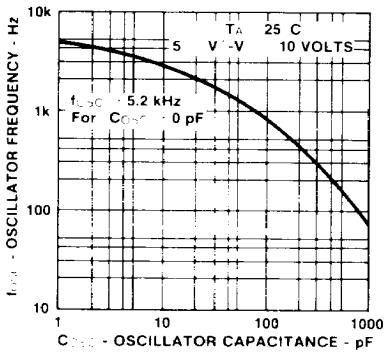

### SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



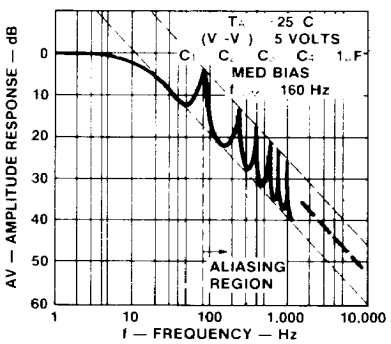
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



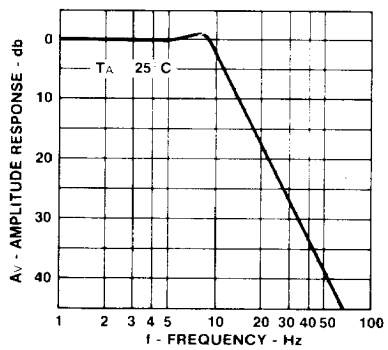

OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING

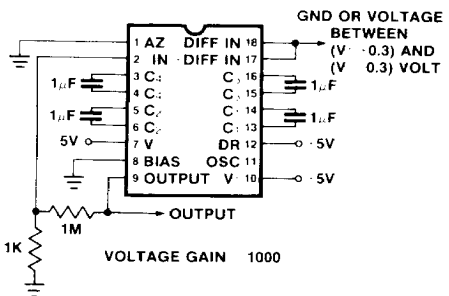



AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER




FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).




**TEST CIRCUIT 1:** USE TO MEASURE:

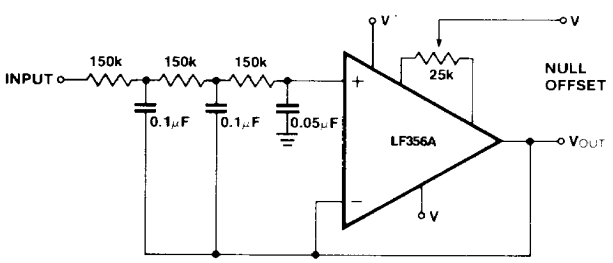
a) INPUT OFFSET VOLTAGE $\left(\frac{V_{OUT}}{1000}\right)$

b) INPUT EQUIV NOISE VOLTAGE

c) SUPPLY CURRENT

d) CMRR

e) PSRR




**TEST CIRCUIT 2:** DC to 10Hz (1Hz) Unity Gain Low Pass Filter

## DETAILED DESCRIPTION

### CAZ Instrumentation Amp Overview

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the AM-7605/AM-7606 CAZ instrumentation amp is the provision for self-compensation for internal error voltages, whether they are derived from steady-state conditions, temperature, supply voltage fluctuations, or are variable over a long term.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the AM-7605/AM-7606 is shown in Figure 1.

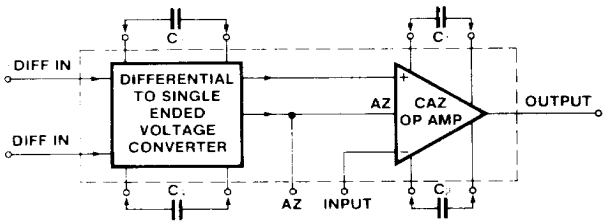



**Figure 1:** Simplified Block Diagram

The AM-7605/AM-7606 have approximately constant input equivalent noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the AM-7605/AM-7606 is its low-frequency operation (10 to 20 Hz maximum). However in many applications speed is not the most important parameter.

### CAZ Op Amp Section

Operation of the CAZ amp section of the AM-7605/AM-7606 instrumentation amplifier is best illustrated by referring to Figure 2. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp — the AZ, or auto-zero terminal. The voltage on the AZ input is that level to which each of the internal op amps are to be auto-zeroed. In Mode A, op amp #2 is connected into a unity gain mode through on-chip analog switches, and charges external capacitor $C_2$ to a voltage equal to the DC input offset voltage of the amplifier, in addition to the instantaneous low-frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor $C_2$ (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, and charges a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency ($f_{COM}$) so that at all times one or the other of the on-chip op amps is processing the input signal while the voltages on capacitors $C_1$ and $C_2$ are being updated regularly to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

* Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.
* Long-term offset voltage drift phenomena can be compensated and dramatically reduced.
* Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.
* Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and

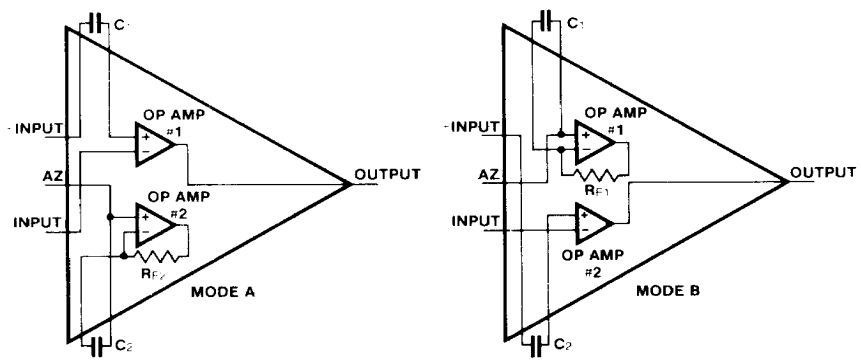



**Figure 2:** Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

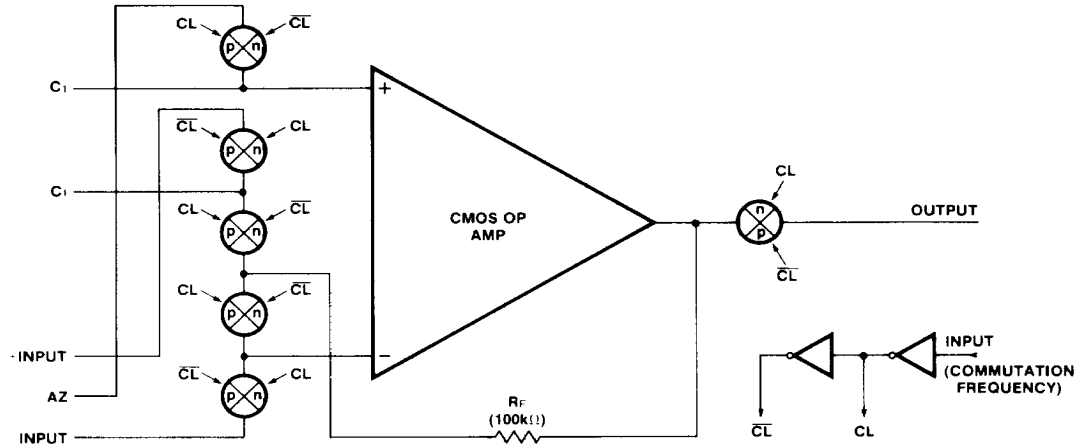


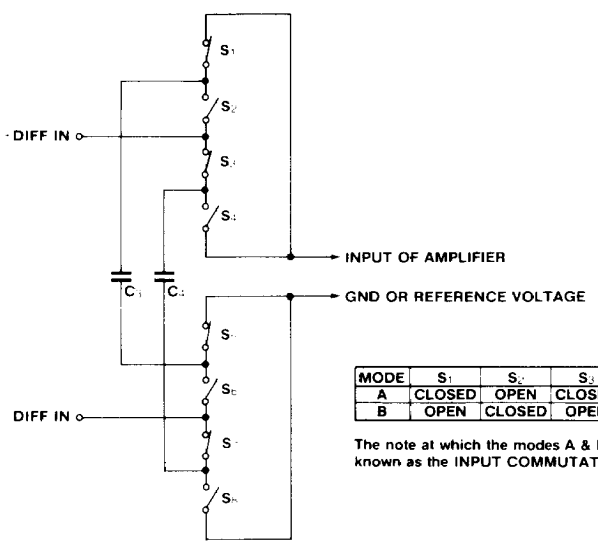

**Figure 3:** Schematic of analog switches connecting each internal OP AMP to the external inputs at the output.

the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. CMOS structure provides the CAZ amp concept with open-loop gains of greater than 100 dB, typical input offset voltages of ±5 mV, and ultra-low output leakage currents, typically 1 pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 3. Here, one op amp and its associated analog switches are required to connect each on-chip op amp so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

## DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

An idealized schematic of a voltage converter block is shown in Figure 4. The mode of operation is quite simple, involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input and the other from a ground or reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 5, where the voltage steps equal the differential voltage ($V_A$-$V_B$) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequency, commutation and noise voltages are added. Sampling theory states that to preserve the integrity of the information to be processed, at least two samples must be taken within a period (1/f) of the highest frequency of the signal being




| MODE | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ |
|---|---|---|---|---|---|---|---|---|
| A | CLOSED | OPEN | CLOSED | OPEN | CLOSED | OPEN | CLOSED | OPEN |
| B | OPEN | CLOSED | OPEN | CLOSED | OPEN | CLOSED | OPEN | CLOSED |

The note at which the modes A & B are cycled through is known as the INPUT COMMUTATION FREQUENCY

**Figure 4:** Schematic of the differential to single ended voltage converter

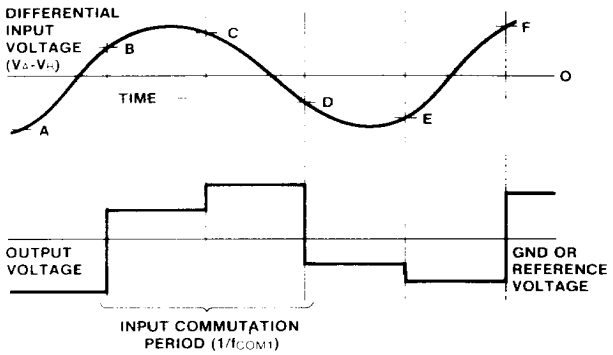



**Figure 5:** Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph on page 5.

sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is transferred to a lower frequency. This phenomenon is known as aliasing. Although the output responds above the commutation frequency, the frequencies of the output responses have been aliased down to frequencies below the commutation frequency.

The example shown in Figure 4 for the voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have finite ON impedances of 30kΩ, plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors $C_0$ and $C_O$ must be about 1μF to preserve signal translation accuracies to 0.01%. The 1μF capacitors, coupled with the 30kΩ equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is approximately 3 dB at 10 Hz.

## APPLICATIONS

### USING THE AM-7605/AM-7606 TO BUILD A DIGITAL READOUT TORQUE WRENCH

A typical application for the AM-7605/AM-7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ intrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting this voltage to a single-ended voltage reference to ground. The signal is then amplifier by the CAZ instrumentation amplifier and applied to the input of a 3-1/2 digit dual-slope A/D converter chip for LCD panel meter display. The A/D converter device used in this instance is the Intersil ICL7106.

In the digital readout torque wrench circuit, the internal reference voltage of the ICL7106 is used instead of the conventional external reference source. In order to set the full-scale reading, it is required that, given a certain strain gauge bridge with a defined pressure voltage sensitivity, a value of gain for the AM-7605/AM-7606 instrumentation CAZ amp be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Note that the common to V+ voltage of the CAZ amp is about 2.8V. This voltage must therefore be divided by about 10 to provide the 0.25V reference voltage. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2 mA.

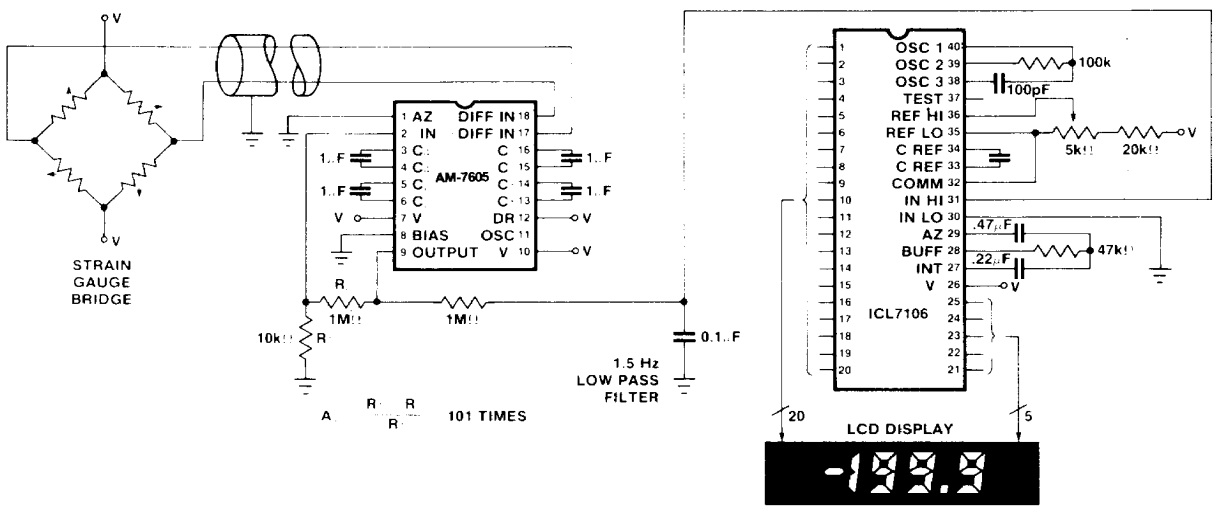



**Figure 6:** 3-1/2 Digit Digital Readout Torque Wrench

## SOME HELPFUL HINTS

### Testing the AM-7605/AM-7606 CAZ Instrumentation Amplifier

Test Circuits #1 and #2 provide convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5 Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be of a high-input impedance type — not a capacitor across the feedback resistor $R_2$ nor a low-impedance type of around 1kΩ — but rather must be rated at about 100kΩ and 1.0μF so that the output dynamic loading on the CAZ instrumentation amp is about 100kΩ.

### Bias Control

The on-chip op amps consume over 90% of the power required by the AM-7605/AM-7606 instrumentation op amp. For this reason, the internal op amps have externally-programmable bias levels. These levels are set by connecting the BIAS terminal to either $V^+$, GND, or $V^-$. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of power supply versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the lower the amplitude of commutation spikes) and offset errors due to "IR" voltage drops and thermoelectric temperature gradients across the chip and the higher the temperature gradients across the chip and the highe the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

### Output Loading (Resistive)

With a 10kΩ load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as 2kΩ.

However, with loads of less than 50kΩ, the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly 50kΩ each. Thus the open-loop gain is 20 dB less with a 2kΩ load than it would be with a 20kΩ load. Therefore, for high gain configurations requiring high accuracy, an output loading of 100kΩ or less is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked, and that is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

### Output Loading (Capacitive)

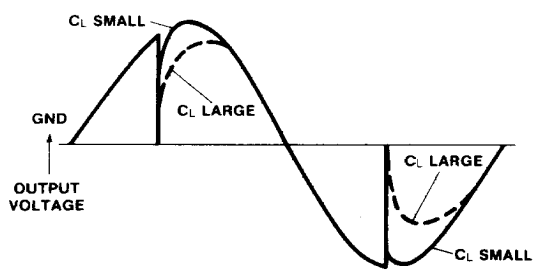
In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteristic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 7. It can be seen that the effect of a large load capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5 Hz filter will require a 100kΩ resistor and a 1.0μF capacitor, or a 1 MΩ resistor and an 0.1μF capacitor.

### Oscillator and Digital Circuitry Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open circuit. If the full divider network is used, this will result in a nominal commutation frequency of approximately 160 Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2 kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The AM-7605/AM-7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to $V^-$) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the $V^-$ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 8) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the $V^+$ supply (with respect to ground) is +5V (±10%) and the logic driver also operates from a similar voltage supply. The



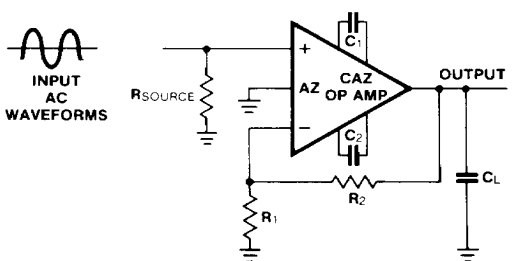




**Figure 7:** Effect of a load capacitor on output voltage waveforms.

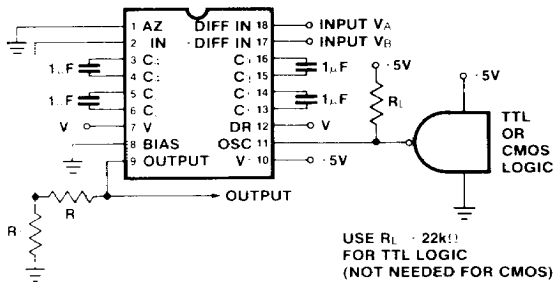



**Figure 8:** AM-7605 being clocked from external logic into the oscillator terminal.

reason for this requirement is that the logic section (including the oscillator) operates from an internal −5V supply, referenced to V⁻ support which is generated on-chip, and which is not accessible externally.

### Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects whereby electrical junctions consist of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. Special thermoelectric solder (70% cadmium, 30% tin) should be used. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep well away from equipment which dissipates heat.

### Component Selection

The two auto-zero capacitors ($C_1$ and $C_2$) should each be about 1.0μF value. These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them do not change significantly, problems of dielectric absorption, charge bleed-off and the like are not as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene and Mylar are the best.

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors is not critical. Even polarized electrolytic capacitors rated at 1.0μF and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

### Commutation Voltage Transient Effects

Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency pre-amplifiers limited to DC through 10 Hz. The is due to the finite switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest in-band frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors $C_1$ and $C_2$ must have values of at least 10,000 x 10 pF, or 0.1μF each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0 pA at an ambient temperature of 25° C.

The output waveform in Test Circuit #1 (with no input signal) is shown in Figure 9. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7 mV are not amplified by 1000.

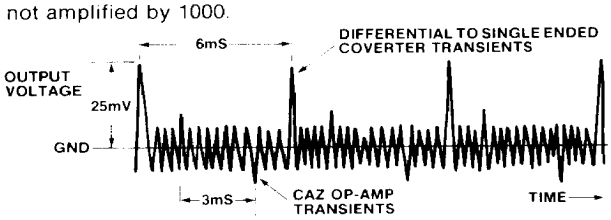



**Figure 9:** Output waveform from Test Circuit 1.

### Layout Considerations

Care should be exercised in positioning components on the PC board, particularly the capacitors $C_1$, $C_2$, $C_3$ and $C_4$, all of which must be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

## PACKAGE DIMENSIONS