REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25								
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
99-09-28

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 512K x 8-BIT, RADIATION-HARDENED, LOW VOLTAGE SRAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67264	5962-99607

SHEET 1 OF 25

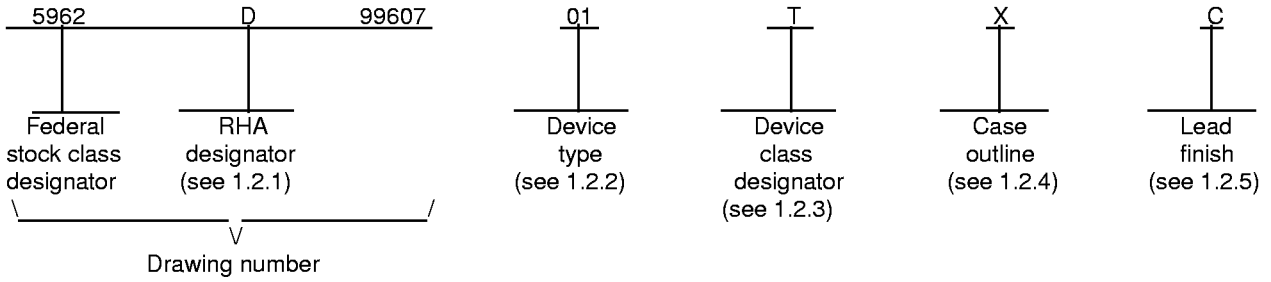
DSCC FORM 2233
APR 97

5962-E490-99

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V), and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class T, the user is encouraged to review the manufacturers Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	8Q512	512K X 8-bit rad-hard low voltage SRAM	25 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	36	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range, (V_{DD})	-0.5 V dc to +4.6 V dc
Voltage range on any input pin	-0.5 V dc to +4.6 V dc
Voltage range on any output pin	-0.5 V dc to +4.6 V dc
Input current, dc	± 10 mA
Power dissipation	1.0 W
Operating free-air temperature range, (T_A)	-55EC to +125EC
Storage temperature range, (T_{STG})	-65°C to +150EC
Junction temperature, (T_J)	+150EC
Thermal resistance, junction-to-case, (Θ_{JC}): Case U	+10EC/W

1.4 Recommended operating conditions.

Supply voltage range, (V_{DD})	+3.0 V dc to +3.6 V dc
Supply voltage, (V_{SS})	0 V dc
Input voltage, dc	0 V dc to V_{DD}
Operating free-air temperature, (T_A)	-55EC to +125EC

1.5 Radiation features

Maximum total dose available (dose rate = 3 rads(Si)/s)	≥ 24 x 10^3 rads(Si)
Dose rate upset	4/
Dose rate survivability	4/
Single event phenomenon (SEP) effective	
linear energy threshold (LET) with no upsets	≥ 90.5 MeV-cm^2/mg
with no latch-up	≥ 1.5 MeV-cm^2/mg
Neutron irradiation	4/

1.6 Digital logic testing for device classes T, Q, and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltage values in this drawing are with respect to V_{SS}.
4/ When a value is determined per customer requirements, it shall be provided.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535, and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be as specified on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation test circuit. The radiation test circuit shall be as specified on figure 6.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or aquiring activity upon request. For device classes Q, T and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or aquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan, including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturers QM plan.

For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's QM plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_A \le +125°C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
High-level input voltage	V_{IH}			1,2,3	All	2.0		V
			M,D	1 1/		2/		
Low-level input voltage	V_{IL}			1,2,3	All		0.8	V
			M,D	1 1/			2/	
High-level output voltage	V_{OH1}	I_{OH} = -4mA, V_{DD} = 3.0 V (TTL)		1,2,3	All	2.4		V
			M,D	1 1/		2/		
High-level output voltage	V_{OH2}	I_{OH} = -200µA, V_{DD} = 3.0 V (CMOS)		1,2,3	All	V_{DD} –0.10		V
			M,D	1 1/		2/		
Low-level output voltage	V_{OL1}	I_{OL} = 8 mA, V_{DD} = 3.0 V (TTL)		1,2,3	All		0.4	V
			M,D	1 1/			2/	
Low-level output voltage	V_{OL2}	I_{OL} = 200 µA, V_{DD} = 3.0 V (CMOS)		1,2,3	All		0.08	V
			M,D	1 1/			2/	
Input capacitance	C_{IN}	see 4.4.1e, f = 1 MHz at 0 V, T_A = 25°C 3/	V_{IN} = 25 mV	4	All		10	pF
Bidirectional I/O capacitance	$C_{I/O}$		$V_{I/O}$ = 25 mV	4	All		12	pF
Input current leakage	I_{IN}	$V_{SS} \le V_{IN} \le V_{DD}$		1,2,3	All	-2.0	+2.0	µA
			M,D	1 1/		2/	2/	
Three-state output current leakage	I_{OZ}	$0\ V \le V_O \le V_{DD}$, $V_{DD} = V_{DD}$ (max) $\overline{G} = V_{DD}$ (max)		1,2,3	All	-2.0	+2.0	µA
			M,D	1 1/		2/	2/	
Short-circuit output current 4/ 5/	I_{OS}	$0\ V \le V_O \le V_{DD}$		1,2,3	All	-90	+90	mA
			M,D	1 1/		2/	2/	
Operating supply current at 1MHz	I_{DD}	Inputs: V_{IL} = 0.8 V V_{IH} = 2.0 V, I_{OUT} = 0 mA V_{DD} = -0.5 V		1,2,3	All		125	mA
			M,D	1 1/			2/	
Operating supply current at 40MHz	I_{DD1}	Inputs: V_{IL} = 0.8 V V_{IH} = 2.0 V, I_{OUT} = 0 mA V_{DD} = -0.5 V		1,2,3	All		180	mA
			M,D	1 1/			2/	
Standby supply current at 0 MHz	I_{DD2}	$\overline{E1} = V_{DD} - 0.5\ V$, $V_{DD} = V_{DD}$(max)		1,3	All		6	mA
		$V_{IH} = V_{DD} - 0.5\ V$	M,D	1 1/			2/	
		Inputs: $V_{IL} = V_{SS}$ I_{OUT} = 0 mA		2			40	
			M,D	1 1/			2/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Test conditions $-55EC \le T_A \le +125EC$ $+3.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Functional test		See 4.4.1c $V_{IH} = V_{DD} -0.5\ V$	M,D	7,8A,8B 7 1/	All		2/	
Read cycle time 6/	t_{AVAV}	See figures 3 and 4.		9,10,11	All	25		ns
			M,D	9 1/		2/		
Read access time	t_{AVQV}			9,10,11	All		25	ns
			M,D	9 1/			2/	
Output hold time 7/	t_{AXQX}			9,10,11	All	3		ns
			M,D	9 1/		2/		
$\overline{G}$ -controlled output enable time 7/	t_{GLQX}			9,10,11	All	3		ns
			M,D	9 1/		2/		
$\overline{G}$ -controlled output enable time (read cycle 3)	t_{GLQV}			9,10,11	All		10	ns
			M,D	9 1/			2/	
$\overline{G}$ -controlled output three-state time 8/	t_{GHQZ}			9,10,11	All		10	ns
			M,D	9 1/			2/	
$\overline{E1}$ -controlled output enable time 7/ 9/	t_{ETQX}			9,10,11	All	3		ns
			M,D	9 1/		2/		
$\overline{E1}$ -controlled access time 9/	t_{ETQV}			9,10,11	All		25	ns
			M,D	9 1/			2/	
$\overline{E1}$ -controlled output three-state time 6/ 8/ 10/	t_{EFQZ}			9,10,11	All		10	ns
			M,D	9 1/			2/	
Write cycle time 11/	t_{AVAV}			9,10,11	All	25		ns
			M,D	9 1/		2/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Test conditions $-55°C \le T_A \le +125°C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Device enable to end of write	t_{ETWH}	See figures 3 and 4.		9,10,11	All	20		ns
			M,D	9 1/		2/		
Address setup time for write ($\overline{E1}$ -controlled)	t_{AVET}			9,10,11	All	0		ns
			M,D	9 1/		2/		
Address setup time for write ($\overline{W}$ - controlled)	t_{AVWL}			9,10,11	All	0		ns
			M,D	9 1/		2/		
Write pulse width	t_{WLWH}			9,10,11	All	20		ns
			M,D	9 1/		2/		
Address hold time for write ($\overline{W}$ - controlled)	t_{WHAX}			9,10,11	All	2		ns
			M,D	9 1/		2/		
Address hold time for device enable ($\overline{E1}$ -controlled)	t_{EFAX}			9,10,11	All	2		ns
			M,D	9 1/		2/		
$\overline{W}$ -controlled three-state time 8/	t_{WLQZ}			9,10,11	All		10	ns
			M,D	9 1/			2/	
$\overline{W}$ -controlled output enable time 7/	t_{WHQX}			9,10,11	All	5		ns
			M,D	9 1/		2/		
Device enable pulse width ($\overline{E1}$ -controlled)	t_{ETEF}			9,10,11	All	20		ns
			M,D	9 1/		2/		
Data setup time	t_{DVWH}			9,10,11	All	15		ns
			M,D	9 1/		2/		
Data hold time 7/	t_{WHDX}			9,10,11	All	2		ns
			M,D	9 1/		2/		
Device enable controlled write pulse width	t_{WLEF}			9,10,11	All	20		ns
			M,D	9 1/		2/		

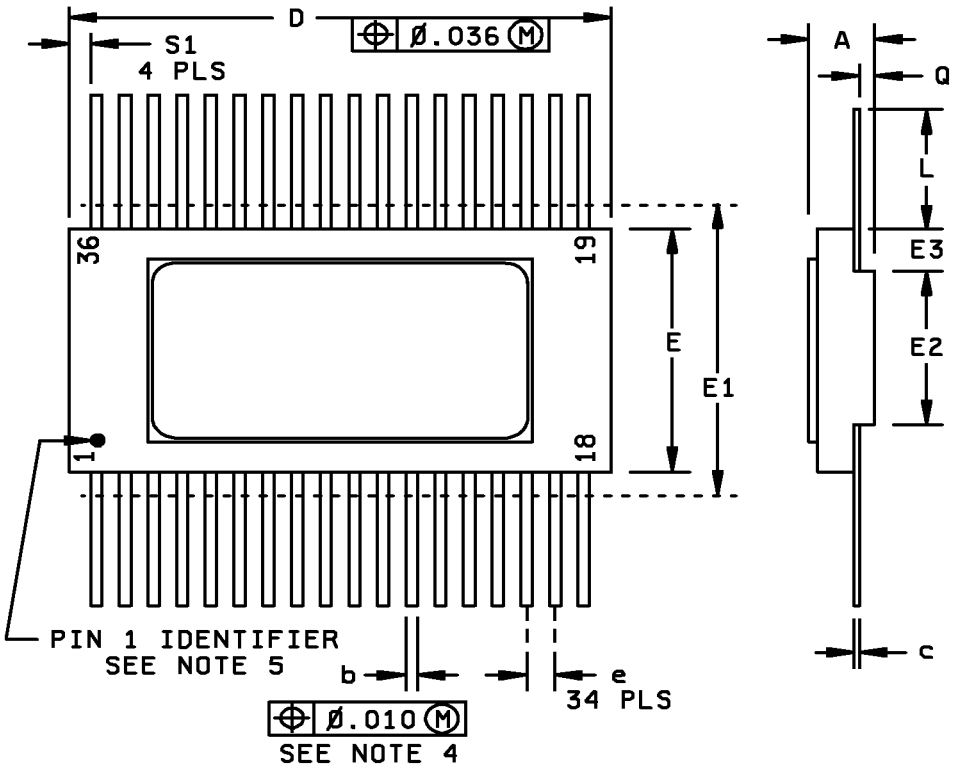
See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Test conditions $-55EC \le T_A \le +125EC$ $+3.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data setup time 7/	t_{DVEF}	See figures 3 and 4.	9,10,11	All	15		ns
		M,D	9 1/		2/		
Data hold time	t_{EFDX}		9,10,11	All	2		ns
		M,D	9 1/		2/		
Address valid to end of write	t_{AVWH}		9,10,11	All	20		ns
		M,D	9 1/		2/		
Write disable time 11/	t_{WHWL}		9,10,11	All	5		ns
		M,D	9 1/		2/		

1/ When performing postirradiation electrical measurements for any RHA level T_A = +25EC. Limits shown are guaranteed at T_A = +25EC " 5EC. The M and D in the test condition column are the postirradiation limits for the device types specified in the device types column.
2/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
3/ Measured only for initial qualification and after any design or process changes which may affect this parameter.
4/ Supplied as a design limit but not guaranteed or tested.
5/ Not more than one output may be shorted at a time for maximum duration of one second.
6/ This is a functional test.
7/ Three-state is defined as a 300 mV change from steady-state output voltage.
8/ Three-state is defined as a 1.1 V change from steady-state output low voltage and an 800 mV change from output high voltage.
9/ The ET (enable true) notation refers to the falling edge of $\overline{E1}$. SEU immunity does not affect the read parameters.
10/ The EF (enable false) notation refers to the rising edge of $\overline{E1}$. SEU immunity does not affect the read parameters.
11/ Functional test performed with outputs disabled ($\overline{G}$ high).

Case outline U



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.29	3.05	.090	.120
b	0.38	0.51	.015	.020
c	0.10	0.18	.004	.007
D		23.62		0.930
E	11.99	12.40	.472	.488
E1		12.65		.498
E2	8.89		.350	
E3	0.76		.030	
e	1.27 BSC		.050 BSC	
L	7.75	8.26	.305	.325
S1	0.13		.005	
Q	0.66	1.14	.026	.045

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. All exposed metalized areas are gold plated over electroplated nickel.
3. Package lid is electrically connected to V_{SS}.
4. Lead position and coplanarity are not measured.
5. Pin 1 identification area.

FIGURE 1. Case outline.

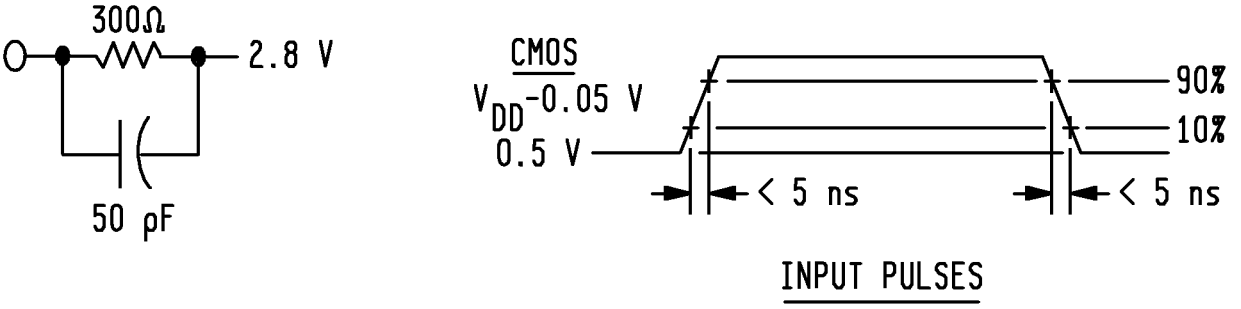
Device types	All
Case outlines	U
Terminal number	Terminal symbol
1	A0
2	A1
3	A2
4	A3
5	A4
6	$\overline{E1}$
7	DQ0
8	DQ1
9	V_{DD}
10	V_{SS}
11	DQ2
12	DQ3
13	$\overline{W}$
14	A5
15	A6
16	A7
17	A8
18	A9
19	NC
20	A10
21	A11
22	A12
23	A13
24	A14
25	DQ4
26	DQ5
27	V_{DD}
28	V_{SS}
29	DQ6
30	DQ7
31	$\overline{G}$
32	A15
33	A16
34	A17
35	A18
36	NC

FIGURE 2. Terminal connections.

$\overline{G}$	$\overline{W}$	$\overline{E1}$	I/O Mode	Mode
X 1/	X	1	3-state	Standby
X	0	0	Data-in	Write
1	1	0	3-state	Read 2/
0	1	0	Data out	Read

1/ X is defined as a “don’t care” condition.
2/ Device active; outputs disabled.

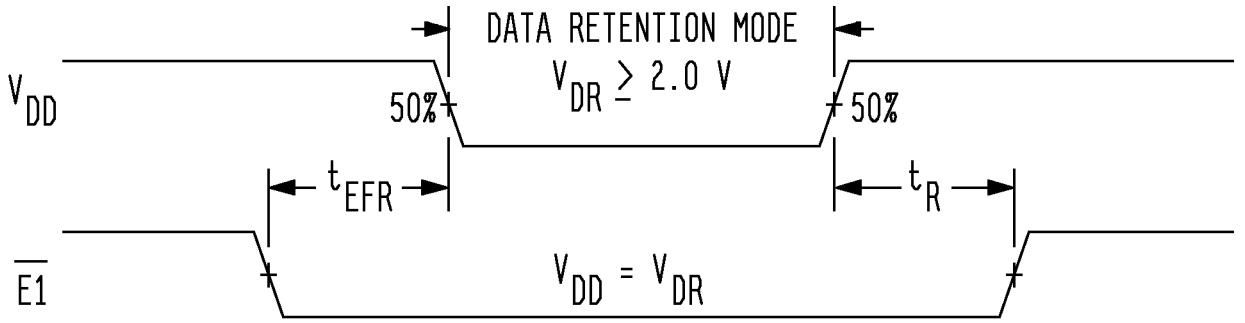
FIGURE 2. Truth table.



Notes: 1. 50 pF includes scope probe and test socket capacitance.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD}/2$).

FIGURE 3. Output load circuit and input waveforms.

Low V_{DD} data retention waveform.



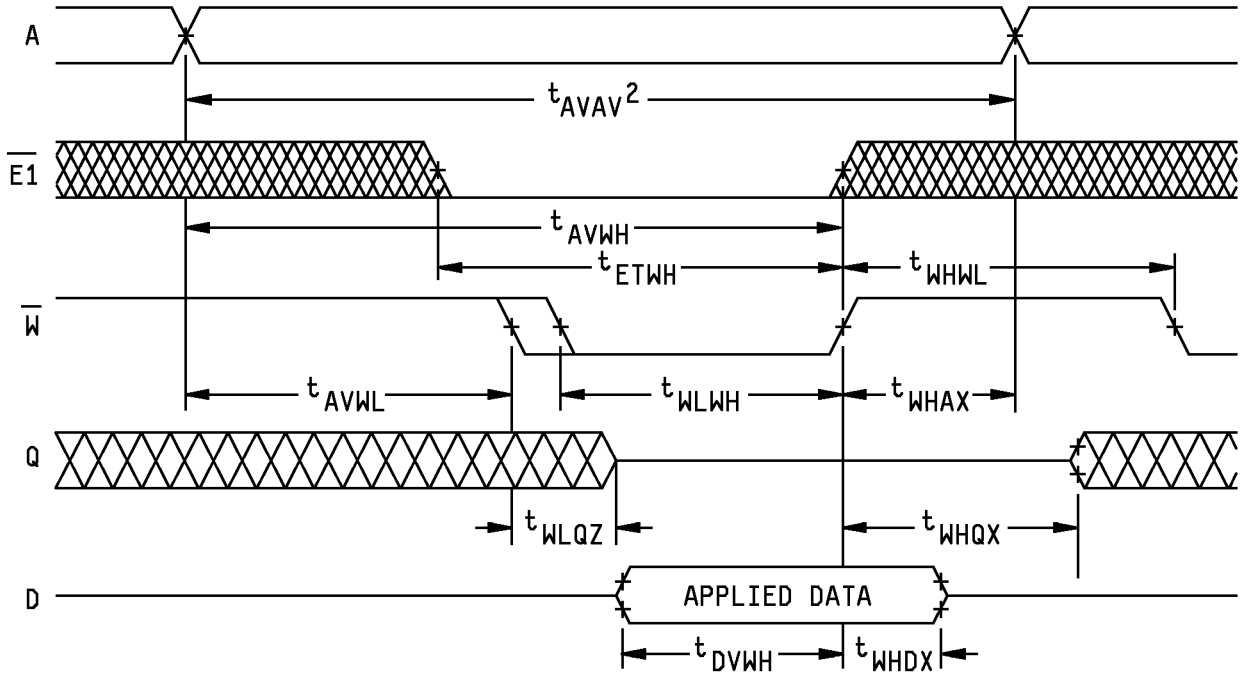
Data retention characteristics (pre-irradiation)
(T_C = 25°C, V_{DD} = 3.0 V, 1 second data retention pulse)

Symbol	Parameter	Minimum	Maximum	Unit
V_{DR}	V_{DD} for data retention	2.0	---	V
I_{DDR} 1/	Data retention current	---	1.0	mA
t_{EFR} 1/ 2/	Chip deselect to data retention time	0		ns
t_R 1/ 2/	Operation recovery time	t_{AVAV}		ns

1/ $\overline{E1}$ = V_{SS}, all other inputs = V_{DR} or V_{SS}.
2/ Not guaranteed or tested.

FIGURE 4. Timing waveforms.

Write cycle 1: write enable-controlled access.

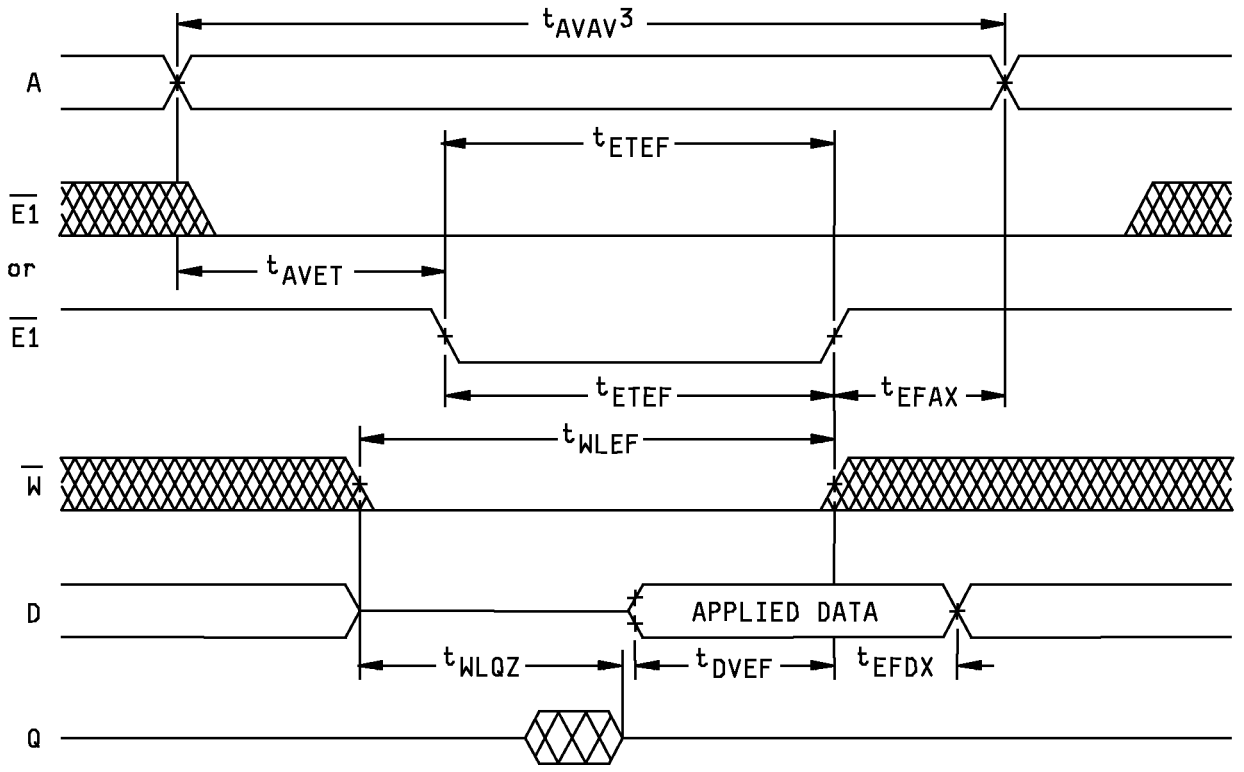


Notes: 1. $\overline{G} \leq V_{IL}$(max). If $\overline{G} \geq V_{IH}$ (min) then Q will be in three-state for the entire cycle.

2. $\overline{G}$ high for t_{AVAV} cycle.

FIGURE 4. Timing waveforms - continued.

Write cycle 2: chip enable-controlled access.



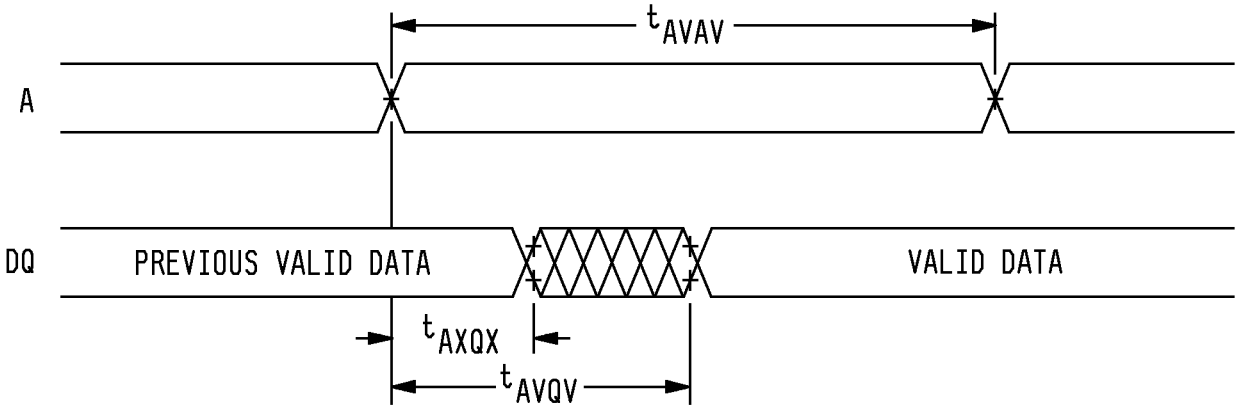
Notes: 1. $\overline{G} \leq V_{IL}$(max). If $\overline{G} \geq V_{IH}$ (min) then Q will be in three-state for the entire cycle.

2. Either $\overline{E1}$ scenario can occur.

3. $\overline{G}$ high for t_{AVAV} cycle.

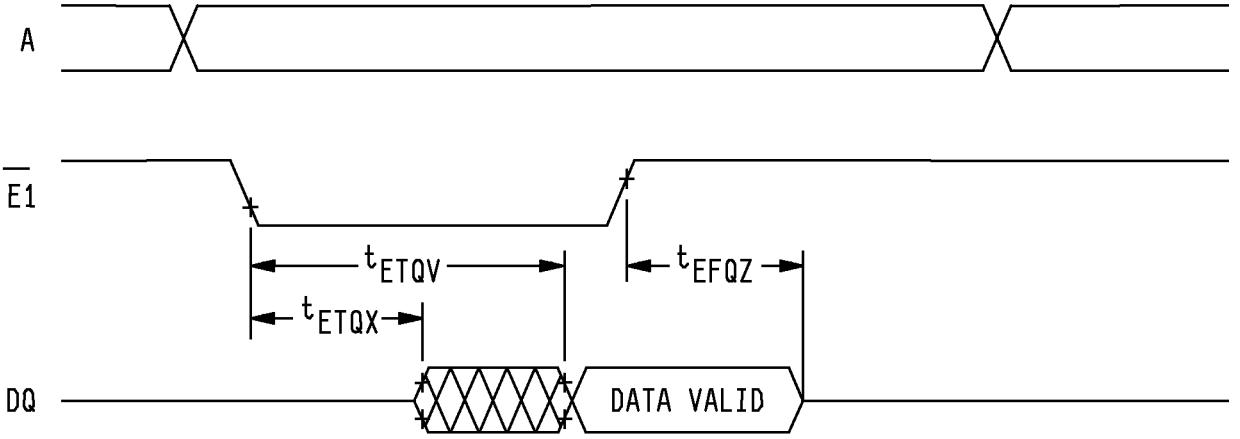
FIGURE 4. Timing waveforms - continued.

SRAM read cycle 1: address access.



Note: $\overline{E1}$ and $\overline{G} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

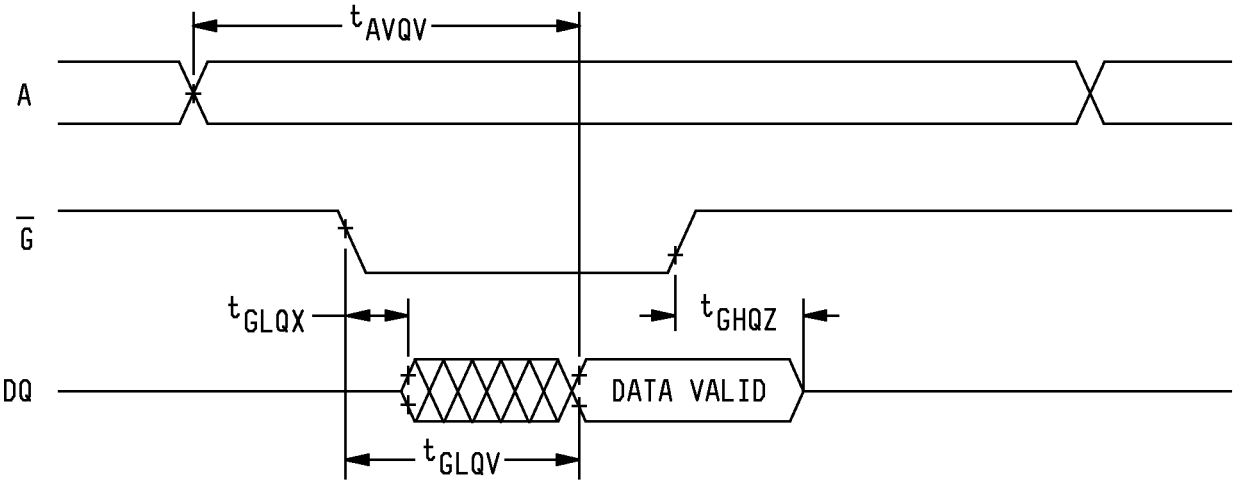
SRAM read cycle 2: chip enable-controlled access.



Note: $\overline{G} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

FIGURE 4. Timing waveforms - continued.

SRAM read cycle 3: output enable-controlled access.



Note: $\overline{E1} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

FIGURE 4. Timing waveforms - continued.

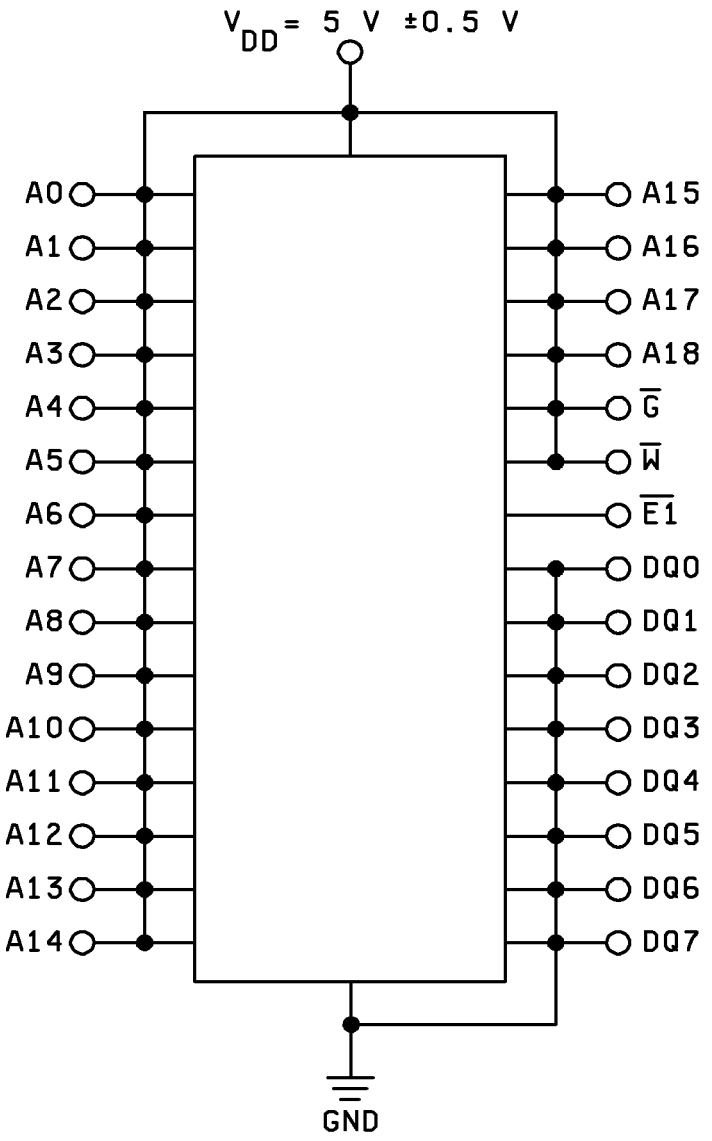


FIGURE 5. Radiation test circuit.

4.2.2 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's QM plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q, T and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device class M, procedures and circuits shall be manitained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes T, Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

e. Subgroup 4 (capacitance measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 Mhz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125EC, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (inaccordance with MIL-STD-883, method 5005,table1)	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class M	Device class Q	Device class V	Device class T
1	Interim electrical parameters (see 4.2)	- - -	- - -	1,7,9	As specified in QM plan
2	Static burn-in I and II (method 1015)	Not required	Not required	Required	
3	Same as line 1	- - -	- - -	1*, 7* Δ	
4	Dynamic burn-in (method 1015)	Required	Required	Required	
5	Same as line 1	- - -	- - -	1*, 7* Δ	
6	Final electrical parameters	1*,2,3,7*,8A,8B, 9,10,11	1*,2,3,7*,8A, 8B,9,10,11	1*,2,3,7*,8A, 8B,9,10,11	
7	Group A test requirements	1,2,3,4**,7,8A,8B, 9,10,11	1,2,3,4**,7, 8A,8B,9,10,11	1,2,3,4**,7,8A, 8B,9,10,11	
8	Group C end-point electrical parameters	2,3,7,8A,8B	2,3,7,8A,8B	1,2,3,7,8A,8B, 9,10,11 Δ	
9	Group D end-point electrical parameters	2,3,8A,8B	2,3,8A,8B	2,3,8A,8B	
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9	

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limited shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified the manufacturer's QM plan.
7/ See 4.4.1d.

4.4.2.2 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in table IIA herein. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. The end-point electrical parameters for class T shall be as specified in the table I, Group A subgroups, or as modified in the QM plan.

Table IIB. Delta limits at +25EC.

Test 1/	All device types
I_{DD2}	" 10% of specified value in table I or 35 µA, whichever is greater 2/

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

2/ If device is tested at or below 35 µA, no deltas are required.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25EC " 5EC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q, T and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V and T devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at inital qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60E to the normal, inclusive (i.e. 0E# angle # 60E). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $ 100 errors or $ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $ 20 microns in silicon.

e. The test temperature shall be +25 EC and the maximum rated operating temperature " 10 EC.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA,Columbus, Ohio 43216-5000, or telephone (614)692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

APPENDIX

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-09-28

Approved sources of supply for SMD 5962-99607 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962D9960701TUC	65342	UT8Q512-UCC
5962D9960701TUA	65342	UT8Q512-UCA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronics Systems Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-3486