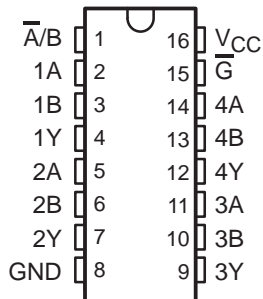


# SN54HCT157, SN74HCT157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

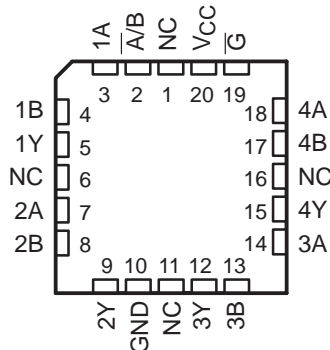
SCLS071D – NOVEMBER 1988 – REVISED OCTOBER 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current Outputs Drive Up To 15 LSTTL Loads
- Typical  $t_{pd} = 15$  ns
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible
- Buffered Inputs and Outputs

SN54HCT157 ... J OR W PACKAGE  
SN74HCT157 ... D OR N PACKAGE  
(TOP VIEW)



SN54HCT157 ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe ( $\overline{G}$ ) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HCT157N	SN74HCT157N
	SOIC – D	Tube of 40	SN74HCT157D	HCT157
		Reel of 2500	SN74HCT157DR	
		Reel of 250	SN74HCT157DT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCT157J	SNJ54HCT157J
	CFP – W	Tube of 150	SNJ54HCT157W	SNJ54HCT157W
	LCCC – FK	Tube of 55	SNJ54HCT157FK	SNJ54HCT157FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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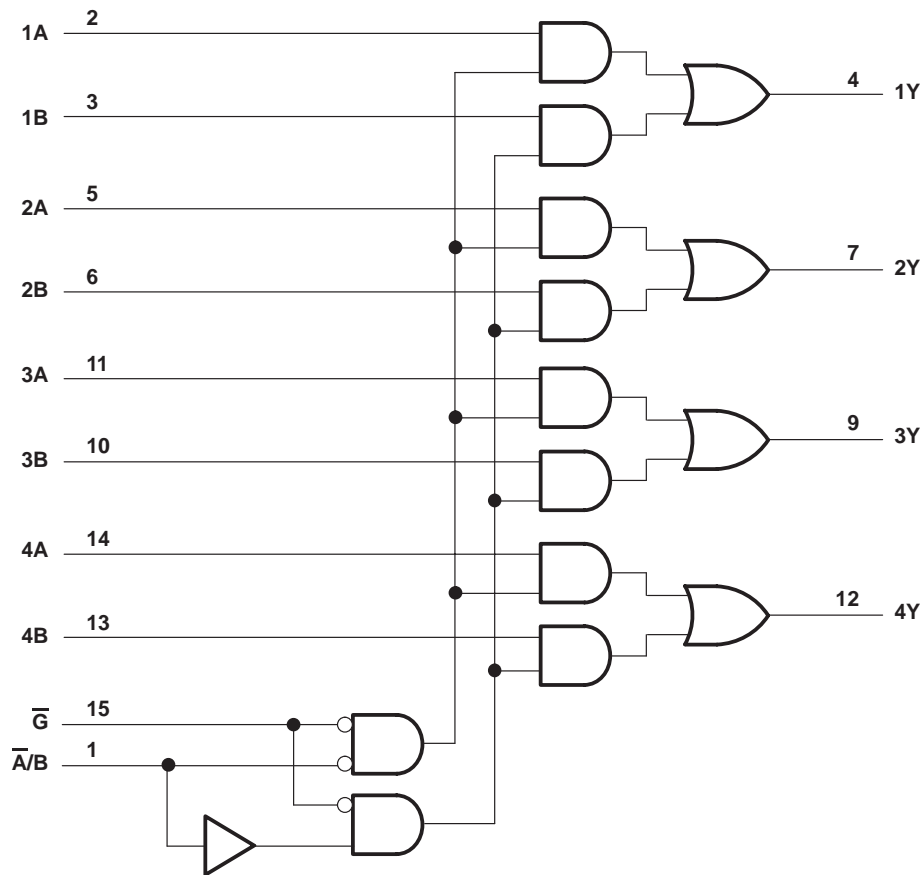
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SN54HCT157, SN74HCT157  
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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FUNCTION TABLE				
INPUTS				OUTPUT Y
STROBE $\overline{G}$	SELECT $\overline{A/B}$	DATA		
		A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

# SN54HCT157, SN74HCT157

## QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS071D – NOVEMBER 1988 – REVISED OCTOBER 2003

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±35 mA
Continuous current through $V_{CC}$ or GND	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
N package	67°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

			SN54HCT157			SN74HCT157			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2			2			V
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			0.8			0.8	V
$V_I$	Input voltage		0	$V_{CC}$		0	$V_{CC}$		V
$V_O$	Output voltage		0	$V_{CC}$		0	$V_{CC}$		V
$t_t$	Input transition (rise and fall) time			500			500		ns
$T_A$	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT157		SN74HCT157		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\ \mu\text{A}$	4.4	4.499		4.4		4.4		V
		$I_{OH} = -6\ \text{mA}$	3.98	4.3		3.7		3.84		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\ \mu\text{A}$		0.001	0.1		0.1		0.1	V
		$I_{OL} = 6\ \text{mA}$		0.17	0.26		0.4		0.33	
$I_I$	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V			8		160		80	μA
$\Delta I_{CC}^\dagger$	One input at 0.5 V or 2.4 V, Other inputs at 0 or $V_{CC}$	5.5 V		1.4	2.4		3		2.9	mA
$C_i$		4.5 V to 5.5 V		3	10		10*		10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

<sup>†</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or  $V_{CC}$ .

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# SN54HCT157, SN74HCT157

## QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT157		SN74HCT157		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	4.5 V		18	28		42		35	ns
			5.5 V		15	25		38		32	
	$\bar{A}/B$	Y	4.5 V		20	32		48		40	
			5.5 V		17	29		43		36	
	$\bar{G}$	Y	4.5 V		18	26		39		33	
			5.5 V		15	23		35		30	
$t_t$		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

switching characteristics over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT157		SN74HCT157		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	4.5 V		23	42		63		52	ns
			5.5 V		19	38		52		46	
	$\bar{A}/B$	Y	4.5 V		24	46		72		58	
			5.5 V		21	41		61		52	
	$\bar{G}$	Y	4.5 V		21	39		58		48	
			5.5 V		19	35		49		43	
$t_t$		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	12	pF

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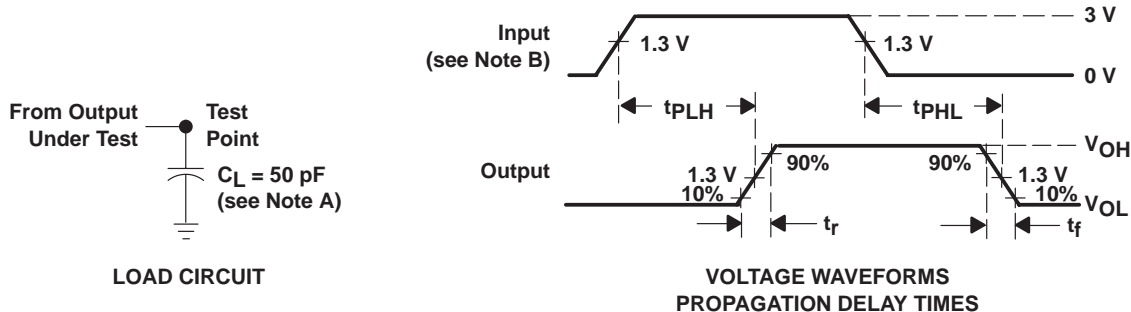


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# SN54HCT157, SN74HCT157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74HCT157D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT157DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT157DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT157DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT157DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT157DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT157DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT157DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT157DTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT157N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HCT157NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

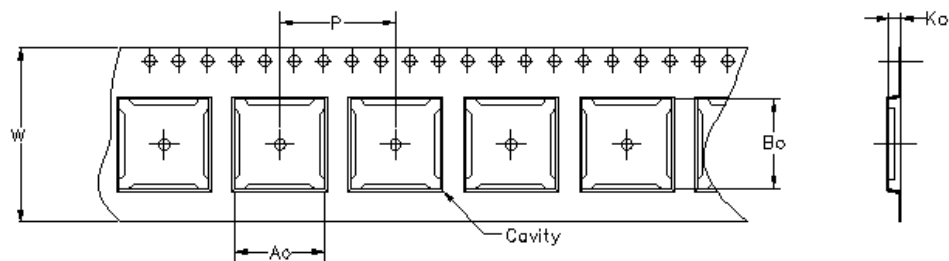
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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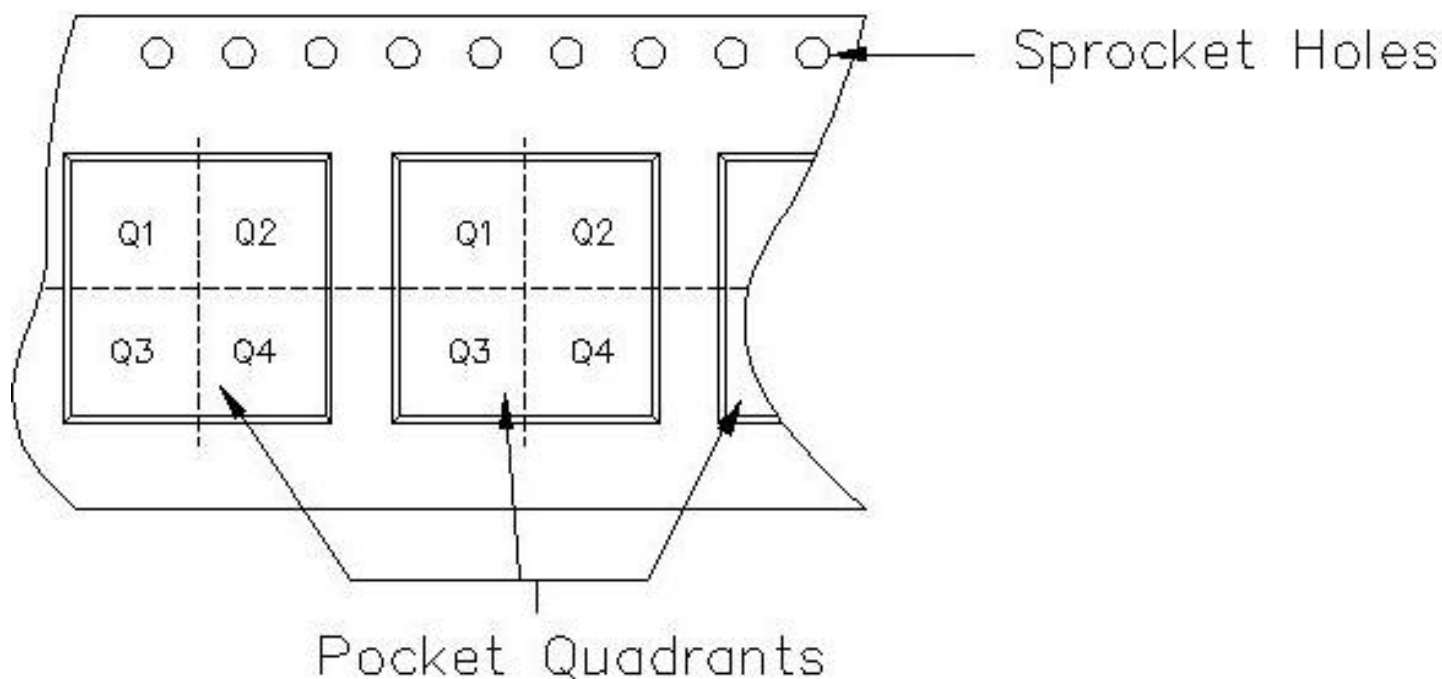
to Customer on an annual basis.





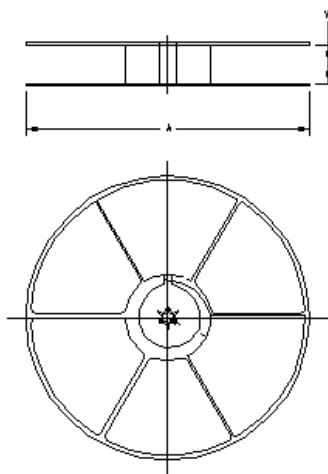
Carrier tape design is defined largely by the component length, width, and thickness.

$A_0$ = Dimension designed to accommodate the component width.
$B_0$ = Dimension designed to accommodate the component length.
$K_0$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



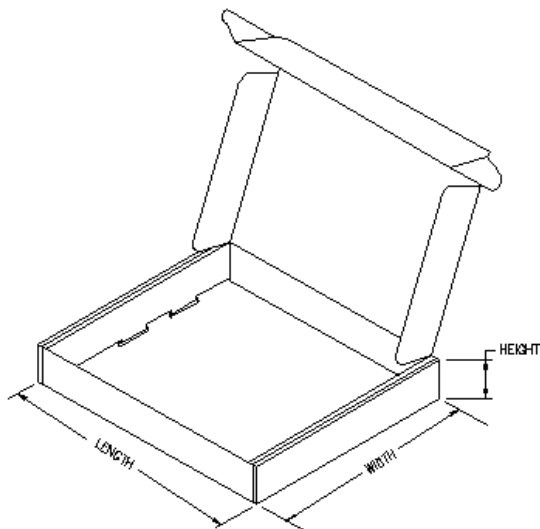
## TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT157DR	D	16	FMX	330	16	6.5	10.3	12.1	2	16	Q1



## TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74HCT157DR	D	16	FMX	342.9	336.6	28.58



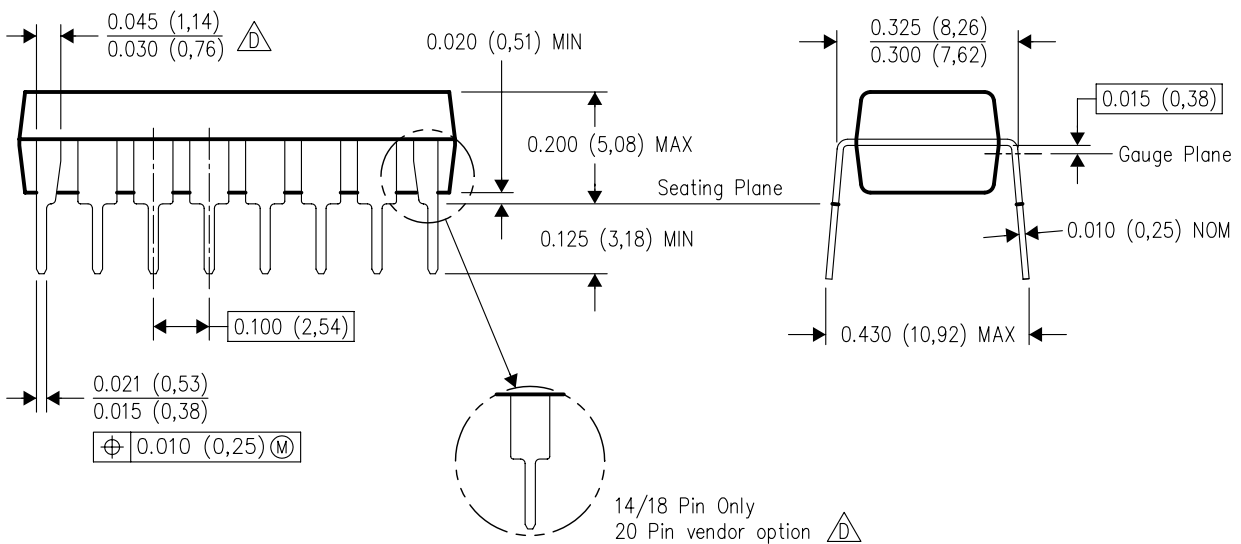
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
-  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
-  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

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