



Integrated Device Technology, Inc.

HIGH-PERFORMANCE IDT54/74FCT841/2841AT/BT/CT/DT CMOS BUS INTERFACE LATCHES

FEATURES:

- **Common features:**
 - A, B, C and D speed grades
 - Low input and output leakage $\leq 1\mu\text{A}$ (max.)
 - CMOS power levels
 - True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
 - Meets or exceeds JEDEC standard 18 specifications
 - Product available in Radiation Tolerant and Radiation Enhanced versions
 - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
 - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT841T:**
 - High drive outputs (-15mA IOH, 48mA IOL)
 - Power off disable outputs permit "live insertion"
- **Features for FCT2841T:**
 - Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise

DESCRIPTION:

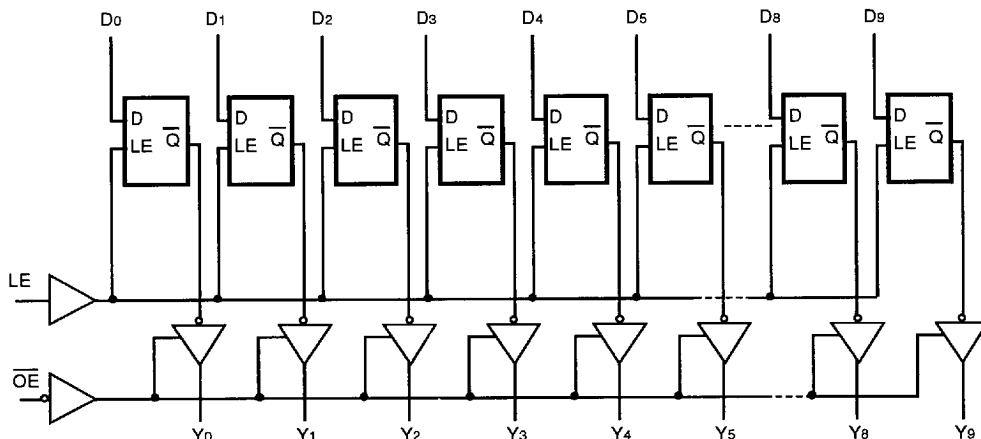
The IDT54/74FCT8xx series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT841AT/BT/CT/DT bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841/2841AT/BT/CT/DT are buffered, 10-bit wide versions of the popular '373 function. They are ideal for use as an output port requiring high IOH/IOH.

All of the IDT54/74FCT8xx high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

The IDT54/74FCT2841AT/BT/CT/DT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall-times-reducing the need for external series terminating resistors. The IDT54/74FCT2xxxT parts are plug-in replacements for IDT54/74FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAM



2571 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

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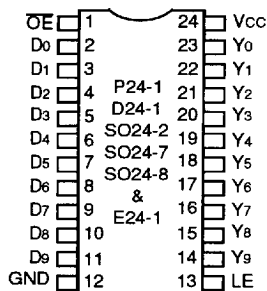
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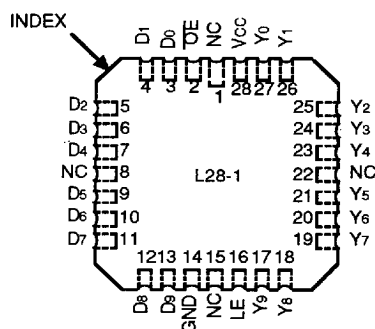
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PIN CONFIGURATIONS

DIP/SSOP/SSOP/QSOP/CERPACK
TOP VIEW

2571 drw 02

LCC
TOP VIEW

2571 drw 03

PIN DESCRIPTION

Name	I/O	Description
Di	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Yi	O	The 3-state latch outputs.
OE	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs Yi are in high-impedance (off) state.

2571 tbl 01

FUNCTION TABLE⁽¹⁾

Inputs			Internal	Output	Function
OE	LE	Di	Qi	Yi	
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

2571 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	-0.5 to Vcc + 0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

2571 lmk 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

2. Input and Vcc terminals only.

3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COU	Output Capacitance	VOUT = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

2571 lmk 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾		$V_I = 0.5\text{V}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC}		—	0.01	1	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT841T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -6\text{mA MIL.}$	2.4	3.3	—	V
			$I_{OH} = -8\text{mA COM'L.}$	—	—	—	—
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 32\text{mA MIL.}$ $I_{OL} = 48\text{mA COM'L.}$	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$		—	—	± 1	μA

2571 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT2841T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		60	115	150	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-60	-115	-150	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V

2571 Ink 07

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾			Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾			—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open OE = GND LE = V _{CC} One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	FCTxxxT FCT2xxxT	— —	0.15 0.06	0.25 0.12	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle OE = GND LE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND V _{IN} = 3.4 V _{IN} = GND	FCTxxxT FCT2xxxT FCTxxxT FCT2xxxT	— — — —	1.5 0.6 1.8 0.9	3.5 2.2 4.5 3.2	mA
		V _{CC} = Max. Outputs Open f _i = 2.5MHz 50% Duty Cycle OE = GND LE = V _{CC} Eight Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND V _{IN} = 3.4 V _{IN} = GND	FCTxxxT FCT2xxxT FCTxxxT FCT2xxxT	— — — —	3.0 1.2 5.0 3.2	6.0 ⁽⁵⁾ 3.4 ⁽⁵⁾ 14.0 ⁽⁵⁾ 11.4 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} \cdot D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions ⁽¹⁾	FCT841AT FCT2841AT				FCT841BT FCT2841BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay DI to Y _I (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay LE to Y _I	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	
tPZH tPZL	Output Enable Time $\overline{OE}$ to Y _I	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Y _I	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	
tSU	Data to LE Set-up Time	CL = 50pF	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time	RL = 500Ω	2.5	—	3.0	—	2.5	—	2.5	—	ns
tW	LE Pulse Width HIGH ⁽³⁾		4.0	—	5.0	—	4.0	—	4.0	—	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

- These parameters are guaranteed but not tested.
- These conditions are guaranteed but not tested.

2571 tbi 09

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions ⁽¹⁾	FCT841CT FCT2841CT				FCT841DT FCT2841DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay DI to Y _I (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	5.5	1.5	6.3	1.5	4.2	—	—	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	13.0	1.5	15.0	1.5	8.0	—	—	
tPLH tPHL	Propagation Delay LE to Y _I	CL = 50pF RL = 500Ω	1.5	6.4	1.5	6.8	1.5	4.0	—	—	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	15.0	1.5	16.0	1.5	8.0	—	—	
tPZH tPZL	Output Enable Time OE to Y _I	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.3	1.5	4.8	—	—	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	12.0	1.5	13.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time OE to Y _I	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	5.7	1.5	6.0	1.5	4.0	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	6.3	1.5	4.0	—	—	
tSU	Data to LE Set-up Time	CL = 50pF	2.5	—	2.5	—	1.5	—	—	—	ns
tH	Data to LE Hold Time	RL = 500Ω	2.5	—	2.5	—	1.0	—	—	—	ns
tW	LE Pulse Width HIGH ⁽³⁾		4.0	—	4.0	—	3.0	—	—	—	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

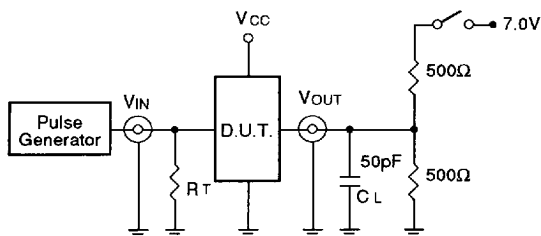
- These parameters are guaranteed but not tested.
- These conditions are guaranteed but not tested.

2571 tbi 10

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2571 drw 08

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

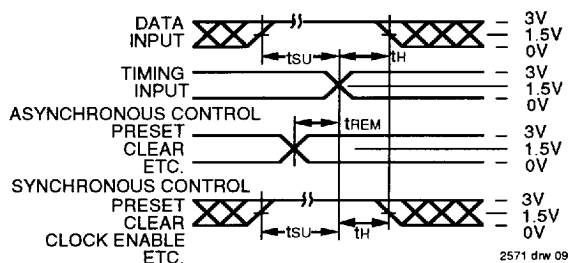
DEFINITIONS:

CL = Load capacitance; includes jig and probe capacitance.

RT = Termination resistance; should be equal to ZOUT of the Pulse Generator.

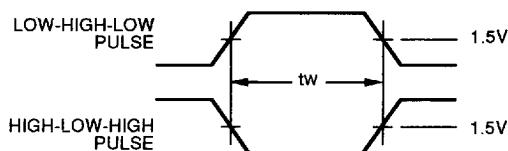
2571 Ink 11

SET-UP, HOLD AND RELEASE TIMES



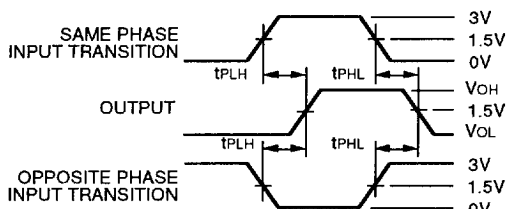
2571 drw 09

PULSE WIDTH



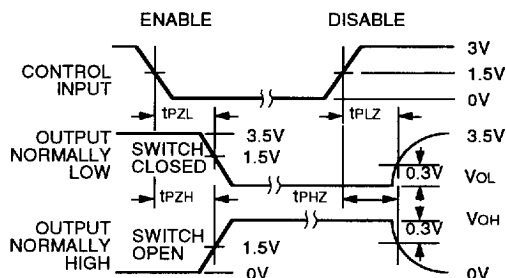
2571 drw 10

PROPAGATION DELAY



2571 drw 11

ENABLE AND DISABLE TIMES



2571 drw 12

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_h \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT	XX	FCT	X	XXXX	X	X	
Temp. Range			Family	Device Type	Package	Process	
						Blank	Commercial
						B	MIL-STD-883, Class B
						P	Plastic DIP
						D	CERDIP
						E	CERPACK
						L	Leadless Chip Carrier
						SO	Small Outline IC
						PY	Shrink Small Outline Package
						Q	Quarter-size Small Outline Package
						841AT	10-Bit Non-Inverting Latch
						841BT	
						841CT	
						841DT	
						Blank	High Drive
						2	Balanced Drive
						54	-55°C to +125°C
						74	0°C to +70°C

2571 drw 13