HT82V24

16-Bit, 15MSPS, 3-Channel CCD/CIS Analog Signal Processor

Features

- Operating voltage: 5V
- Low power consumption at 380mW (Typ.)
- Power-down mode: Under 2μA (Typ.)
- 16-bit 15 MSPS A/D converter
- Supports ADI/WM mode data output formats selection
- Guaranteed won't miss codes
- 1~6x programmable gain
- Correlated Double Sampling
- ±300mV programmable offset
- Input clamp circuitry
- Internal voltage reference
- Multiplexed byte/nibble-wide output (8×2/4×4 format)
- Programmable 3-wire serial interface
- 3V/5V digital I/O compatibility
- 3-channel operation up to 5 MSPS for each channel
- 2-channel (Even-Odd) operation up to 7.5 MSPS for each channel
- 1-channel operation up to 15 MSPS
- 20/28-pin SOP/SSOP package (Pb-free on request)

Applications

Flatbed document scanners

Film scanners

Digital color copiers

Multifunction peripherals

General Description

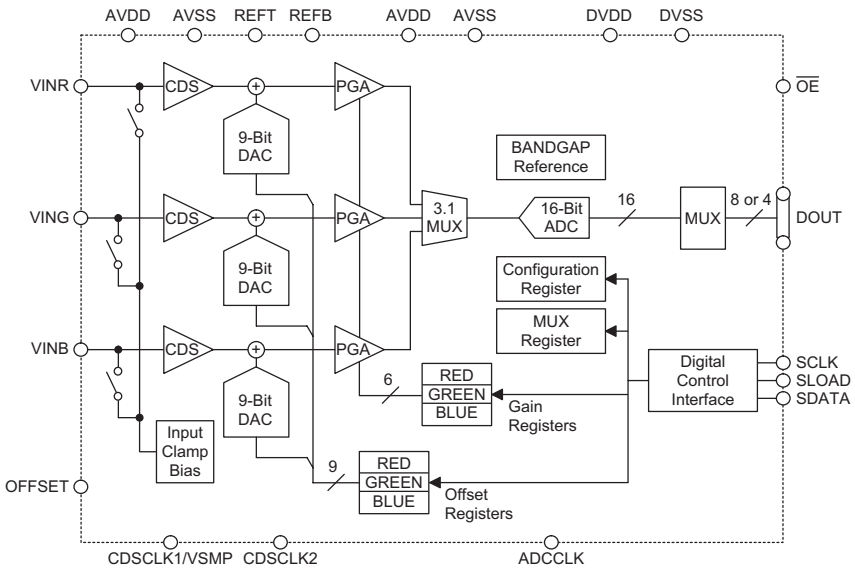
The HT82V24 is a complete analog signal processor for CCD imaging applications. It features a 3-channel architecture designed to sample and condition the outputs of tri-linear color CCD arrays. Each channel consists of an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA), and a high performance 16-bit A/D converter.

The CDS amplifiers may be disabled for use with sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, which do not require CDS.

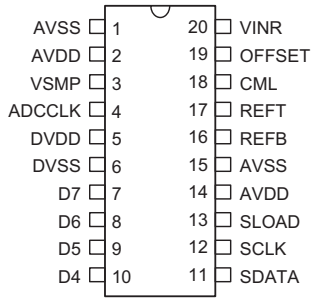
The 16-bit digital output is multiplexed into an 8/4-bit output word that is accessed using two/four read cycles. The internal registers are programmed through a 3-wire serial interface, which provides gain, offset and operating mode adjustments. HT82V24 supports ADI/WM mode data output formats.

The HT82V24 operates from a single 5V power supply, typically consumes 380mW of power.

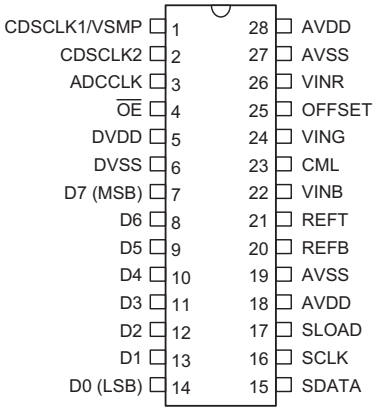
Block Diagram



Pin Assignment



HT82V24
−20 SOP-A/SSOP-A



HT82V24
−28 SOP-A/SSOP-A

Pin Description

Pin Name	I/O	Description
CDSCLK1/VSMP	DI	CDS reference clock pulse input ADI mode: CDSCLK1 WM mode: VSMP
CDSCLK2	DI	CDS data clock pulse input
ADCCLK	DI	A/D sample clock input for 3-channels mode
$\overline{OE}$	DI	Output enable, active low
DVDD	P	Digital power
DVSS	P	Digital ground
D7~D0	DO	Digital data output
SDATA	DI/DO	Serial data input/output
SCLK	DI	Clock input for serial interface
SLOAD	DI	Serial interface load pulse
AVSS	P	Analog ground
AVDD	P	Analog supply
REFB	AO	Reference decoupling
REFT	AO	Reference decoupling
VINB	AI	Analog input, blue
CML	AO	Internal reference output
VING	AI	Analog input, green
OFFSET	AO	Clamp bias level decoupling
VINR	AI	Analog input, red

Absolute Maximum Ratings

Supply Voltage .....V_{SS}–0.3V to V_{SS}+5.5V

Input Voltage .....V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature .....–50°C to 125°C

Operating Temperature .....–25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Logic Inputs							
V_{IH}	High Level Input Voltage	—	—	$0.8\times DV_{DD}$	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	—	$0.2\times DV_{DD}$	V
I_{IH}	High Level Input Current	—	—	—	10	—	μA
I_{IL}	Low Level Input Current	—	—	—	10	—	μA
C_{IN}	Input Capacitance	—	—	—	10	—	pF
Logic Outputs							
V_{OH}	High Level Output Voltage	—	—	$DV_{DD}-0.5$	—	—	V
V_{OL}	Low Level Output Voltage	—	—	—	—	0.5	V
I_{OH}	High Level Output Current	5V	—	—	0.7	—	mA
I_{OL}	Low Level Output Current	5V	—	—	1.1	—	mA

A.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Power Supplies							
AV_{DD}	Analog Power	—	—	4.75	5	5.25	V
DV_{DD}	Digital I/O Power	—	—	3	5	5.25	V
Maximum Conversion Rate							
f_{MAX3}	3-channel Mode with CDS	—	—	15	—	—	MSPS
f_{MAX2}	2-channel Mode with CDS	—	—	15	—	—	MSPS
f_{MAX1}	1-channel Mode with CDS	—	—	15	—	—	MSPS
Accuracy (Entire Signal Path)							
	ADC Resolution	—	—	—	16	—	Bits
	Integral Nonlinear (INL)	—	—	—	±32	—	LSB
	Differential Nonlinear (DNL)	—	—	–1	—	1	LSB
	Offset Error	—	—	–150	—	150	mV
	Gain Error	—	—	—	5	—	%FSR
Analog Inputs							
R_{FS}	Full-scale Input Range	—	—	—	2.0/3.0*	—	Vp-p
V_i	Input Limits	—	—	A_{VSS}-0.3	—	A_{VDD}+0.3	V
C_i	Input Capacitance	—	—	—	10	—	pF
I_i	Input Current	—	—	—	10	—	nA
Amplifiers							
	PGA Gain at Minimum	—	—	—	1	—	V/V
	PGA Gain at Maximum	—	—	—	6	—	V/V
	PGA Gain Resolution	—	—	—	6	—	Bits
	Programmable Offset at Minimum	—	—	—	–300	—	mV
	Programmable Offset at Maximum	—	—	—	300	—	mV
	Offset Resolution	—	—	—	9	—	Bits

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Temperature Range							
t_A	Operating	—	—	0	—	70	°C
Power Consumption							
P_{tot3}	Total Power Consumption (3CH)	—	—	—	380	—	mW
P_{tot2}	Total Power Consumption (2CH)	—	—	—	340	—	mW
P_{tot1}	Total Power Consumption (1CH)	—	—	—	300	—	mW

Note: "*" means the full-scale input range select by configuration register

Timing Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock Parameters					
t_{PRA}	3-channel pixel rate	200	—	—	ns
t_{PRB}	2-channel (Even-Odd) pixel rate	133	—	—	ns
t_{PRC}	1-channel pixel rate	66	—	—	ns
t_{ADCLK}	ADCCLK Pulse Width	33	—	—	ns
t_{C1}	CDSCLK1 Pulse Width	15	30	—	ns
t_{C2}	CDSCLK2 Pulse Width	15	30	—	ns
t_{C1C2}	CDSCLK1 Falling to CDSCLK2 Rising	0	—	—	ns
t_{ADC2}	ADCCLK Rising to CDSCLK2 Falling	0	—	—	ns
t_{C2ADR}	CDSCLK2 Rising to ADCCLK Rising	5	—	—	ns
t_{C2ADF}	CDSCLK2 Falling to ADCCLK Falling	30	—	—	ns
t_{C2C1}	CDSCLK2 Falling to CDSCLK1 Rising	30	—	—	ns
t_{AD}	Analog Sampling Delay	—	5	—	ns
Serial Interface					
f_{SCLK}	Maximum SCLK Frequency	10	—	—	MHz
t_{LS}	SLOAD to SCLK Setup Time	10	—	—	ns
t_{LH}	SCLK to SLOAD Hold Time	10	—	—	ns
t_{DS}	SDATA to SCLK Rising Setup Time	10	—	—	ns
t_{DH}	SCLK Rising to SDATA Hold Time	10	—	—	ns
t_{RDV}	Falling to SDATA Valid	10	—	—	ns
Data Output					
t_{OD}	Output Delay	—	12	—	ns

Functional Description

Integral Nonlinear (INL)

Integral nonlinear error refers to the deviation of each individual code from a line drawn from zero scale through a positive full scale. The point used as zero scale occurs 1/2 LSB before the first code transition. A positive full scale is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinear (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed for the 16-bit resolution indicates that all the 65536 codes respectively, are present in the over-all operating range.

Offset Error

The first ADC code transition should occur at a level 1/2 LSB above the nominal zero scale voltage.

The offset error is the deviation of the actual first code transition level from the ideal level.

Gain Error

The last code transition should occur for an analog value of 1/2 LSB below the nominal full-scale voltage.

Gain error is the deviation of the actual difference between the first and the last code transitions and the ideal difference between the first and the last code transitions.

Sampling Delay

The sampling delay is the time delay that occurs when a sampling edge is applied to the HT82V24 until the actual sample of the input signal is held. Both CDSCLK1 and CDSCLK2 sample the input signal during the transition from high to low, so the sampling delay is measured from each clock′s falling edge to the instant the actual internal sample is taken.

Internal Register Descriptions

Register Name	Address			Data Bits								
	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	0	0	0	0	Don′t care		3-CH	CDS on	Clamp Voltage	Enable Power Down	Input Range	1 byte out
MUX	0	0	1	0	RGB/ BGR	Red	Green	Blue	0	0	0	0
Red PGA	0	1	0	0	0	0	MSB					LSB
Green PGA	0	1	1	0	0	0	MSB					LSB
Blue PGA	1	0	0	0	0	0	MSB					LSB
Red Offset	1	0	1	MSB								LSB
Green Offset	1	1	0	MSB								LSB
Blue Offset	1	1	1	MSB								LSB

Internal Register Map (ADI Mode)

Register Name	Address			Data Bits								
	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	0	0	0	1	Clamp Timing Control		3-CH	CDS on	Clamp Voltage	Enable Power Down	Input Range	Output Format
MUX	0	0	1	DEL	RGB/ BGR	Red	Green	Blue	POSNNEG	VDEL		
Red PGA	0	1	0	0	0	0	MSB					LSB
Green PGA	0	1	1	0	0	0	MSB					LSB
Blue PGA	1	0	0	0	0	0	MSB					LSB
Red Offset	1	0	1	MSB								LSB
Green Offset	1	1	0	MSB								LSB
Blue Offset	1	1	1	MSB								LSB

Internal Register Map (Wolfson Mode)

Configuration Register

The configuration register controls the HT82V24′s operating mode and bias levels. Bits D7 and D6 set the clamp timing in WM mode and there are don't care in ADI Mode. Bit D5 will configure the HT82V24 for the 3-channel (high) mode of operation. Setting the bit D4 high will enable the CDS mode of operation, and setting this bit low will enable the SHA mode of operation.

Bit D3 sets the dc bias level of the HT82V24′s input clamp. This bit should always be set high for the 4V clamp bias, unless a CCD with a reset feed through transient exceeding 2V is used. Setting the bit D3 low, the clamp voltage is 3V. Bit D2 controls the power-down mode. Setting bit D2 high will place the HT82V24 into a very low power ″sleep″ mode. All register contents are retained while the HT82V24 is in the power-down state. Setting bit D1 high will select the 3V input range, otherwise the 2V input range is selected.

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Don′t care		3 channels	CDS operation	Clamp bias	Power-down	Input Range	1 byte out (High-byte only)
			1=On*	1=CDS mode*	1=4V*	1=On	1=3V	1=On
			0=Off	0=SHA mode	0=3V	0=Off (Normal)*	0=2V*	0=Off*

Configuration Register Settings (ADI Mode)

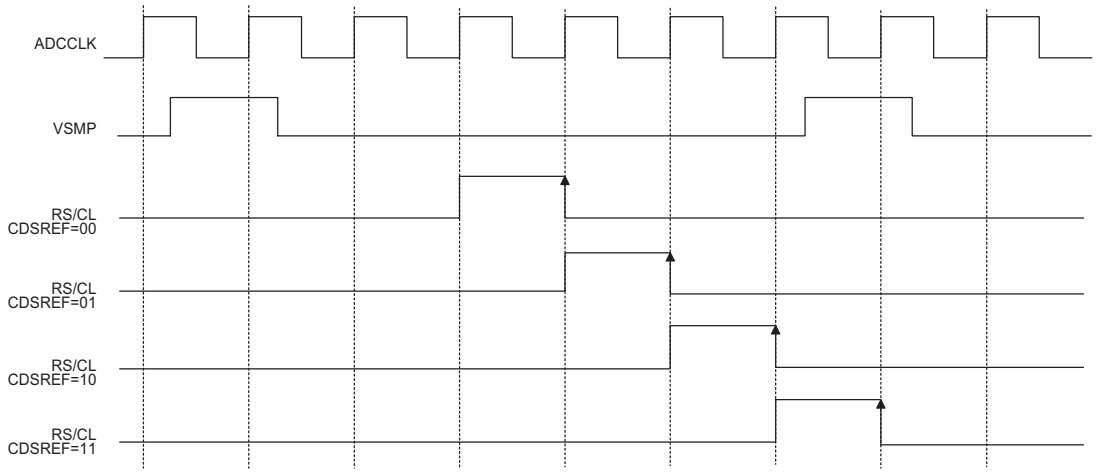
D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 1	Clamp Timing Control		3 channels	CDS operation	Clamp bias	Power-down	Input Range	Output Format
	CDSREF1	CDSREF0	1=On*	1=CDS mode*	1=4V*	1=On	1=3V	1=Byte output
	0*	0*	0=Off	0=SHA mode	0=3V	0=Off (Normal)*	0=2V*	0=Nibble output*,**

Configuration Register Settings (Wolfson Mode)

Note: * Power-on default value

** It needs D5=0, D0=0 to enable Nibble output (1CH WM mode)

Bits D7 and D6 control the reset sample and clamp timing



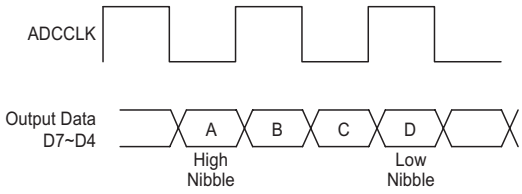
Reset Sample and Clamp Timing (RS/CL)

Note: CDSREF=(CDSREF1,CDSREF0)

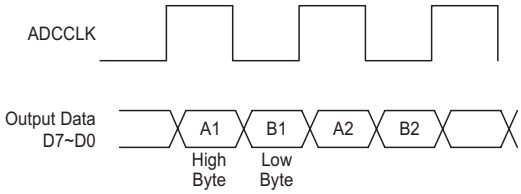
Bit D0 control the ADC output cycle of the HT82V24.

Bit D8 selects the ADC data output format selection. Setting D8 high enables the WM mode data output format while setting bit D8 low enables the ADI mode output data format. The one nibble data will output data to pins D7~D4 and 4×4 (WM) mode output the data format selected. The output format as the following table:

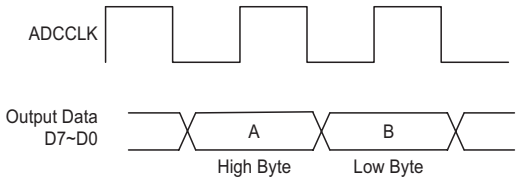
D8	D0	ADC Output Format
0	0	D5=1: 3-CH 8×2 (ADI) D5=0: 1 or 2-CH 8×2 (ADI)
0	1	D5=1: 3-CH 8×1 (ADI) D5=0: 1 or 2-CH 8×1 (ADI)
1	0	D5=0: 1-CH 4×4 (WM)
1	1	D5=1: 3-CH 8×2 (WM) D5=0: 1-CH 8×2 (WM)



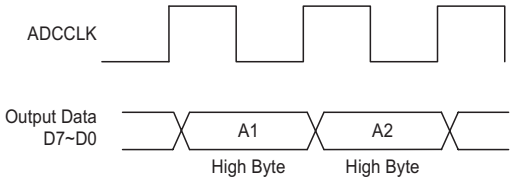
4x4 (WM) Output Data Format



8x2 (ADI) Output Data Format



8x2 (WM) Output Data Format



8x1 (ADI) Output Data Format

MUX Register

The MUX register controls the sampling channel order and the 2-channel mode configuration in the HT82V24. Bit D8 is used to set the output latency in ADC clock period and is only valid when WM mode data output format is selected. Bit D7 is used when operating in the 3-channel mode or the 2-channel mode. Setting bit D7 high will sequence the MUX to sample the red channel first, then the green channel, and then the blue channel. When in the 3-channel mode, the CDSCLK2 rising edge always resets the MUX to sample the red channel first (see timing diagrams). When bit D7 is set low, the channel order is reversed to blue first, green second, and red third. The CDSCLK2 rising edge will always reset the MUX to sample the blue channel first. Bits D6, D5 and D4 are used when operating in 1 or 2-channel mode. Bit D6 is set high to sample the red channel. Bit D5 is set high to sample the green channel. Bit D4 is set high to sample the blue channel. The MUX will remain stationary during 1-channel mode. The two channel mode is selected by setting two of the channel select bits (D4~D6) high. The MUX samples the channels in the order selected by bit D7. In WM mode, Bits D0~D2 are used to control the sampling point delay option. Bit D3 is used to select the rising or falling edge on the CDSCLK1 input pin and generates an internal VSMP pulse. Bits D0~D3 set to 0 in ADI Mode.

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	MUX Order	Channel Select			Set to 0			
	1=R-G-B*	1=RED*	1=GREEN	1=BLUE				
	0=B-G-R	0=Off	0=Off*	0=Off*				

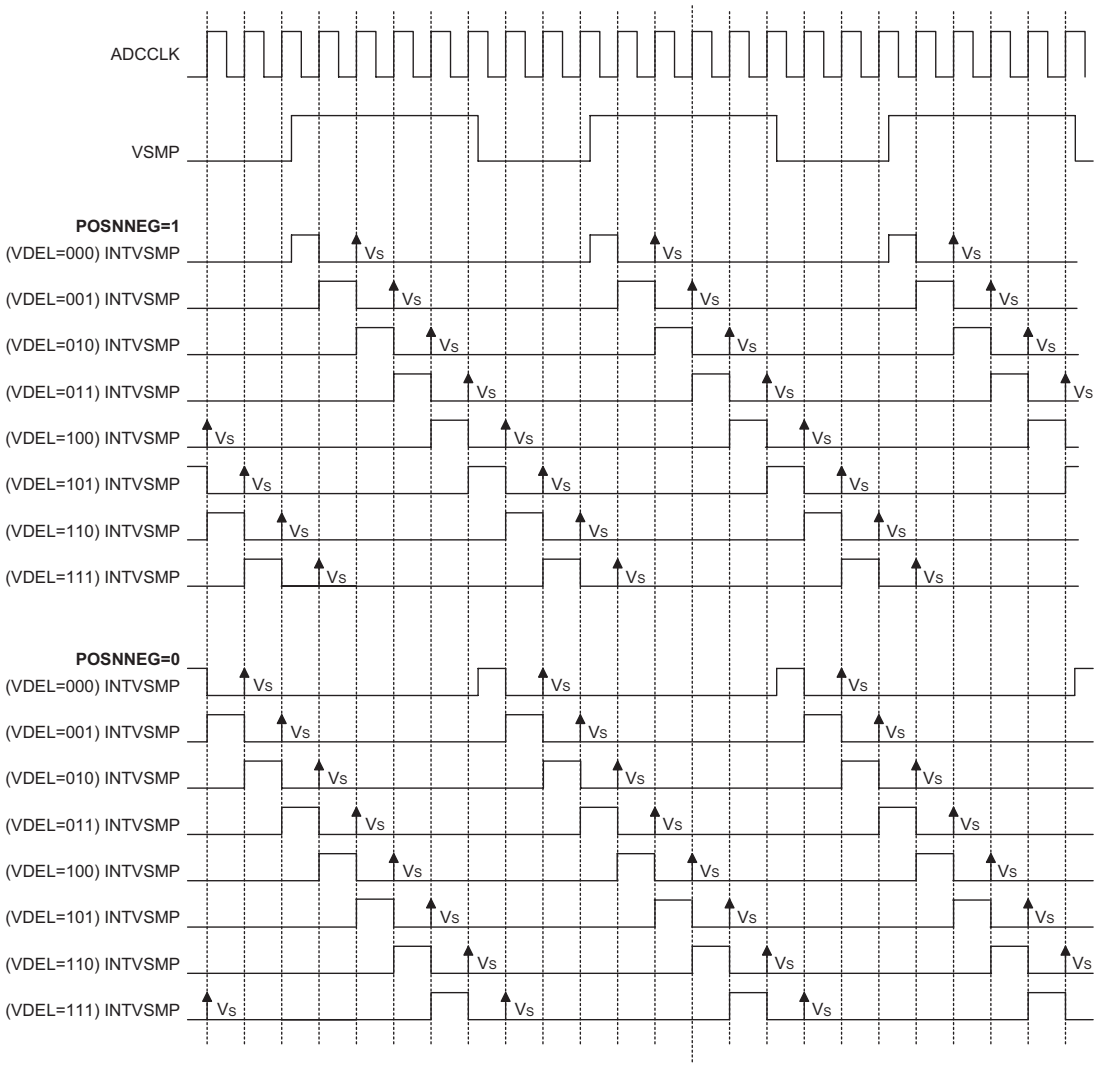
MUX Register Settings (ADI Mode)

D8	D7	D6	D5	D4	D3	D2	D1	D0
DEL	MUX Order	Channel Select			CDS Edge Detection Select	Delay Period Select		
1: Delay by two ADC clock	1=R-G-B*	1=RED*	1=GREEN	1=BLUE	POSNNEG	VDEL 2	VDEL 1	VDEL 0
0: Minimum latency*	0=B-G-R	0=Off	0=Off*	0=Off*	0*	0*	0*	0*

MUX Register Settings (Wolfson Mode)

Note: * Power-on default value

D0~D3 and D8 are valid only at WM mode.



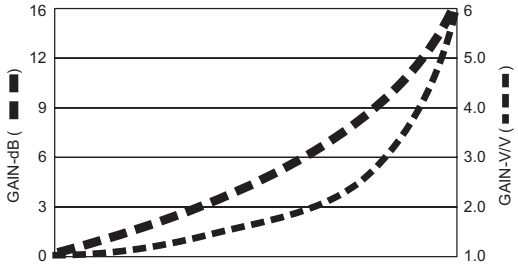
Note: VDEL=(VDEL2, VDEL1, VDEL0)

PGA Gain Registers

There are three PGA registers for use in individually programming the gain in the red, green and blue channels. Bits D8, D7 and D6 in each register must be set low, and bits D5 through D0 control the gain range in 64 increments. See figure for a graph of the PGA gain versus PGA register code. The coding for the PGA registers is a straight binary, with an all zero words corresponding to the minimum gain setting (1x) and an all one word corresponding to the maximum gain setting (6x).

The HT82V24 uses one Programmable Gain Amplifier (PGA) for each channel. Each PGA has a gain range from 1x (0dB) to 6x (15.6dB), adjustable in 64 steps. The Figure shows the PGA gain as a function of the PGA register code. Although the gain curve is approximately linear in dB, the gain in V/V varies in nonlinear proportion with the register code, according to the following the equation: $\text{Gain}=\frac{6}{1+4.85x(\frac{63-G}{63})}$

Where G is the decimal value of the gain register contents, and varies from 0 to 63.



PGA Gain Transfer Function

D8	D7	D6	D5	D4	D3	D2	D1	D0	Gain (V/V)	Gain (dB)
Set to 0	Set to 0	Set to 0	MSB					LSB		
0	0	0	0	0	0	0	0	0*	1.0	0.0
0	0	0	0	0	0	0	0	1	1.039	0.33
					.				.	.
					.				.	.
					.				.	.
0	0	0	1	1	1	1	1	0	5.57	14.9
0	0	0	1	1	1	1	1	1	6	15.6

PGA Gain Register Settings

Note: * Power-on default value

Offset Registers

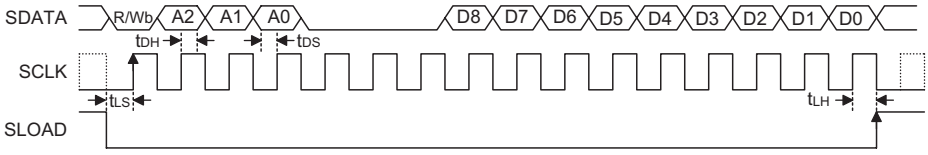
There are three offset registers for use in individually programming the offset in the red, green, and blue channels. Bits D8 through D0 control the offset range from –300mV to 300mV in 512 increments.

The coding for the offset registers is sign magnitude, with D8 as the sign bit. The following table shows the offset range as a function of the bits D8 through D0.

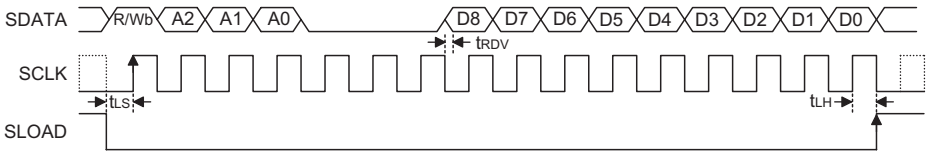
D8	D7	D6	D5	D4	D3	D2	D1	D0	Offset (mV)
MSB								LSB	
0	0	0	0	0	0	0	0	0*	0
0	0	0	0	0	0	0	0	1	1.17
					.				.
					.				.
					.				.
0	1	1	1	1	1	1	1	1	300
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	–1.17
					.				.
					.				.
					.				.
1	1	1	1	1	1	1	1	1	–300

Note: * Power-on default value

Timing Diagrams

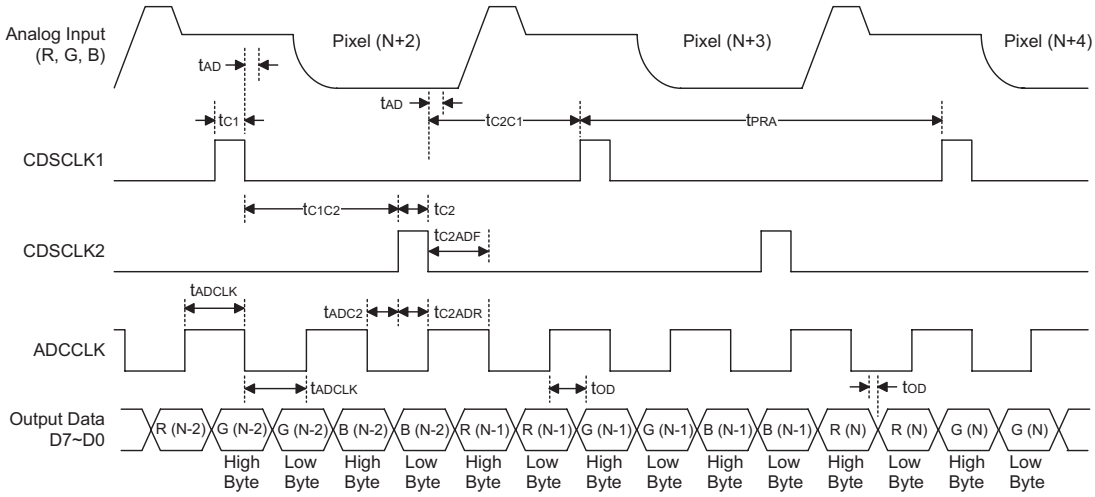


Serial Write Operation Timing

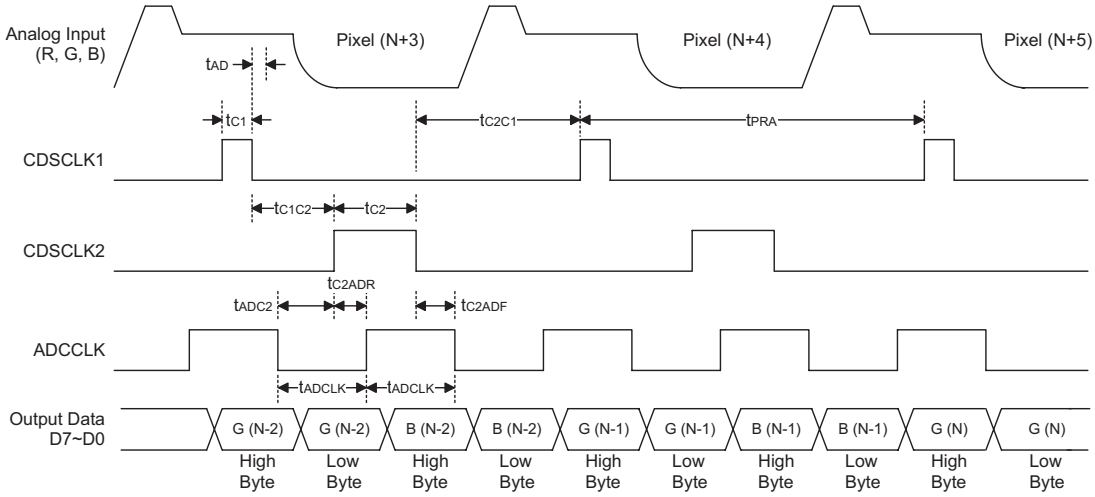


Serial Read Operation Timing

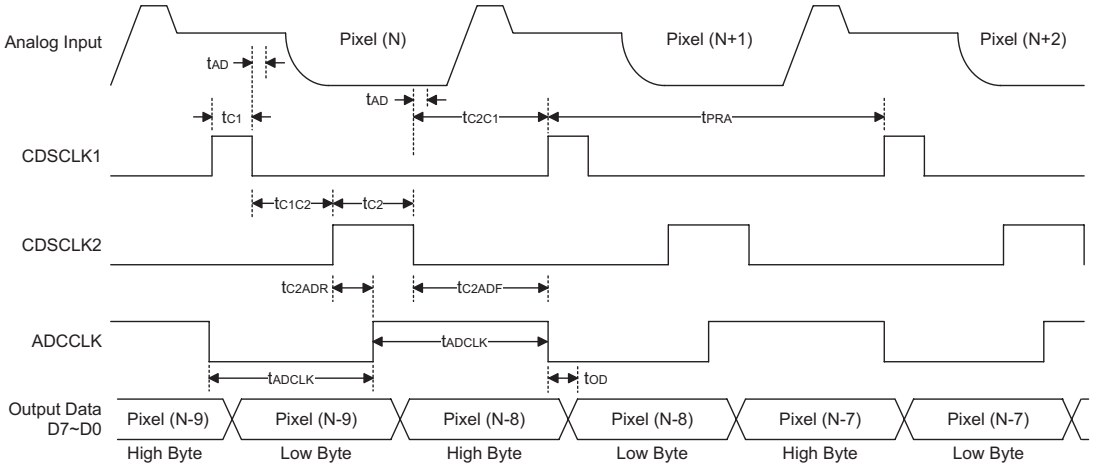
Part (A): 8×2 (ADI) Output Format



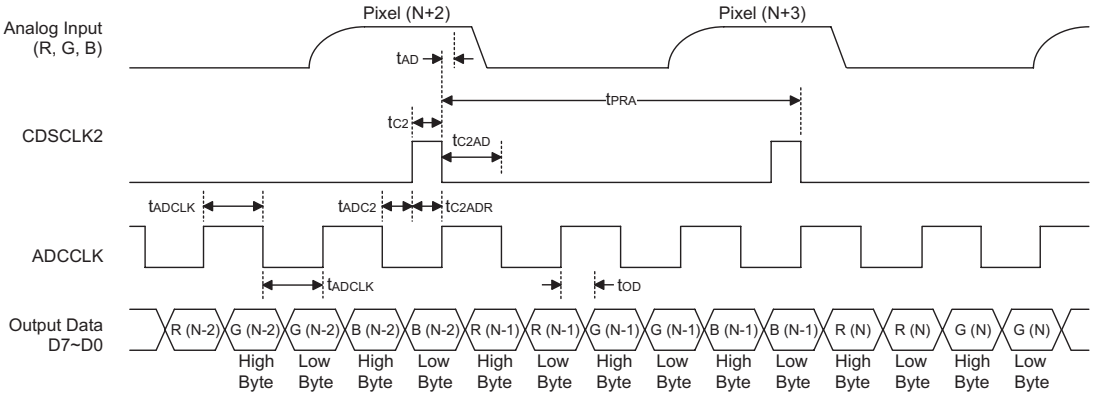
3-Channel CDS Mode Timing



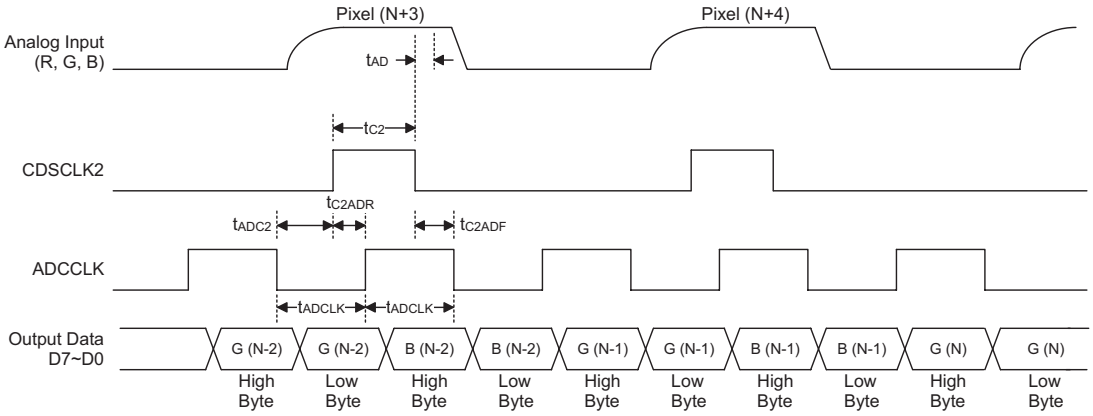
2-Channel CDS Mode Timing



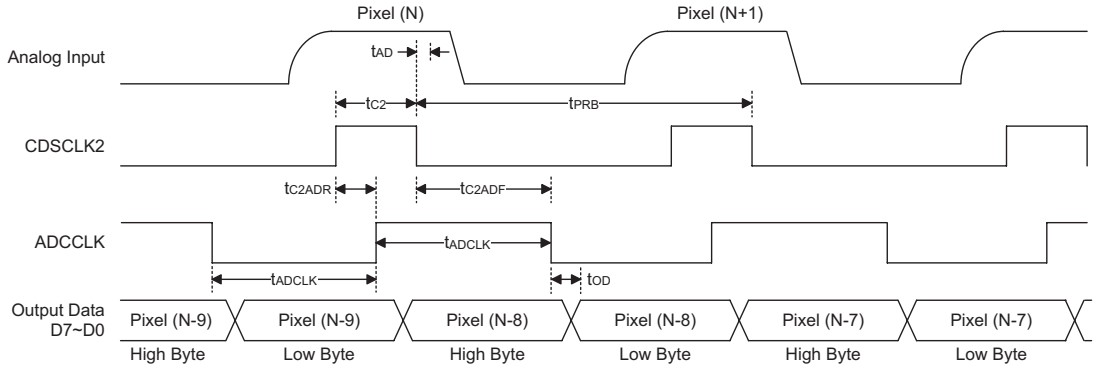
1-Channel CDS Mode Timing



3-Channel SHA Mode Timing



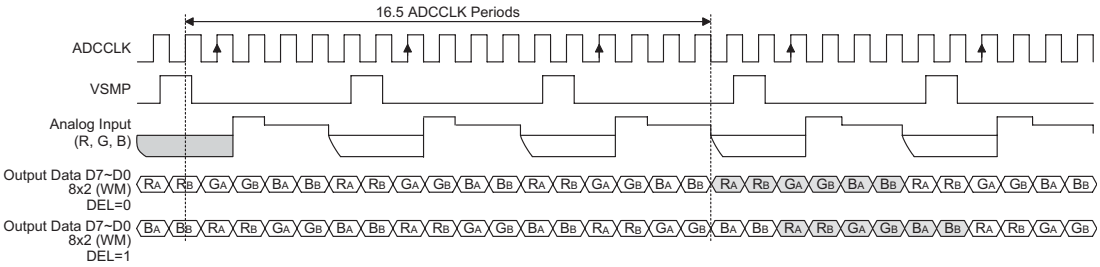
2-Channel SHA Mode Timing



1-Channel SHA Mode Timing

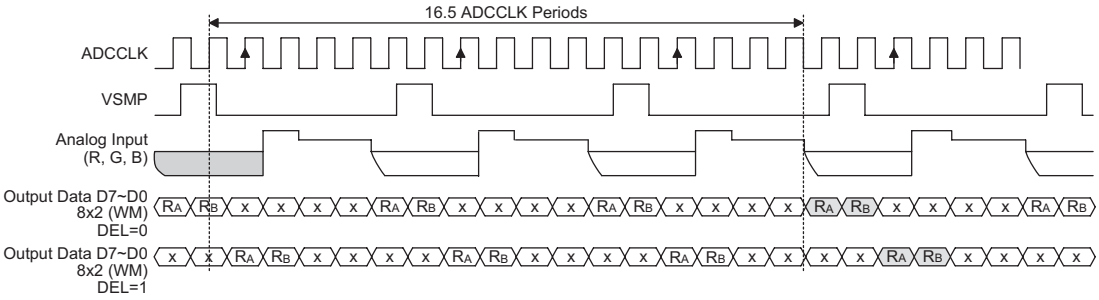
Part (B): WM Mode Output Format at VDEL=(0,0,0), POSNEG=1 (Those Diagrams are identical for both CDS and SHA Operation)

- 3-CH 8×2 (WM)



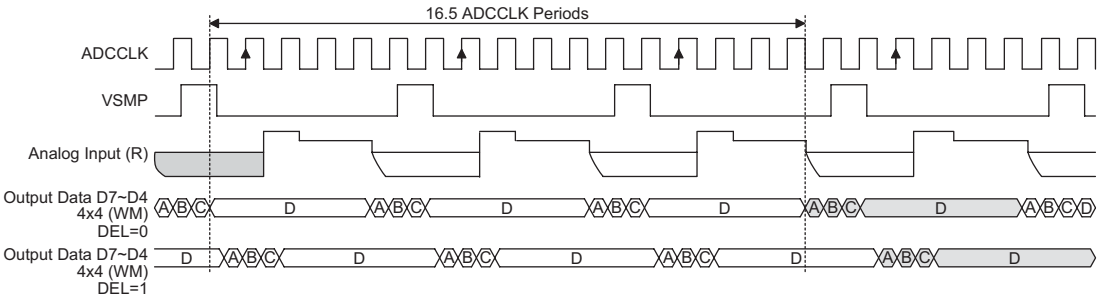
3-Channel Mode Timing (Select R-G-B Mode)

- 1-CH 8×2 (WM)



1-Channel Mode Timing (Select R Mode)

- 1-CH 4×4 (WM)

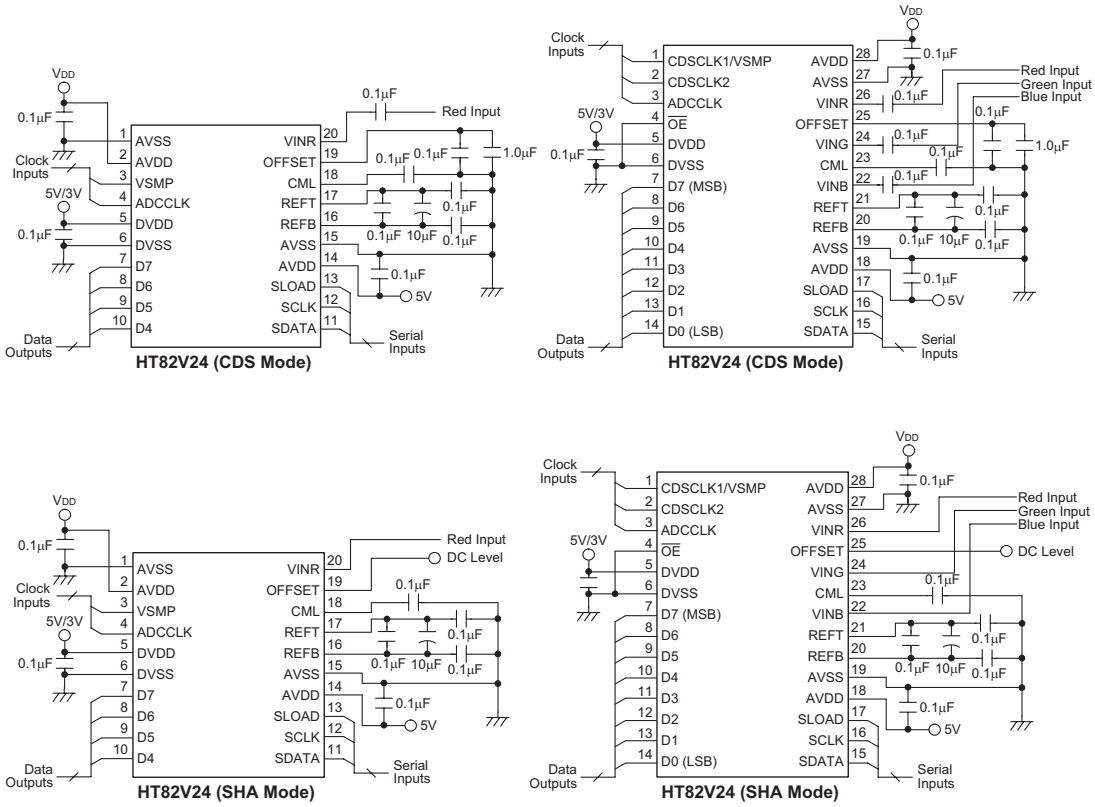


1-Channel Mode Timing (Select R Mode)

Application Circuits

The recommended circuit configuration for the 3-channel CDS mode operation is shown in the figure below (ADI mode data output format). The recommended input coupling capacitor value is 0.1μF.

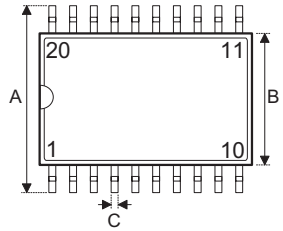
A single ground plane is recommended for the HT82V24. A separate power supply may be used for DRVDD, the digital driver supply, but this supply pin should still be decoupled to the same ground plane as with the rest of the HT82V24. The loading of the digital outputs should be minimized, either by using short traces to the digital ASIC, or by using external digital buffers. To minimize the effect of digital transients during major output code transitions, the falling edge of the CDSCLK2 should occur in coincidence with or before the rising edge of ADCCLK. All 0.1μF decoupling capacitors should be located as close as possible to the HT82V24 pins. When operating in a single channel mode, the unused analog inputs should be grounded.

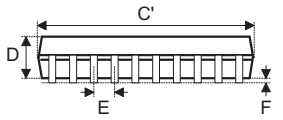


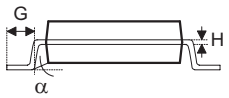
Note: For the 3-channel SHA mode, all of the above considerations also apply for this configuration, except that the analog input signals are directly connected to the HT82V24 without the use of coupling capacitors. The OFFSET pin should be grounded if the inputs to the HT82V24 are to be referenced to ground, or a DC offset voltage should be applied to the OFFSET pin in the case where a coarse offset needs to be removed from the inputs. The analog input signals must already be dc-biased between 0V and 2V, if OFFSET is connected to ground.

Package Information

20-pin SOP (300mil) Outline Dimensions

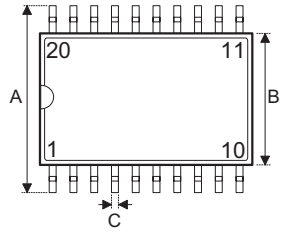


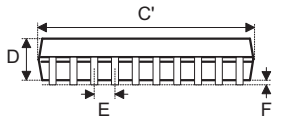


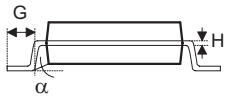


Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	394	—	419
B	290	—	300
C	14	—	20
C′	490	—	510
D	92	—	104
E	—	50	—
F	4	—	—
G	32	—	38
H	4	—	12
α	0°	—	10°

20-pin SSOP (209mil) Outline Dimensions

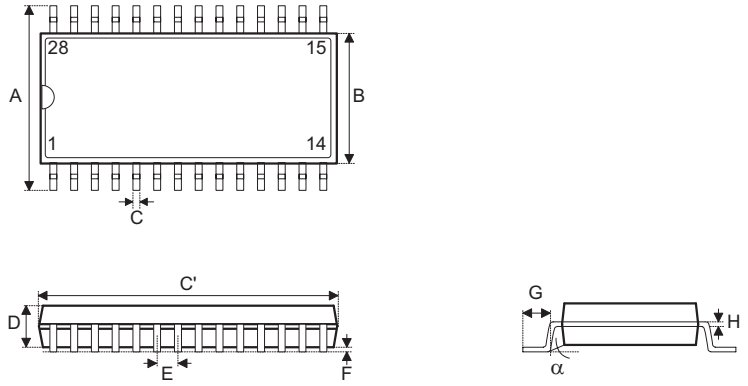






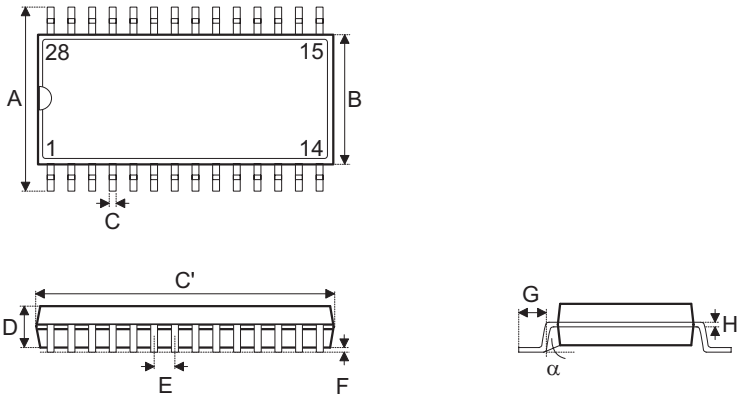
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	291	—	323
B	196	—	220
C	9	—	15
C′	271	—	295
D	65	—	73
E	—	25.59	—
F	4	—	10
G	26	—	34
H	4	—	8
α	0°	—	8°

28-pin SOP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	394	—	419
B	290	—	300
C	14	—	20
C′	697	—	713
D	92	—	104
E	—	50	—
F	4	—	—
G	32	—	38
H	4	—	12
α	0°	—	10°

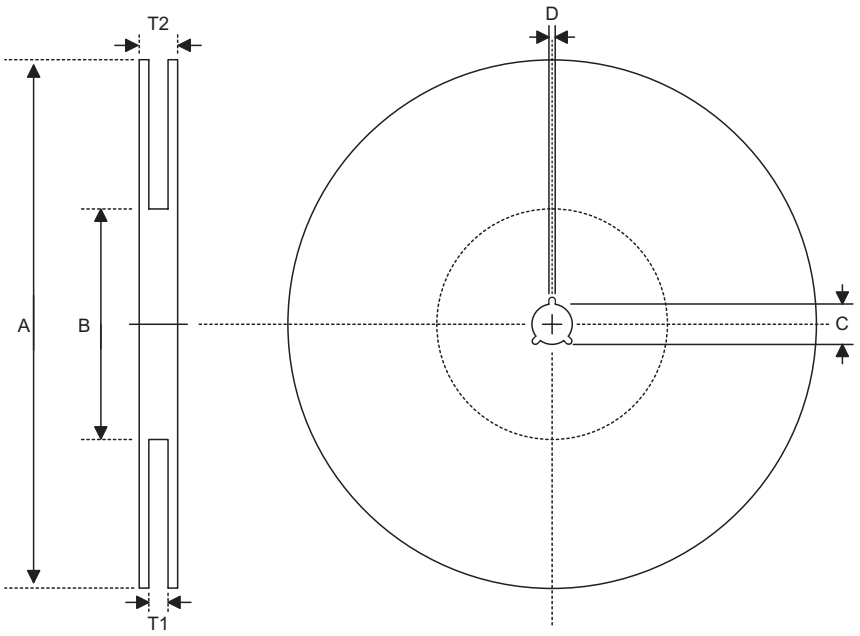
28-pin SSOP (209mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	291	—	323
B	196	—	220
C	9	—	15
C′	396	—	407
D	65	—	73
E	—	25.59	—
F	4	—	10
G	26	—	34
H	4	—	8
α	0°	—	8°

Product Tape and Reel Specifications

Reel Dimensions



SOP 20W

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13+0.5 −0.2
D	Key Slit Width	2±0.5
T1	Space Between Flange	24.8+0.3 −0.2
T2	Reel Thickness	30.2±0.2

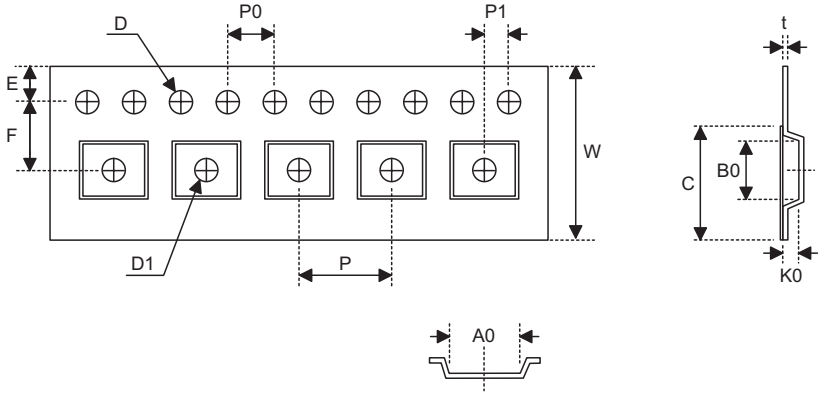
SSOP 20N (209mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13+0.5 −0.2
D	Key Slit Width	2±0.5
T1	Space Between Flange	16.8+0.3 −0.2
T2	Reel Thickness	22.2±0.2

SOP 28W (300mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13+0.5 −0.2
D	Key Slit Width	2±0.5
T1	Space Between Flange	24.8+0.3 −0.2
T2	Reel Thickness	30.2±0.2

Carrier Tape Dimensions



SOP 20W

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24+0.3 −0.1
P	Cavity Pitch	12±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.5+0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4±0.1
P1	Cavity to Perforation (Length Direction)	2±0.1
A0	Cavity Length	10.8±0.1
B0	Cavity Width	13.3±0.1
K0	Cavity Depth	3.2±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	21.3

SSOP 20N (209mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16+0.3 −0.1
P	Cavity Pitch	12±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	1.5+0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4±0.1
P1	Cavity to Perforation (Length Direction)	2±0.1
A0	Cavity Length	7.1±0.1
B0	Cavity Width	7.2±0.1
K0	Cavity Depth	2±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	13.3

SOP 28W (300mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24±0.3
P	Cavity Pitch	12±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.5+0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4±0.1
P1	Cavity to Perforation (Length Direction)	2±0.1
A0	Cavity Length	10.85±0.1
B0	Cavity Width	18.34±0.1
K0	Cavity Depth	2.97±0.1
t	Carrier Tape Thickness	0.35±0.01
C	Cover Tape Width	21.3

Holtek Semiconductor Inc. (Headquarters)
No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189
http://www.holtek.com.tw

Holtek Semiconductor Inc. (Taipei Sales Office)
4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan
Tel: 886-2-2655-7070
Fax: 886-2-2655-7373
Fax: 886-2-2655-7383 (International sales hotline)

Holtek Semiconductor Inc. (Shanghai Sales Office)
7th Floor, Building 2, No.889, Yi Shan Rd., Shanghai, China 200233
Tel: 021-6485-5560
Fax: 021-6485-0313
http://www.holtek.com.cn

Holtek Semiconductor Inc. (Shenzhen Sales Office)
43F, SEG Plaza, Shen Nan Zhong Road, Shenzhen, China 518031
Tel: 0755-8346-5589
Fax: 0755-8346-5590
ISDN: 0755-8346-5591

Holtek Semiconductor Inc. (Beijing Sales Office)
Suite 1721, Jinyu Tower, A129 West Xuan Wu Men Street, Xicheng District, Beijing, China 100031
Tel: 010-6641-0030, 6641-7751, 6641-7752
Fax: 010-6641-0125

Holmate Semiconductor, Inc. (North America Sales Office)
46712 Fremont Blvd., Fremont, CA 94538
Tel: 510-252-9880
Fax: 510-252-9885
http://www.holmate.com