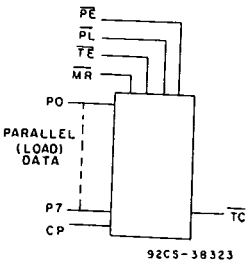
CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

File Number **1596**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Stage Synchronous Down Counters

40102 - 2-Decade BCD Type
40103 - 8-Bit Binary Type

Type Features:

- *Synchronous or asynchronous preset*
- *Cascadable in synchronous or ripple mode*

The RCA-CD54/74HC40102, 40103 and CD54/74HCT40102, 40103 are manufactured with high speed silicon gate technology and consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The 40102 is configured as two cascaded 4-bit BCD counters, and the 40103 contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the $\overline{TC}$ output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK (CP). Counting is inhibited when the $\overline{TE}$ input is high. The $\overline{TC}$ output goes low when the count reaches zero if the $\overline{TE}$ input is low, and remains low for one full clock period.

When the $\overline{PE}$ input is low, data at the P0-P7 inputs are clocked into the counter on the next positive clock transition regardless of the state of the $\overline{TE}$ input. When the $\overline{PL}$ input is low, data at the P0-P7 inputs are asynchronously forced into the counter regardless of the state of the $\overline{PE}$, $\overline{TE}$, or CLOCK inputs. Input P0-P7 represent two 4-bit BCD words for the 40102 and a single 8-bit binary word for the 40103. When the MR input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the 40102 and 225_{10} for the 40103) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except $\overline{TE}$ are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

The 40102 and 40103 may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

These circuits possess the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits and can drive up to 10 LSTTL loads.

The CD54HC40102, 40103, and CD54HCT40102, 40103 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC40102, 40103 and CD74HCT40102, 40103 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC} + 0.5V$) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

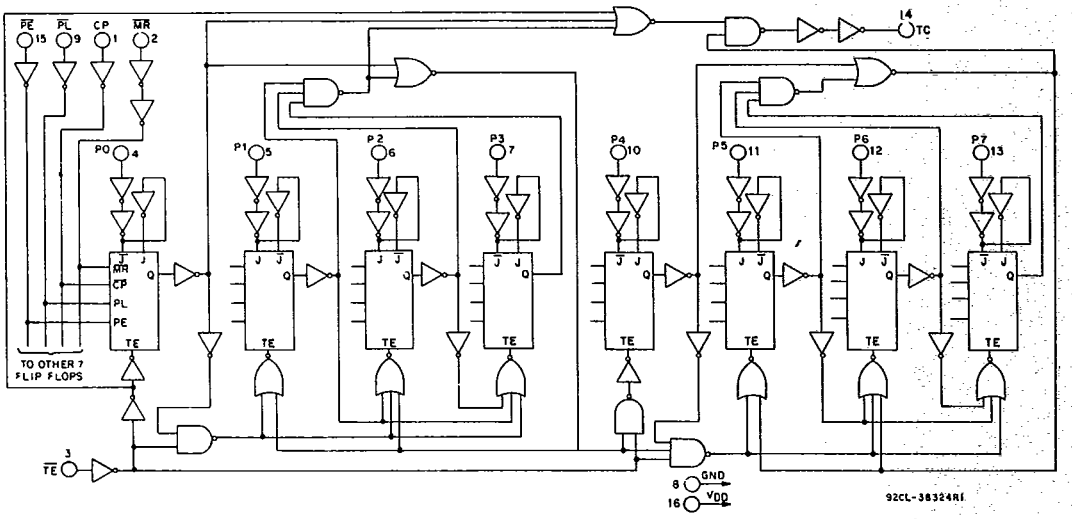


Fig. 1 - Logic diagram for the CD54/74HC/HCT40102.

TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
1	1	1	1	Synchronous	Inhibit Counter
1	1	1	0		Count Down
1	1	0	X		Preset On Next Positive Clock Transition
1	0	X	X	Asynchronously	Preset Asynchronously
0	X	X	X		Clear to Maximum Count

Notes:
1. 0 = Low Level
   1 = High Level
   X = Don't Care
2. Clock Connected to Clock Input.
3. Synchronous operation: Changes Occur on Negative-to-Positive Clock Transitions.
4. Load Inputs: 40102 BCD: MSD = P7, P6, P5, P4 (P7 is MSB)
   LSD = P3, P2, P1, P0 (P3 is MSB)
   40103 Binary: MSB = P7, LSB = P0

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

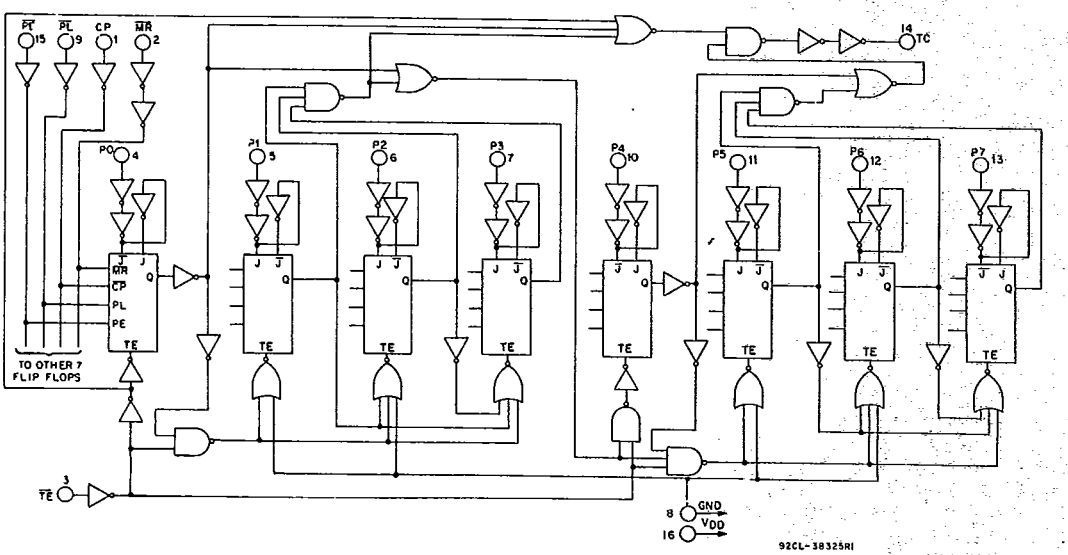
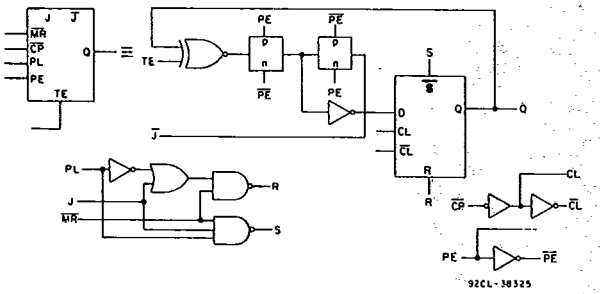


Fig. 2 - Logic diagram for the CD54/74HC/HCT40103.



Flip-Flop detail.

T-45-23-17

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC40102-40103/CD54HC40102-40103										CD74HCT40102-40103/CD54HCT40102-40103									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
P0 - P7	0.20
$\overline{TE}$, $\overline{MR}$	0.40
CP	0.60
$\overline{PE}$	0.80
$\overline{PL}$	1.35

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay CP to $\overline{TC}$ (Sync. Preset)	t_{PHL} t_{PLH}	15	25	25	ns
CP to $\overline{TC}$ (Async. Preset)	t_{PHL} t_{PLH}	15	25	26	ns
$\overline{TE}$ to $\overline{TC}$	t_{PHL} t_{PLH}	15	17	21	ns
$\overline{PL}$ to $\overline{TC}$	t_{PHL} t_{PLH}	15	23	28	ns
$\overline{MR}$ to $\overline{TC}$	t_{PHL} t_{PLH}	15	23	23	ns
CP Max. Frequency	f_{MAX}	15	25	25	MHz
Power Dissipation Capacitance*	C_{PD}	—	25	27	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + C_L V_{CC}^2 f_o$ where:
f_i = input frequency.
f_o = output frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

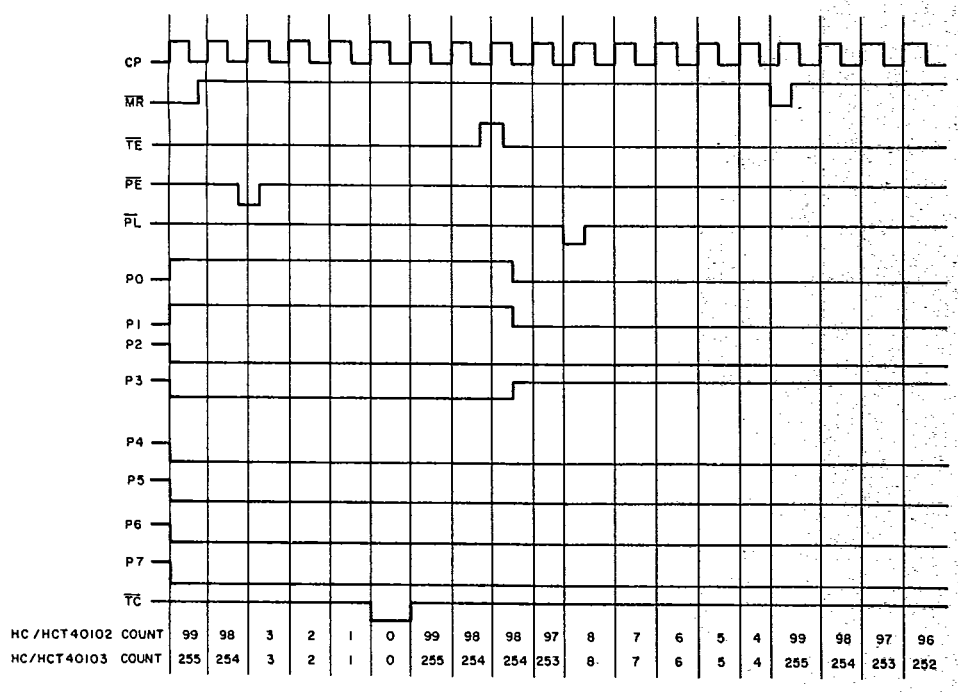


Fig. 3 - Timing diagram for HC/HCT40102 and HC/HCT40103.

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

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PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CP Pulse Width	t_W	2	165	—	—	—	205	—	—	—	250	—	—	—	ns
		4.5	33	—	35	—	41	—	44	—	50	—	53	—	
		6	28	—	—	—	35	—	—	—	43	—	—	—	
$\overline{PL}$ Pulse Width	t_W	2	125	—	—	—	155	—	—	—	190	—	—	—	ns
		4.5	25	—	43	—	31	—	54	—	38	—	65	—	
		6	21	—	—	—	26	—	—	—	32	—	—	—	
$\overline{MR}$ Pulse Width	t_W	2	125	—	—	—	135	—	—	—	190	—	—	—	ns
		4.5	25	—	35	—	31	—	44	—	38	—	53	—	
		6	21	—	—	—	26	—	—	—	32	—	—	—	
CP Max. Frequency*	$f_{CP(Max.)}$	2	3	—	—	—	2	—	—	—	2	—	—	—	MHz
		4.5	15	—	14	—	12	—	11	—	10	—	9	—	
		6	18	—	—	—	14	—	—	—	12	—	—	—	
P to CP Setup Time	t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	24	—	25	—	30	—	30	—	36	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
$\overline{PE}$ to CP Setup Time	t_{SU}	2	75	—	—	—	95	—	—	—	110	—	—	—	ns
		4.5	15	—	20	—	19	—	25	—	22	—	30	—	
		6	13	—	—	—	16	—	—	—	19	—	—	—	
$\overline{TE}$ to CP Setup Time	t_{SU}	2	150	—	—	—	190	—	—	—	225	—	—	—	ns
		4.5	30	—	40	—	38	—	50	—	45	—	60	—	
		6	26	—	—	—	33	—	—	—	38	—	—	—	
P to CP Hold Time	t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
$\overline{TE}$ to $\overline{CP}$ Hold Time	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
$\overline{MR}$ to CP Removal Time	t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
$\overline{PE}$ to $\overline{CP}$ Hold Time	t_H	2	2	—	—	—	2	—	—	—	2	—	—	—	ns
		4.5	2	—	2	—	2	—	2	—	2	—	2	—	
		6	2	—	—	—	2	—	—	—	2	—	—	—	

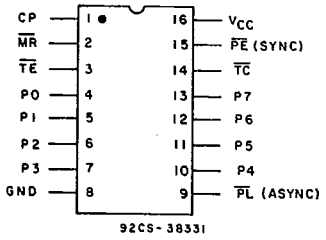
CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay CP to $\overline{TC}$ (Async Preset)	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	ns
	t_{PHL}	4.5	—	60	—	60	—	75	—	75	—	90	—	90	
		6	—	51	—	—	—	64	—	—	—	77	—	—	
CP to $\overline{TC}$ (Sync Preset)	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	ns
		4.5	—	60	—	63	—	75	—	79	—	90	—	95	
	t_{PHL}	6	—	51	—	—	—	64	—	—	—	77	—	—	
$\overline{TE}$ to $\overline{TC}$	t_{PLH}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
		4.5	—	40	—	50	—	50	—	63	—	60	—	75	
	t_{PHL}	6	—	34	—	—	—	43	—	—	—	51	—	—	
$\overline{PL}$ to $\overline{TC}$	t_{PLH}	2	—	275	—	—	—	345	—	—	—	415	—	—	ns
		4.5	—	55	—	68	—	69	—	85	—	83	—	102	
	t_{PHL}	6	—	47	—	—	—	59	—	—	—	71	—	—	
$\overline{MR}$ to $\overline{TC}$	t_{PLH}	2	—	275	—	—	—	345	—	—	—	415	—	—	ns
		4.5	—	55	—	55	—	69	—	69	—	83	—	83	
	t_{PHL}	6	—	47	—	—	—	59	—	—	—	71	—	—	
Output Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	t_{THL}	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

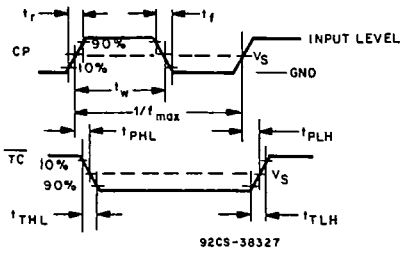
*Noncascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enables ($\overline{PE}$ or $\overline{TE}$)-to-clock SETUP TIMES, and count enables ($\overline{PE}$ or $\overline{TE}$)-to-clock HOLD TIMES determine max. clock frequency. For example, with these HC devices:

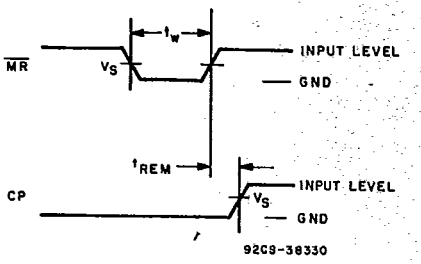
$$C_P f_{MAX} = \frac{1}{\text{CP-to-}\overline{TC}\text{ prop delay} + \overline{TE}\text{-to-CP Setup Time} + \overline{TE}\text{-to-CP Hold Time}} = \frac{1}{60+30+0} \approx 11\ \text{MHz}$$

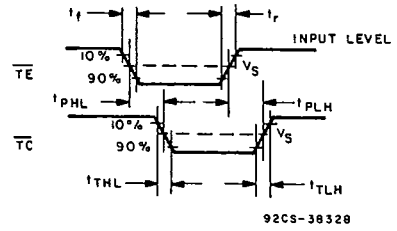


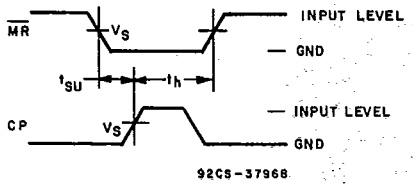
TERMINAL ASSIGNMENT

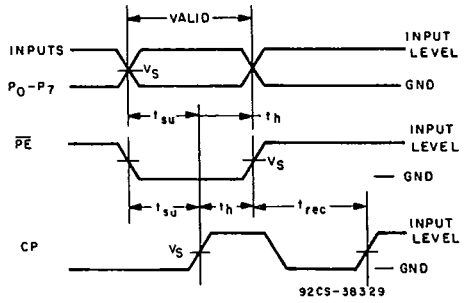
CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

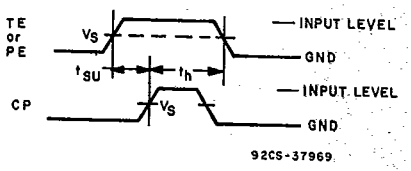












	CD54/74HC	CD54/74HCT
Input Level,	Vcc	3 V
Vs	0.5 Vcc	1.3 V

Transition times, propagation delay times, setup and hold times, and removal times.