

54ABT/74ABT646

Octal Transceivers and Registers with TRI-STATE® Outputs

General Description

The 'ABT646 consists of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{OE}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{OE}$ is Active LOW. In the isolation mode (control $\overline{OE}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Military Drawing (SMD) 5962-9457701

Ordering Code: See Section 10

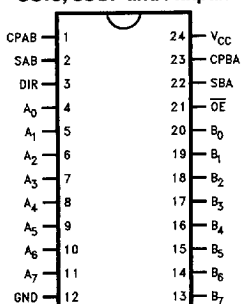
Commercial	Military	Package Number	Package Description
74ABT646CSC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54ABT646J/883	J24A	24-Lead Ceramic Dual-In-Line
74ABT646CMSA (Note 1)		MSA24	24-Lead Molded Shrink Small Outline, EIAJ Type II
	54ABT646W/883	W24C	24-Lead Cerpak
	54ABT5646E/883	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C
74ABT646CMTC (Notes 1, 2)		MTC24	24-Lead Molded Thin Shrink Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix - SCX, MSAX and MTCX.

Note 2: Contact factory for package availability.

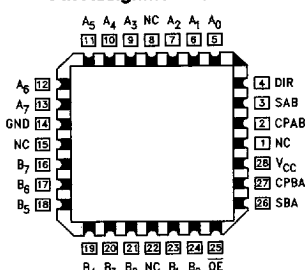
Connection Diagrams

Pin Assignment for SOIC, SSOP and Flatpak



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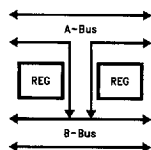
Pin Assignment for LCC



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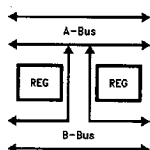
Pin Descriptions

Pin Names	Description
A ₀ –A ₇	Data Register A Inputs/ TRI-STATE Outputs
B ₀ –B ₇	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
$\overline{OE}$	Output Enable Input
DIR	Direction Control Input

Real Time Transfer
A-Bus to B-Bus

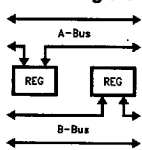
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FIGURE 1

Real Time Transfer
B-Bus to A-Bus

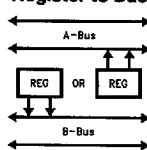
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FIGURE 2

Storage from
Bus to Register

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FIGURE 3

Transfer from
Register to Bus

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FIGURE 4

Inputs							Data I/O*		Function
OE	DIR	CPAB	CPBA	SAB	SBA		A ₀ -A ₇	B ₀ -B ₇	
H	X	H or L	H or L	X	X		Input	Input	Isolation
H	X	↗	X	X	X				Clock A _n Data into A Register
H	X	X	↗	X	X				Clock B _n Data into B Register
L	H	X	X	L	X		Input	Output	A _n to B _n —Real Time (Transparent Mode)
L	H	↗	X	L	X				Clock A _n Data into A Register
L	H	H or L	X	H	X				A Register to B _n (Stored Mode)
L	H	↗	X	H	X				Clock A _n Data into A Register and Output to B _n
L	L	X	X	X	L		Output	Input	B _n to A _n —Real Time (Transparent Mode)
L	L	X	↗	X	L				Clock B _n Data into B Register
L	L	X	H or L	X	H				B Register to A _n (Stored Mode)
L	L	X	↗	X	H				Clock B _n Data into B Register and Output to A _n

*The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

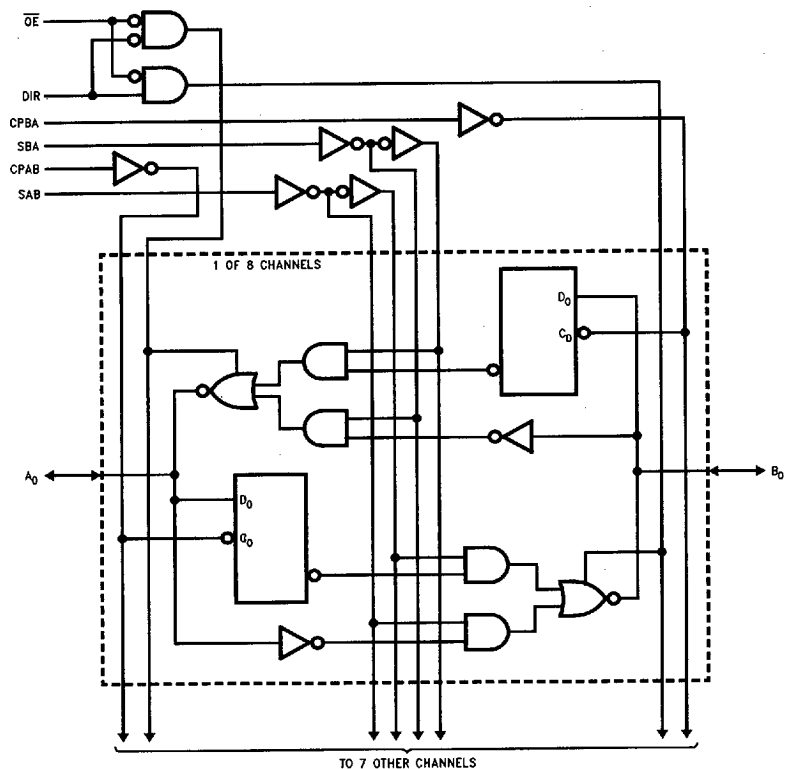
H = HIGH Voltage Level

X = Immaterial

L = LOW Voltage Level

↗ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State in the HIGH State	−0.5V to +5.5V −0.5V to V _{CC}

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT646			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage 54ABT/74ABT	2.5 2.0 2.0			V	Min	I _{OH} = −3 mA, (A _n , B _n) I _{OH} = −24 mA, (A _n , B _n) I _{OH} = −32 mA, (A _n , B _n)
V _{OL}	Output LOW Voltage 54ABT 74ABT			0.55 0.55	V	Min	I _{OL} = 48 mA, (A _n , B _n) I _{OL} = 64 mA, (A _n , B _n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I _{IH}	Input HIGH Current			5 5	μA	Max	V _{IN} = 2.7V (Non-I/O Pins) (Note 2) V _{IN} = V _{CC} (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current			−5 −5	μA	Max	V _{IN} = 0.5V (Non-I/O Pins) (Note 2) V _{IN} = 0.0V (Non-I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			50	μA	0V–5.5V	V _{OUT} = 2.7V (A _n , B _n); $\overline{OE}$ = 2.0V
I _{IL} + I _{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V _{OUT} = 0.5V (A _n , B _n); $\overline{OE}$ = 2.0V
I _{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V _{OUT} = 0V (A _n , B _n)
I _{CEx}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test			100	μA	0.0V	V _{OUT} = 5.5V (A _n , B _n); All Others GND
I _{OCH}	Power Supply Current			250	μA	Max	All Outputs HIGH
I _{OCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			50	μA	Max	Outputs TRI-STATE; All Others GND
I _{CCt}	Additional I _{CC} /Input			2.5	mA	Max	V _I = V _{CC} − 2.1V All Other Outputs at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 2)	No Load		0.18	mA/MHz	Max	Outputs Open $\overline{OE}$ and DIR = GND, Non-I/O = GND or V _{CC} (Note 1) One Bit toggling, 50% duty cycle

Note 1: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

Note 2: Guaranteed but not tested.

DC Electrical Characteristics (SOIC package) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		0.6	0.8	V	5.0	T _A = 25°C (Note 1)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-1.2	-0.9		V	5.0	T _A = 25°C (Note 1)
V _{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T _A = 25°C (Note 3)
V _{IHD}	Minimum High Level Dynamic Input Voltage	2.2	1.8		V	5.0	T _A = 25°C (Note 2)
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	0.5	V	5.0	T _A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n - 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP package): See Section 2 for Waveforms

Symbol	Parameter	74ABT			54ABT		74ABT		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 4.5V-5.5V C _L = 50 pF		T _A = -40°C to +85°C V _{CC} = 4.5V-5.5V C _L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Max Clock Frequency	200			200		200		MHz	
t _{PLH}	Propagation Delay	1.7	3.0	4.9	2.2	8.8	1.7	4.9	ns	2-3, 5
t _{PHL}	Clock to Bus	1.7	3.4	4.9	1.7	8.8	1.7	4.9	ns	2-3, 5
t _{PLH}	Propagation Delay	1.5	2.6	4.5	1.5	7.9	1.5	4.5	ns	2-3, 5
t _{PHL}	Bus to Bus	1.5	3.0	4.5	1.5	7.9	1.5	4.5	ns	2-3, 5
t _{PLH}	Propagation Delay	1.5	3.0	5.0	1.5	8.1	1.5	5.0	ns	2-3, 5
t _{PHL}	SBA or SAB to A _n to B _n	1.5	3.4	5.0	1.5	8.9	1.5	5.0	ns	2-3, 5
t _{PZH}	Enable Time	1.5	3.2	5.5	1.0	7.3	1.5	5.5	ns	2-4
t _{PZL}	OE to A _n or B _n	1.5	3.5	5.5	1.9	8.8	1.5	5.5	ns	2-4
t _{PHZ}	Disable Time	1.5	3.7	6.0	1.5	9.3	1.5	6.0	ns	2-4
t _{PLZ}	OE to A _n or B _n	1.5	3.2	6.0	1.5	9.3	1.5	6.0	ns	2-4
t _{PZH}	Enable Time	1.5	3.4	5.5	1.0	7.7	1.5	5.5	ns	2-4
t _{PZL}	DIR to A _n or B _n	1.5	3.7	5.5	2.2	9.5	1.5	5.5	ns	2-4
t _{PHZ}	Disable Time	1.5	3.8	6.0	1.5	8.7	1.5	6.0	ns	2-4
t _{PLZ}	DIR to A _n or B _n	1.5	3.2	6.0	1.5	9.2	1.5	6.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT		54ABT		74ABT		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max	Min	Max	Min	Max		
$t_{S(H)}$ $t_{S(L)}$	Setup Time, HIGH or LOW Bus to Clock	1.5		1.5	3.0	1.5		ns	2-6
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW Bus to Clock	1.0		1.0	1.0	1.0		ns	2-6
$t_W(H)$ $t_W(L)$	Pulse Width, HIGH or LOW	3.0		3.0	4.0	3.0		ns	2-3

Extended AC Electrical Characteristics (SOIC package): See Section 2 for Waveforms

Symbol	Parameter	74ABT		74ABT		74ABT		Units	Fig. No.
		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 4)		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 250\text{ pF}$ 1 Output Switching (Note 5)		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 6)			
		Min	Max	Min	Max	Min	Max		
		Min	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay	1.5	5.5	2.0	7.5	2.5	10.0	ns	2-3, 5
t _{PHL}	Clock to Bus	1.5	5.5	2.0	7.5	2.5	10.0		
t _{PLH}	Propagation Delay	1.5	6.0	2.0	7.0	2.5	9.5	ns	2-3, 5
t _{PHL}	Bus to Bus	1.5	6.0	2.0	7.0	2.5	9.5		
t _{PLH}	Propagation Delay	1.5	6.0	2.0	7.5	2.5	10.0	ns	2-3, 5
t _{PHL}	SBA or SAB to A _n or B _n	1.5	6.0	2.0	7.5	2.5	10.0		
t _{PZH}	Output Enable Time	1.5	6.0	2.0	8.0	2.5	10.5	ns	2-4
t _{PZL}	$\overline{OE}_n$ or DIR to A _n or B _n	1.5	6.0	2.0	8.0	2.5	10.5		
t _{PHZ}	Output Disable Time	1.5	6.0	(Note 7)		(Note 7)		ns	2-4
t _{PLZ}	$\overline{OE}_n$ or DIR to A _n or B _n	1.5	6.0						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500 Ω , 250 pF) on the output and has been excluded from the datasheet.

Skew (SOIC package): See Section 2 for Waveforms

Symbol	Parameter	74ABT	74ABT	Units	Fig. No.
		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 3)	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 4)		
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.5	ns	2-13
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	2.0	ns	2-13
t_{PS} (Note 5)	Duty Cycle LH-HL Skew	2.0	4.0		2-14
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	4.0	ns	2-17
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	4.5	ns	2-20

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

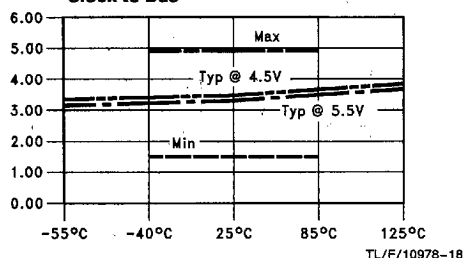
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

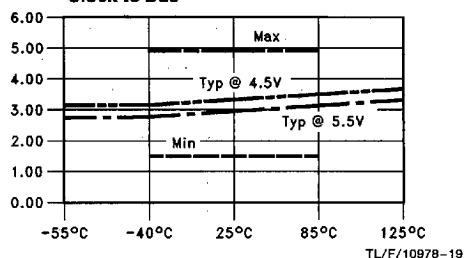
Symbol	Parameter	Typ	Units	Conditions $T_A = 25^{\circ}\text{C}$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$ (non I/O pins)
$C_{I/O}$ (Note 1)	Output Capacitance	11	pF	$V_{CC} = 5.0\text{V}$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency, $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.

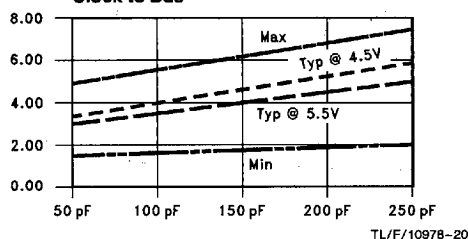
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Clock to Bus



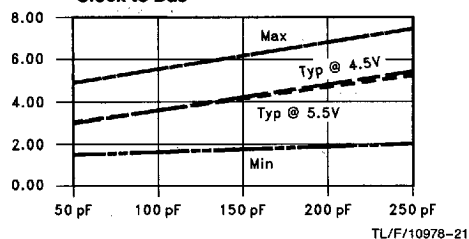
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Clock to Bus



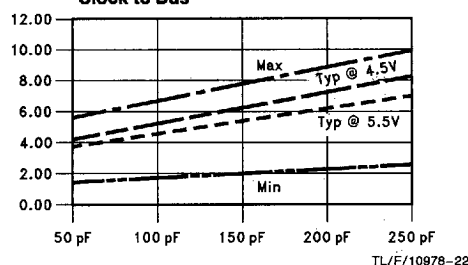
t_{PLH} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$
 Clock to Bus



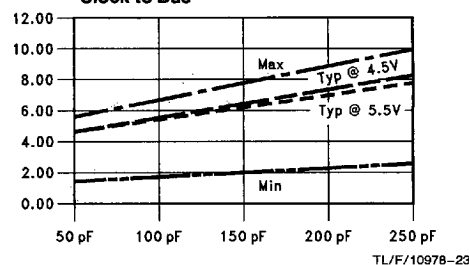
t_{PHL} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$
 Clock to Bus



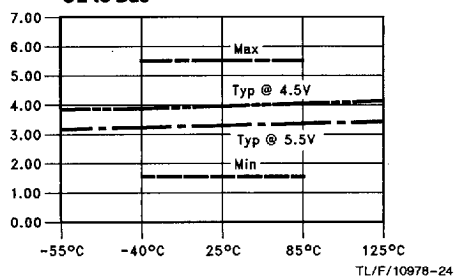
t_{PLH} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$
 Clock to Bus



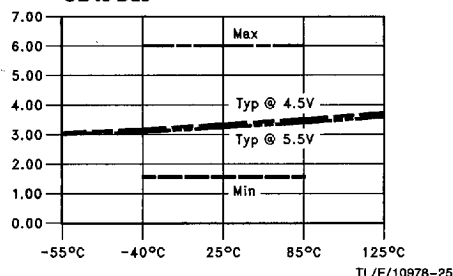
t_{PHL} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$
 Clock to Bus



t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 OE to Bus

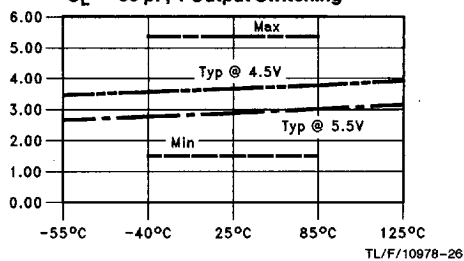


t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 OE to Bus

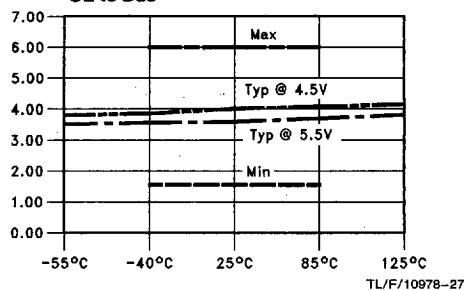


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

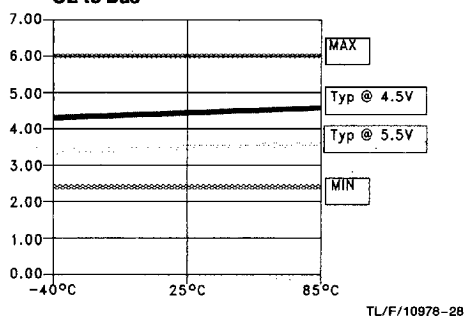
t_{pZH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



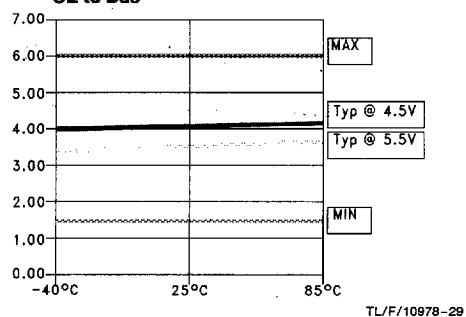
t_{pHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 $\overline{OE}$ to Bus



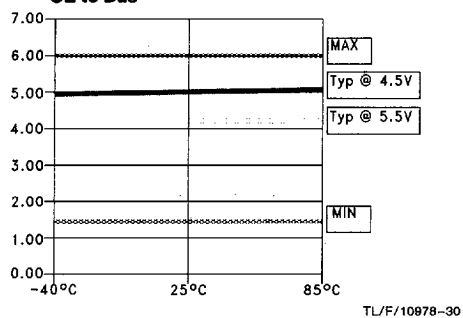
t_{pZH} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 $\overline{OE}$ to Bus



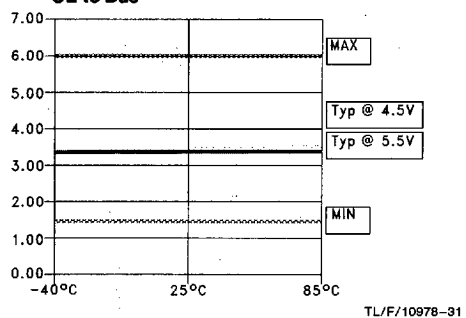
t_{pHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 $\overline{OE}$ to Bus



t_{pZL} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 $\overline{OE}$ to Bus

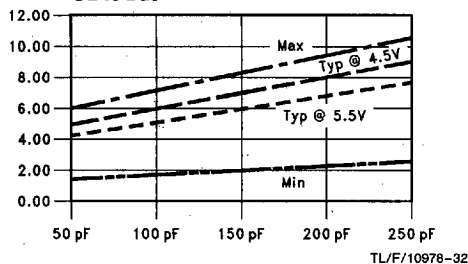


t_{pLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 $\overline{OE}$ to Bus

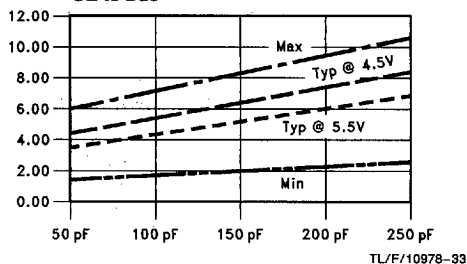


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

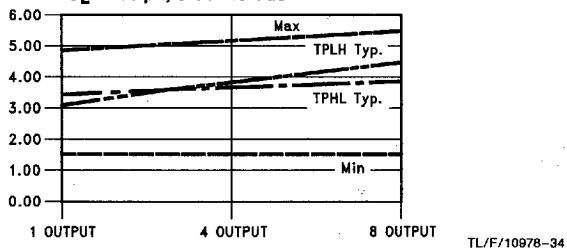
t_{pZL} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$
OE to Bus



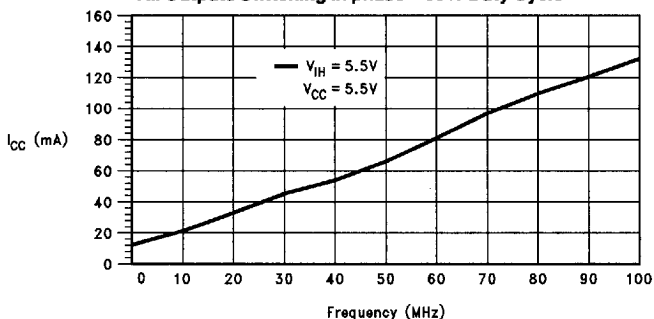
t_{pZH} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$
OE to Bus



t_{pLH} and t_{pHL} vs Number Output Switching
 $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$
 $C_L = 50\text{ pF}$, Clock to Bus

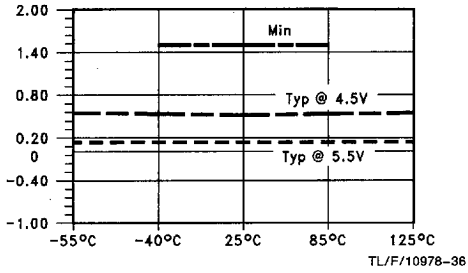


I_{CC} vs Frequency, Average,
 $T_A = 25^\circ\text{C}$, $V_{CC} = 5.5\text{V}$
All Outputs Unloaded/Unterminated;
All Outputs Switching in phase @50% Duty Cycle

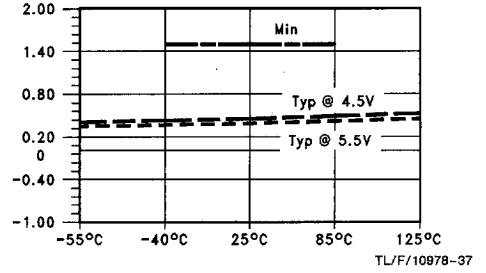


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

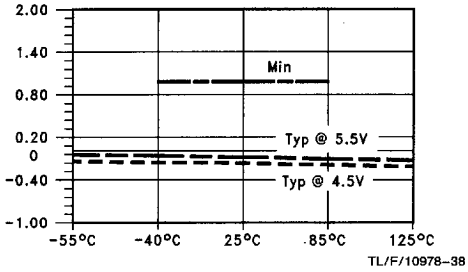
t_{SET} LOW vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Bus to Clock



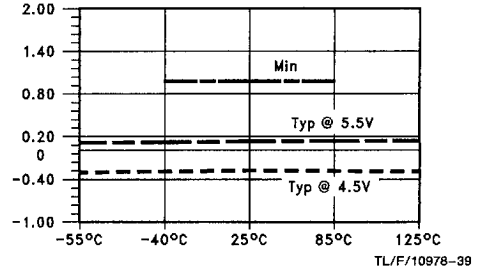
t_{SET} HIGH vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Bus to Clock



t_{HOLD} LOW vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Bus to Clock



t_{HOLD} HIGH vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Bus to Clock



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.