

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI Analog ICs

M65533FP

3ch 8-bit 80MHz A/D Converters

General Description

The M65533FP is a CMOS **3ch 8-bit 80MHz** analog-to-digital converter by sub-ranging architecture for high speed video processing. It can be realized 80MHz operation by using 2 ADCs in parallel. And it has **PLL circuit** generate a stable clock locked to sync signal. It is a type of "AC" connection with internal clamp circuit and variable input range.

Features

- 3ch 8-bit high speed A-D converters
- Maximum conversion rate
- Analog input Level
- Digital input
- Digital output
- Low power dissipation
- Package

- Small input capacitance
- Built-in Reference Voltage
- Built-in Clamp circuit

80 MSPS(min.)
1.0V(Typ) : 0.5 -1.5 V
TTL compatible [$V_{inH}=1.4V$]
 $V_{oH}=0.7 \times V_{cc}$, $V_{oL}=0.3 \times V_{cc}$ [$I_o=4mA$]
700mW [$CL=10pF$]
80 pin QFP package, 0.80mm lead pitch
[PKG size(without lead) =14mm x 20mm]
10 pF
 $V_{ref(+)}=1.5V+150/-330mV(*)$ $V_{ref(-)}=0.5V$
 $V_{clamp}=0.5V+/-250mV(*)$
(*):Controllable by IIC BUS

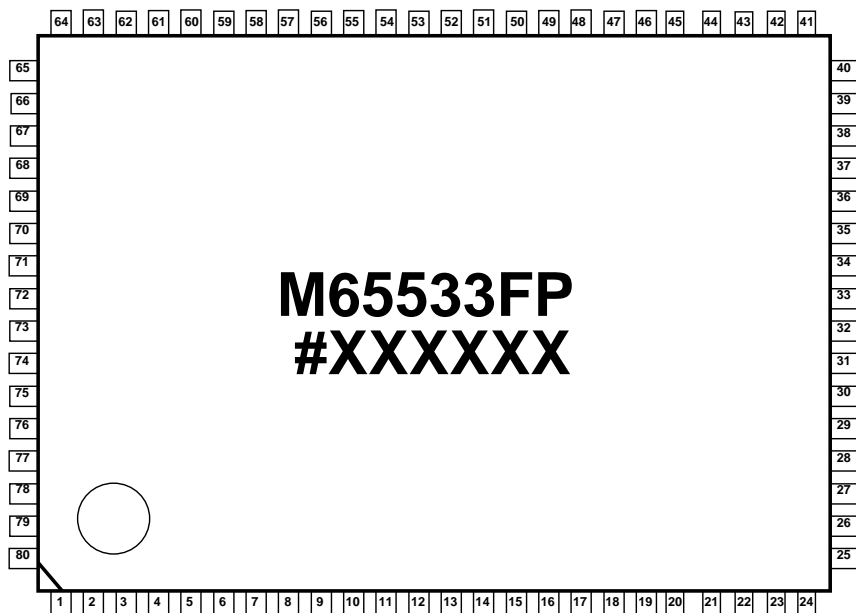
Applications

- LCD monitor
- High speed video processing

Recommended Operating Condition

- Supply voltage range (typ.=3.3V) 3.15 to 3.45 V
- Supply voltage range (typ.=5.0V) 4.75 to 5.25 V for 5V I/F only

Pin configuration(Top View) Shown on next page



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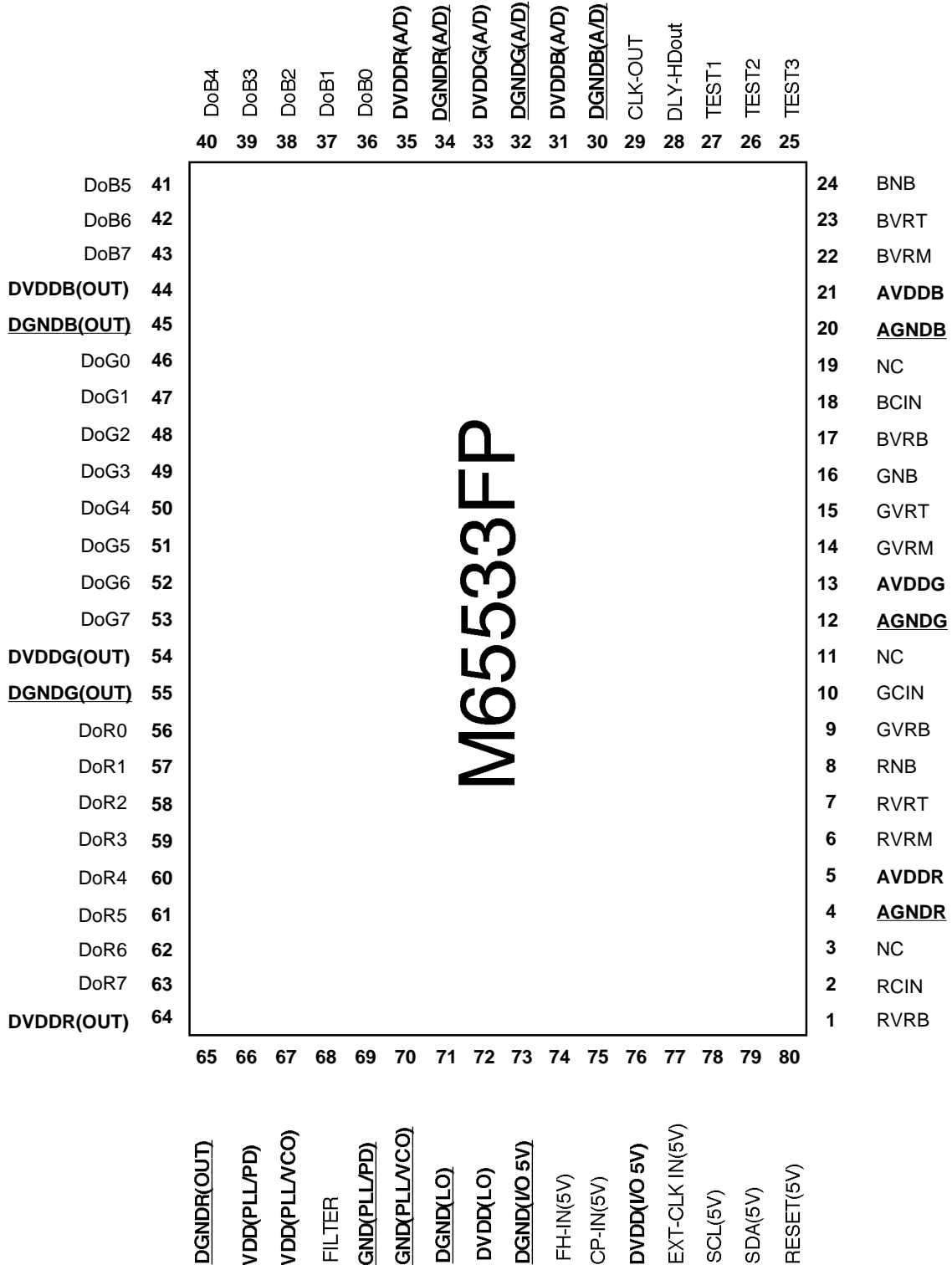
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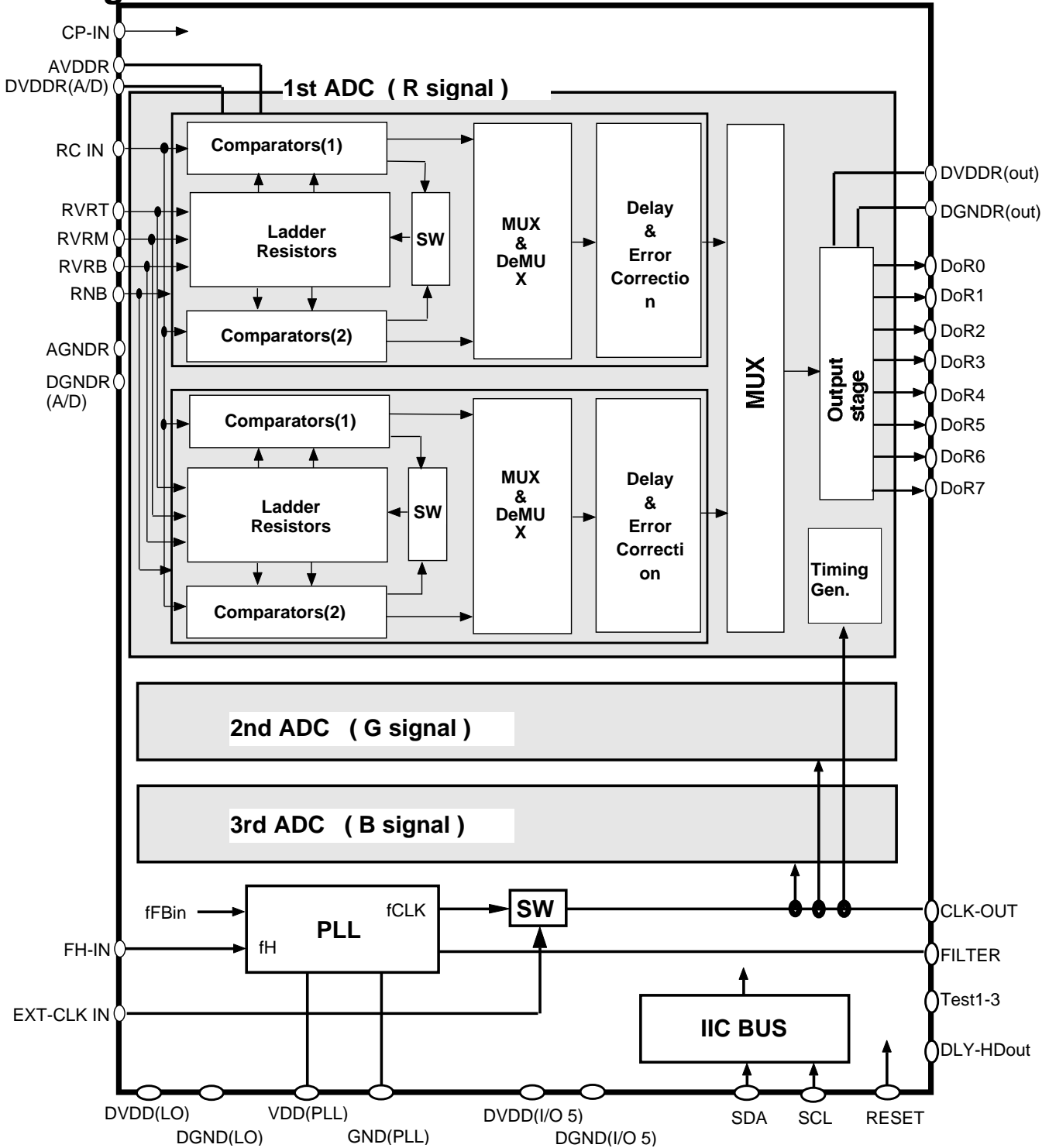
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Pin Configuration



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Block Diagram



(note) Pins for ADC is described for only R signal

Absolute Maximum Ratings (Ta = 25°C, unless otherwise noted.)

Symbol	Parameter	Condition	Ratings	Unit
DVdd	Digital Supply Voltage		0 to 4.0	V
AVdd	Analog Supply Voltage		0 to 4.0	V
Vdd(I/O)	I/O Supply Voltage		0 to 6.0	V
V _{ID}	Digital Input Voltage		0 to 4.0	V
I _{OUT}	Analog Output Current		-30 to 0	mA
P _d	Power Dissipation		1600	mW
T _{opr}	Operating Temperature		0 to +70	°C
T _{stg}	Storage Temperature		-40 to +150	°C

In current measurement, (+) and (-) is corresponding to an inflow and an outflow current, respectively.

Recommended Operating Conditions (Ta = 25°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{dd}	Supply Voltage	3.15	3.30	3.45	V
V _{dd(I/O)}	Supply Voltage(I/O)	4.75	5.0	5.25	V
V _{IH}	Digital Input Voltage (High)	2.4	-	V _{dd}	V
V _{IL}	Digital Input Voltage (Low)	0	-	0.8	V
t _{WH}	Clock Pulse Width (High)	6.25	-	-	ns
t _{WL}	Clock Pulse Width (Low)	6.25	-	-	ns
t _{su}	Set-up Time	5	-	-	ns
t _h	Hold Time	5	-	-	ns

Electrical Characteristics

(Ta = 25°C, AVdd = DVdd = 3.30V, unless otherwise noted.)

(1) Overall

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
A _{Idd} (AD R/G/B)	AD(R/G/B) Analog Supply Current	For R/G/B signal		tof		mA
D _{Idd} (AD R/G/G)	AD(R/G/G) Digital Supply Current	For R/G/B signal		tof		mA
D _{Idd} (I/O R/G/G)	I/O block Supply Current	For R/G/B signal		tof		mA
D _{Idd} (PLL)	PLL block Supply Current			tof		mA
D _{Idd} (LO)	Logic block Supply Current			tof		mA
D _{Idd} (I/O 5)	5V I/O block Supply Current			tof		mA

(2) ADC Block

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bits
V _{dd}	Supply Voltage		3.15	3.30	3.45	V
NL	Integral Nonlinearity	V _{ref} (+)=1.5V, V _{ref} (-)=0.5V			± 1.0	LSB
DNL	Differential Nonlinearity	V _{ref} (+)=1.5V, V _{ref} (-)=0.5V			± 1.0	LSB
V _{OH}	Digital output Voltage "H"		0.7xV _{dd}		V _{dd}	V
V _{OL}	Digital output Voltage "L"		0		0.3xV _{dd}	V
V _{inA}	Analog input range		0.67	1.00	1.15	V _{p-p}
C _{in}	Input Capacitance			10		pF
f _{CLK}	Max. Conversion Rate		80			MHz
V _{ref} (+)	Reference Voltage "High"	Changeable by IIC (16mV step)	1.17	1.5	1.65	V
V _{ref} (M)	Reference Voltage "Middle"		0.84	1.0	1.07	V
V _{ref} (-)	Reference Voltage "Low"			0.5		V
R _{ref}	Reference Resistor			120		Ohms
B.W	Input Bandwidth	-3dB input frequency	70			MHz
tp _{dLH}	Output delay time(L->H)			110	160	ns
tp _{dHL}	Output delay time(H->L)			110	160	ns
t _r	Output rise time			tof		ns
t _f	Output fall time			tof		ns
V _{clamp}	Clamp Voltage	Changeable by IIC (16mV step)	0.25	0.5	0.73	V

(3) PLL Block

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
f _H	Horizontal frequency		10	60	100	KHz
f _{VCO}	VCO frequency		20		80	MHz
j _{PLL}	maximum jitter			0.5	1.0	ns
D.R(PLL)	PLL Divider Ratio	from 800 by 1 step	800		1376	-

Pin Description -1

No connection.
 It is grounded during actual use.

Pin No.	Pin Name	I/O	Function	From or To
31,33,35	DVDDX(A/D)		Digital Power supply (R/G/B signal)	3.3V
5,13,21	AVDDX(A/D)		Analog Power supply (R/G/B signal)	3.3V
44,54,64	DVDDX(OUT)		I/O Power supply (R/G/B signal)	3.3V
66,67	VDD(PLL)		PLL Power supply	3.3V
30,32,34	DGNDX (A/D)		Digital ground (R/G/B signal)	GND
4,12,20	AGNDX (A/D)		Analog ground (R/G/B signal)	GND
45,55,65	DGNDX(OUT)		I/O ground (R/G/B signal)	GND
69,70	GND(PLL)		PLL ground	GND
2,10,18	XCIN	I	R/G/B signal Clamp Input	From LPF
7,15,23	XVRT		Reference Voltage(+) Input (R/G/B signal)	Bypass capacitor
6,14,22	XVRM		Reference Voltage(M) Input (R/G/B signal)	Bypass capacitor
1,9,17	XVRB		Reference Voltage(-) Input (R/G/B signal)	Bypass capacitor
8,16,24	XNB		ADC operating current setting BIAS	Bypass capacitor
36 - 43 46 - 53 56 - 63	DoX<7:0>	O	Digital Output (R/G/B signal)	To Logic LSI
74	FH-IN	I	H Sync Input	From Sync Sep. LSI
68	FILTER		PLL filter	(R+C)//C
29	CLK-OUT	O	Clock output	To Logic LSI
79	SDA	I/O	IIC Data Input/Output	From MCU
78	SCL	I/O	IIC CLK Input	From MCU
80	RESET	I	Reset signal Input	To Vdd
77	EXT-CLK IN	I	External Clock input	From PLL LSI
25,26,27	Test<1-3 >	I/O	Test terminal	

Table of Power-down Function(SubAdd=00h, D2-D0) Setting by IIC BUS

Digital input code	Power-down function
"HHH"	power-down
"LLL"	normal operation

Default

Only Clamp=>"HLL"
 Only PLL=>"LHL"
 Only ADC=>"LLH"

Table of CP Function (SubAdd=11h, D0) Setting by IIC BUS





CP signal	CP function	CP signal	Digital input code	CP Polarity
"H"	Clamping		D0="H"	Inversed
"L"	Hold state		D0="L"	Not-inversed

Table of Hsync Function(SubAdd=17h, D0) Setting by IIC BUS

Digital input code	Hsync function
 D0="H"	Inversed
 D0="L"	Not-inversed

Default

Table of CLK output Function(SubAdd=13h, D0) Setting by IIC BUS

Digital input code	CLK output function
D0="H"	Inversed (180°)
D0="L"	Not-inversed (0°)

Default

Table of Internal/External CLK(SubAdd=16h, D5) Setting by IIC BUS

Digital input code	CLK output function
D5="H"	External
D5="L"	Internal

Default

Table of Digital Output R/G/B < 7 : 0 > Function Setting by IIC BUS

Output "HZ" is available at D1="H" of SubAdd=18h "L"=default

Analog input voltage	Digital output code								Note
	7 MSB	6	5	4	3	2	1	0 LSB	
1.500V	1	1	1	1	1	1	1	1	
1.496V	1	1	1	1	1	1	1	0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
1.000V	1	0	0	0	0	0	0	0	
0.996V	0	1	1	1	1	1	1	1	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0.504V	0	0	0	0	0	0	0	1	
0.500V	0	0	0	0	0	0	0	0	

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**Table of Delay adjustment(SubAdd=16h, D3-D0)
for External CLK (SubAdd=16h, D5="H")**

Setting by IIC BUS

Digital input code				CLK Delayed Adjustment	
D3	D2	D1	D0		
1	1	1	1	75ns	
1	1	1	0	70ns	
⋮	⋮	⋮	⋮	⋮	
1	0	0	0	40ns	
0	1	1	1	35ns	
⋮	⋮	⋮	⋮	⋮	
0	0	0	1	5ns	
0	0	0	0	0ns	

Default

**Table of Vref(+) Voltage adjustment
(SubAdd=0Bh, D4-D0:R 0Ch, D4-D0:G 0Dh, D4-D0:B)**

Setting by IIC BUS

Digital input code					Vref(+) adjustment	Note
D4	D3	D2	D1	D0		
1	1	1	1	1	40LSB	1.5+0.157V
1	1	1	1	0	36LSB	
⋮	⋮	⋮	⋮	⋮	⋮	
1	0	1	0	1	0LSB	1.5-0V
⋮	⋮	⋮	⋮	⋮	⋮	
1	0	0	0	0	-20LSB	
0	1	1	1	1	-24LSB	
⋮	⋮	⋮	⋮	⋮	⋮	
0	0	0	0	1	-80LSB	
0	0	0	0	0	-84LSB	1.5-0.329V

Default

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Table of Clamp level adjustment

Setting by IIC BUS

(SubAdd=0Eh, D4-D0:R 0Fh, D4-D0:G 10h, D4-D0:B)

Digital input code					Delay adjustment level	Note
D4	D3	D2	D1	D0		
1	1	1	1	1	60LSB	0.5V+235mV
1	1	1	1	0	56LSB	
⋮	⋮	⋮	⋮	⋮	⋮	
1	0	0	0	0	0LSB	0.5V-0mV
0	1	1	1	1	-4LSB	
⋮	⋮	⋮	⋮	⋮	⋮	
0	0	0	0	1	-60LSB	
0	0	0	0	0	-64LSB	0.5V-251mV

Default

Table of CLK output Phase (SubAdd=12h, D4 -D0)

Setting by IIC BUS

Digital input code					CLK output phase
D4	D3	D2	D1	D0	
1	1	1	1	1	division into 32 of 1 period
1	1	1	1	0	
⋮	⋮	⋮	⋮	⋮	
1	0	0	0	0	
0	1	1	1	1	
⋮	⋮	⋮	⋮	⋮	
0	0	0	0	1	
0	0	0	0	0	$0 + 0 * 360/32$

Default

Table of CLK output Phase Function (SubAdd=12h,D5)

Setting by IIC BUS

Digital input code	CLK output Phase Function
D5="H"	OFF
D5="L"	ON

Table of CLK's Pol. for A/D (SubAdd=12h,D6)

Setting by IIC BUS

Digital input code	CLK's Pol.
D6="H"	NEGA
D6="L"	POSI

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**Table of PLL divider adjustment
(SubAdd=14h,A6-A0 15h,A3-A0)**

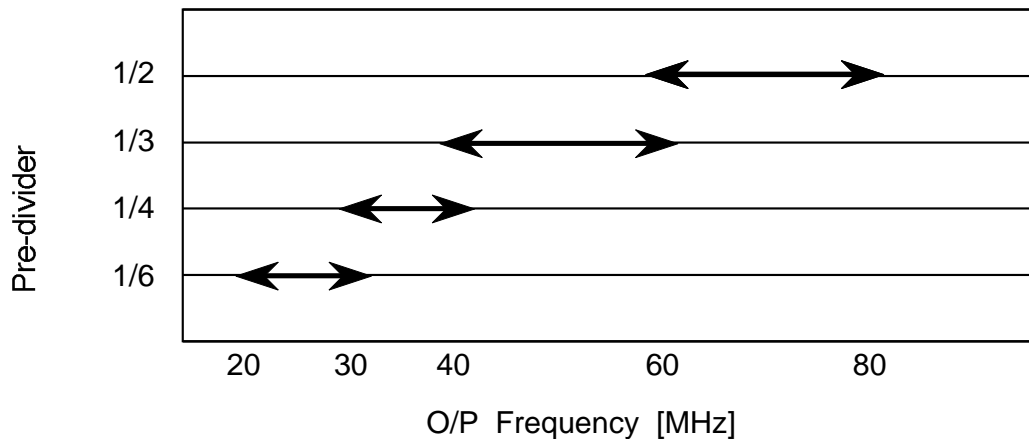
Setting by IIC BUS

Digital input code											Divider adjustment
14h						15h					
A6	A5	A4	A3	A2	A1	A0	A3	A2	A1	A0	
1	0	1	0	1	1	0	0	0	0	0	fH x 1376
1	0	1	0	1	0	1	1	1	1	1	fH x 1375
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
1	0	0	0	0	0	0	0	0	0	0	fH x 1024
0	1	1	1	1	1	1	1	1	1	1	fH x 1023
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0	1	1	0	0	1	0	0	0	0	1	fH x 801
0	1	1	0	0	1	0	0	0	0	0	fH x 800

**Table of PLL divider adjustment
(SubAdd=15h,A6-A5)**

Setting by IIC BUS

Digital input code	PLL Pre-divider adjustment
D6,5="1 1"	1/6
D6,5="1 0"	1/4
D6,5="0 1"	1/3
D6,5="0 0"	1/2



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Table of Reset Function (pin 80)

Reset signal	Reset function
"L"	Reset
"H"	normal operation

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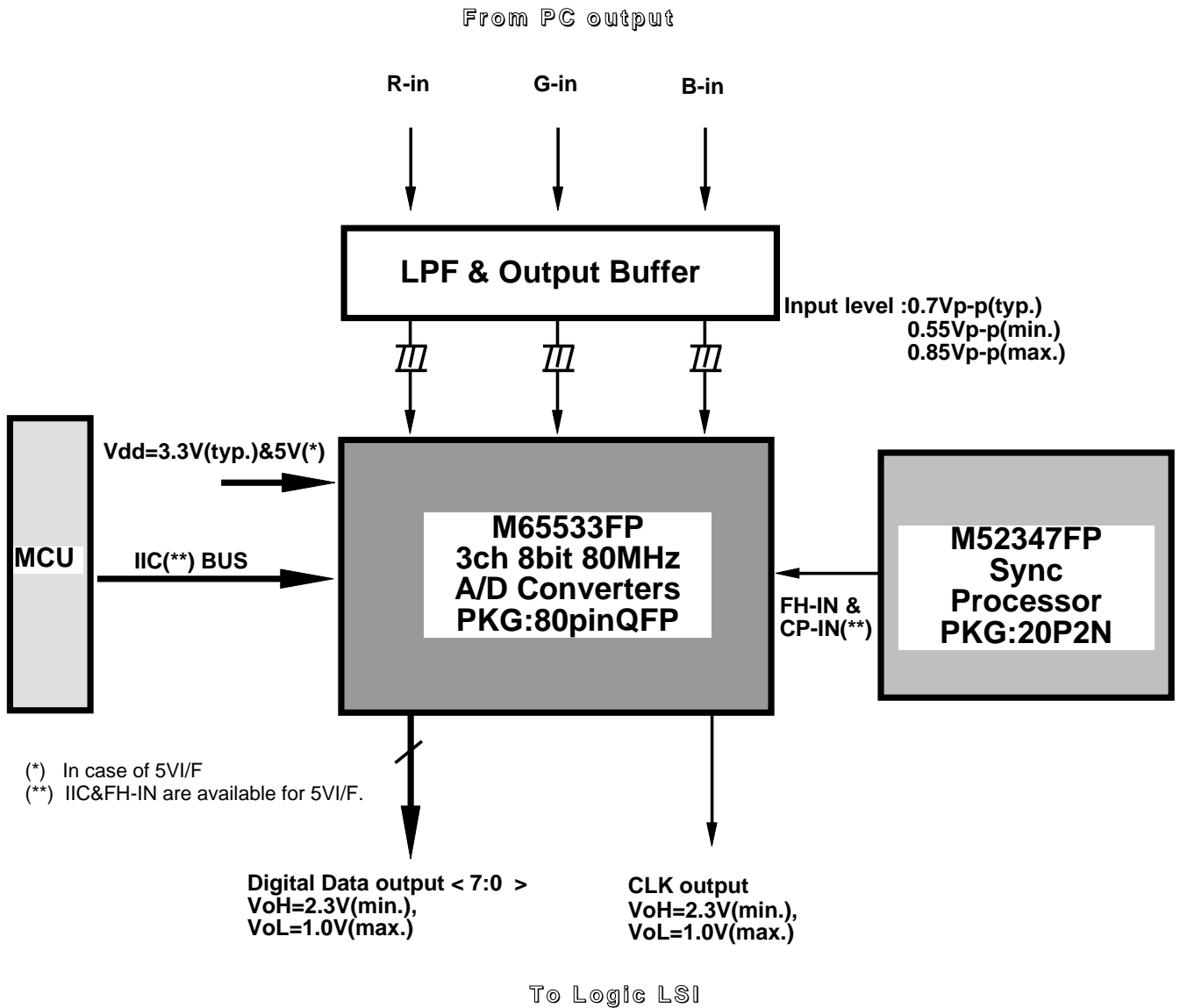
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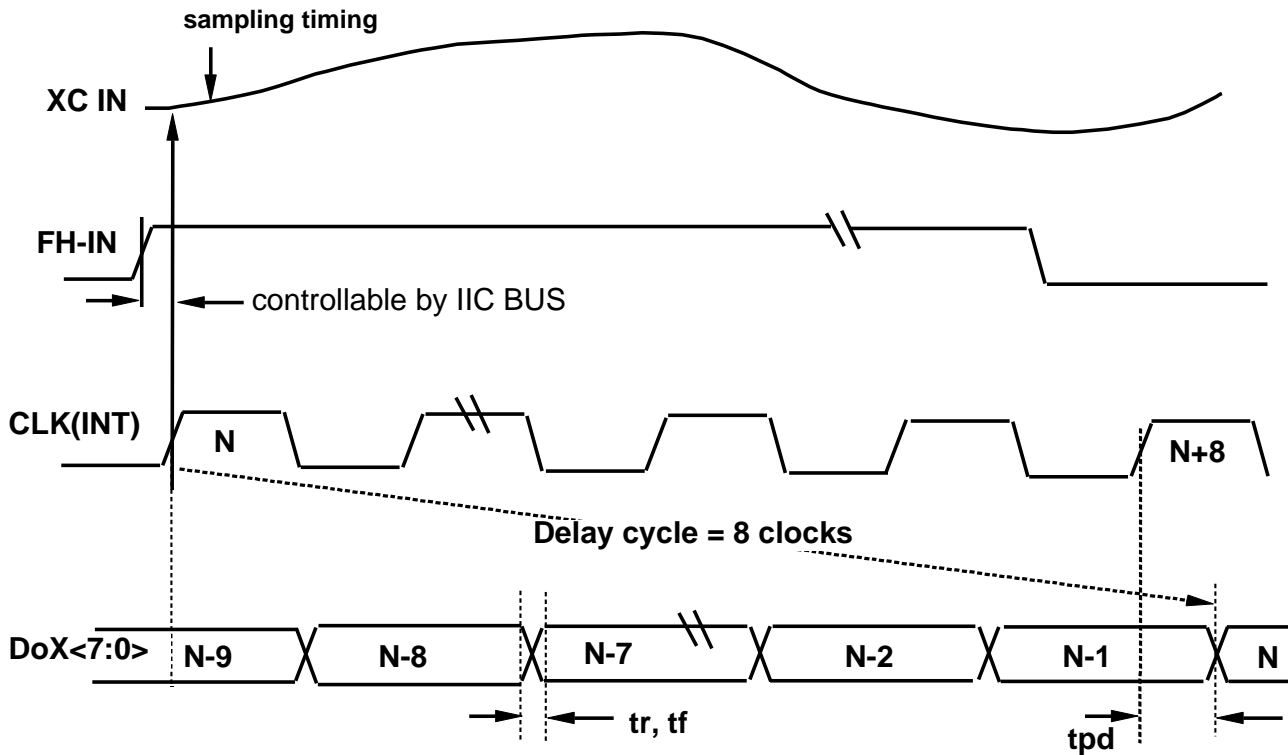
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Application Examples



Analog Input / Digital Output Timing Diagram



Notes to the operation

1. Both a ground and a supply planes in a PCB should be as wide as possible for reducing a parasitic inductance and resistance. Especially, for the better performance, the analog plane needs to be much wider.
2. A tantalum or electrolytic capacitor of 10 μ F or more and a ceramic capacitor of 0.01 μ F are tied together, which are connected between a digital supply and ground, also between a analog supply and ground. These capacitors should be placed as close as possible to the IC. They work as bypass capacitors for preventing a degradation in the performance by a supply voltage fluctuation caused by digital signals including a clock and digital inputs and so on.
3. The analog output should be isolated as much as possible from a clock and digital inputs, thus minimizing decoupling and interactive noise.

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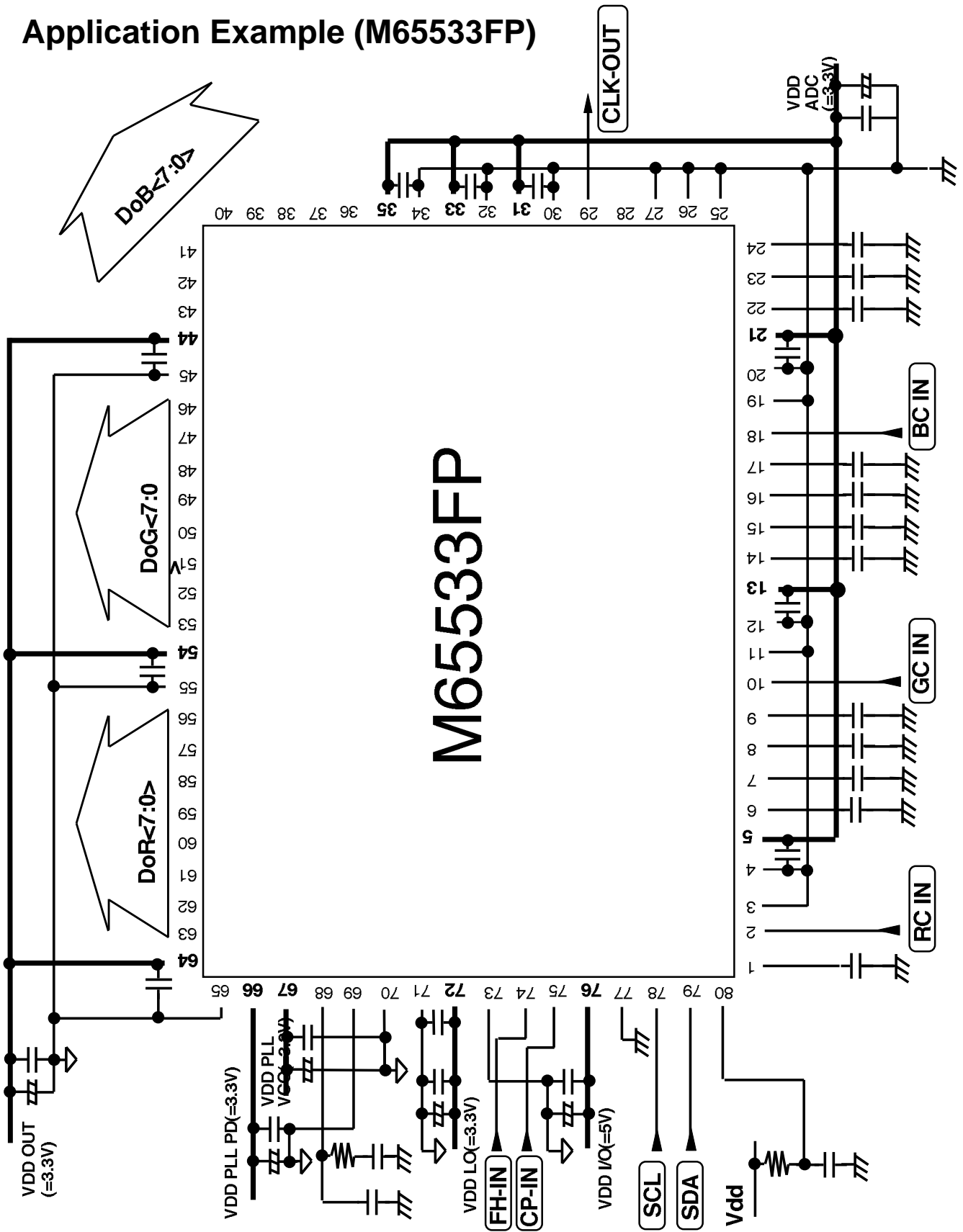
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Application Example (M65533FP)

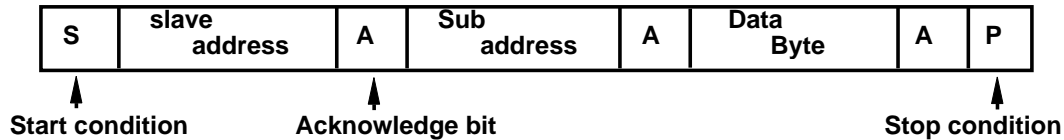


M65533FP IIC-BUS CONTROL TABLE

(1) Slave address :

A6 A5 A4 A3 A2 A1 A0 R/W
 1 0 0 1 1 1 0 0 (=9Ch)

(2) Salve address format :
 read



(3) Sub address byte and Data byte format :
 read

Block	No.	Functions	Bit	Sub Add	Data byte							
					D7	D6	D5	D4	D3	D2	D1	D0
Total	1	Power-down	3	00h	0					A02	A01	A00
ADC	2	Vref(+) Vol (R)	5	0Bh	0			A04	A03	A02	A01	A00
	3	Vref(+) Vol (G)	5	0Ch	0			A04	A03	A02	A01	A00
	4	Vref(+) Vol (B)	5	0Dh	0			A04	A03	A02	A01	A00
	5	Clamp Vol (R)	5	0Eh	0			A04	A03	A02	A01	A00
	6	Clamp Vol (G)	5	0Fh	0			A04	A03	A02	A01	A00
	7	Clamp Vol (B)	5	10h	0			A04	A03	A02	A01	A00
CLK /PLL	8	Clamp-in Pol	1	11h	0							A00
	9	CLK Phase	7	12h	0	A06	A05	A04	A03	A02	A01	A00
	10	CLKOUT Pol	1	13h	0							A00
	11	PLL upper	7	14h	0	A06	A05	A04	A03	A02	A01	A00
	12	PLL lower & Divider	6	15h	0	A06	A05		A03	A02	A01	A00
	13	INT/EXT CLK	5	16h	0		A05		A03	A02	A01	A00
	14	H_Sync Pol	2	17h	0							A00
	15	ADC Output	1	18h	0						A01	
<p>(Note) Blanks should not be defined. Because it may be used for test mode or function check.</p>												