Ordering number : EN7868

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA75676VA — IF Signal Processor (VIF+SIF) for TV and VCR Products

Overview

The LA75676VA is a VIF/SIF IC that supports NTSC intercarrier reception and adopts a semi-adjustment-free design. It is provided in the SSOP24 (225mil, 0.5mm lead pitch) package, which is appropriate for miniature 2-in-1 tuner products. In the VIF block, it adopts a design that uses AFT adjustment to obviate the need for VCO adjustment, and thus can simplify the adjustment steps required in end product manufacturing. It uses a PLL technique for FM detection. It features the 5V supply voltage appropriate for multimedia products. In addition, it achieves superb audio quality by incorporating a buzz canceller that suppresses Nyquist buzzing.

Functions

- VIF block: VIF amplifier, buzz canceller, PLL detector, IF AGC, RF AGC, AFT, and an equalizer amplifier
- SIF block: Limiter amplifier, PLL FM detector

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Circuit voltage	V13, V17		V_{CC}	V
Circuit current	I6		-3	mA
	I10		-10	mA
	I24		-2	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C * Mounted on a board	600	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

* When mounted on a 114.3×76.1×1.6mm^3 glass epoxy board.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5	V
Operating supply voltage range	V_{CC} op		4.5 to 5.5	V

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Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, fp = 45.75MHz

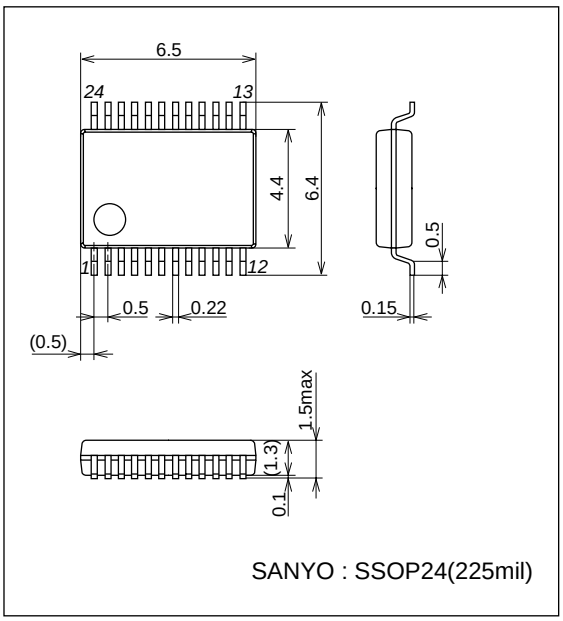
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[VIF Block]						
Circuit current	I5		33	41	49	mA
Maximum RF AGC voltage	V14H		V_{CC}-0.5	V_{CC}		V
Minimum RF AGC voltage	V14L			0	0.5	V
Input sensitivity	Vi	S1 = OFF	32	38	44	dBμV
AGC range	GR		58	63		dB
Maximum allowable input	Vi max		95	100		dBμV
Video output voltage (no input)	V6		3.5	3.8	4.1	V
Sync signal tip voltage	V6tip		0.9	1.2	1.5	V
Video output level	V_O		1.7	2	2.3	Vp-p
Black noise threshold voltage	VBTH		0.5	0.8	1.1	V
Black noise clamp voltage	VBCL		1.6	1.9	2.2	V
Video signal-to-noise ratio	S/N		48	52		dB
C-S beating	IC-S		38	43		dB
Frequency characteristics	fc	6MHz	-3	-1.5		dB
Differential gain	DG			3	6.5	%
Differential phase	DP			3	5	°C
AFT voltage (no signal)	V13		2.0	2.5	3.0	V
Maximum AFT voltage	V13H		4.0	4.4	5.0	V
Minimum AFT voltage	V13L			0.18	1.0	V
AFT detection sensitivity	Sf		28	40	52	mV/kHz
VIF input resistance	Ri	45.75MHz		1.5		kΩ
VIF input capacitance	Ci	45.75MHz		3		pF
APC pull-in range (U)	fpu		1.3	2.0		MHz
APC pull-in range (L)	fpl			-2.0	-1.4	MHz
AFT tolerance frequency 1	dfa 1		-150	0	+150	kHz
VCO 1 maximum range (U)	dfu		1.5	2.0		MHz
VCO 1 maximum range (L)	dfl			-2.0	-1.5	MHz
VCO control sensitivity	B		1.3	2.7	5.4	kHz/mV
[SIF BLOCK]						
Limiting sensitivity	Vli (lim)		39	45	51	dBμV
FM detection output voltage*	V_O (FM)	4.5MHz ±25kHz	400	520	660	mVrms
AMR	AMR		50	60		dB
Total harmonic distortion	THD			0.3	0.8	%
SIF signal-to-noise ratio	S/N (FM)		59	64		dB
4.5MHz output level	Vsout	SIF IN 80dBμV	87	94	101	dBμV

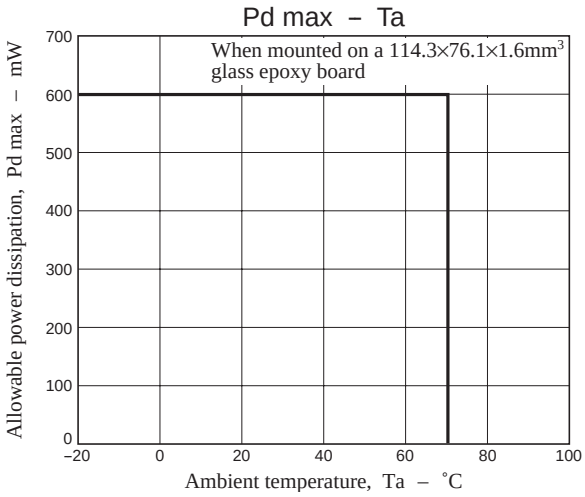
* : If a wider FM detection output dynamic range is required, insert a resistor and capacitor in series between pin 23 and ground to adjust the level.

Package Dimensions

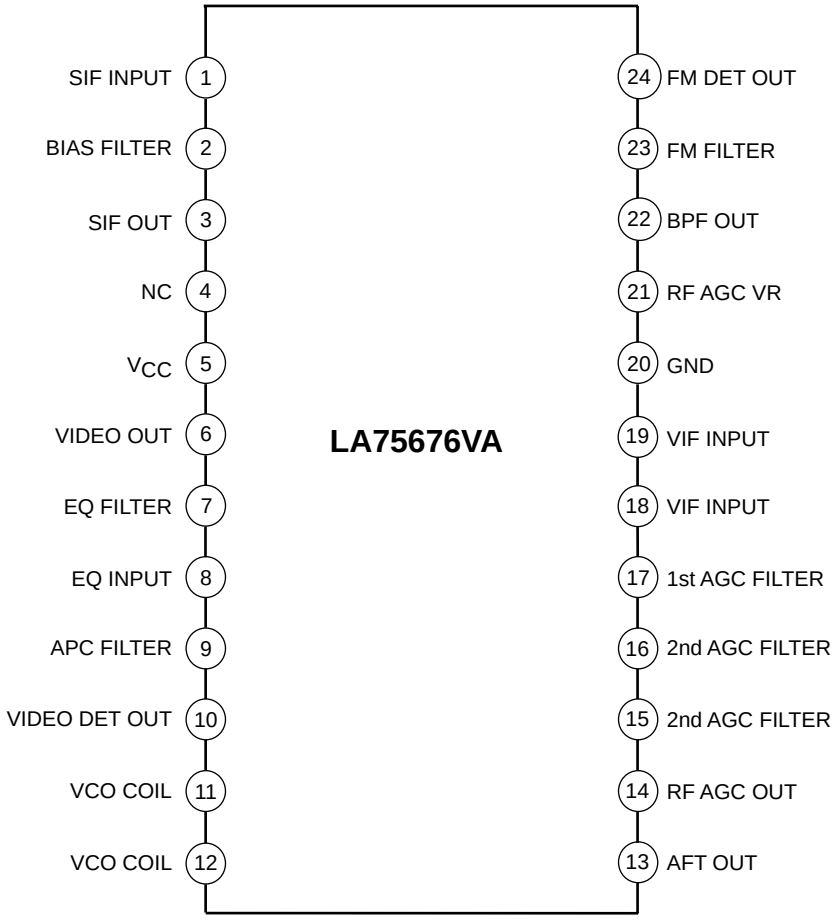
unit : mm (typ)

3287

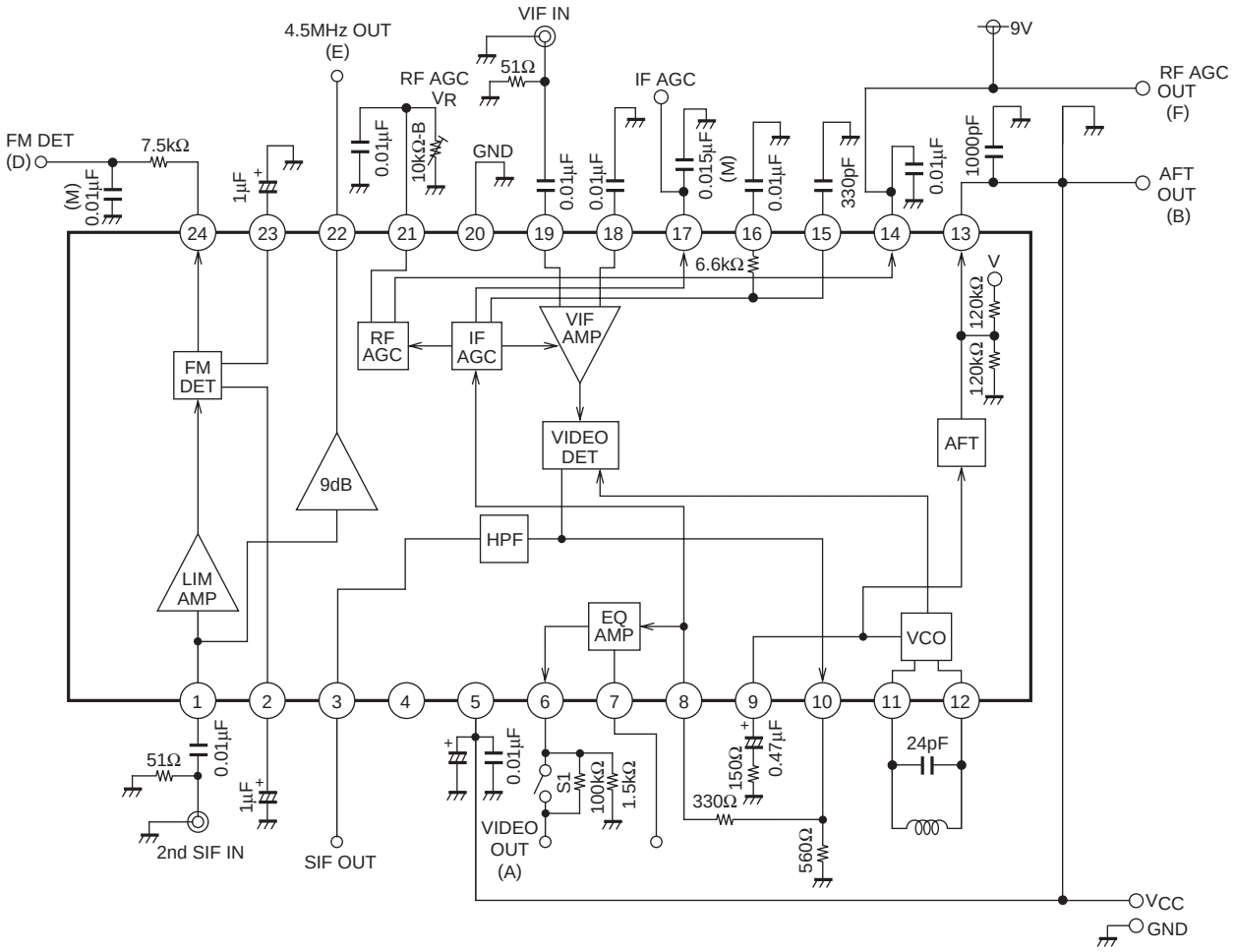




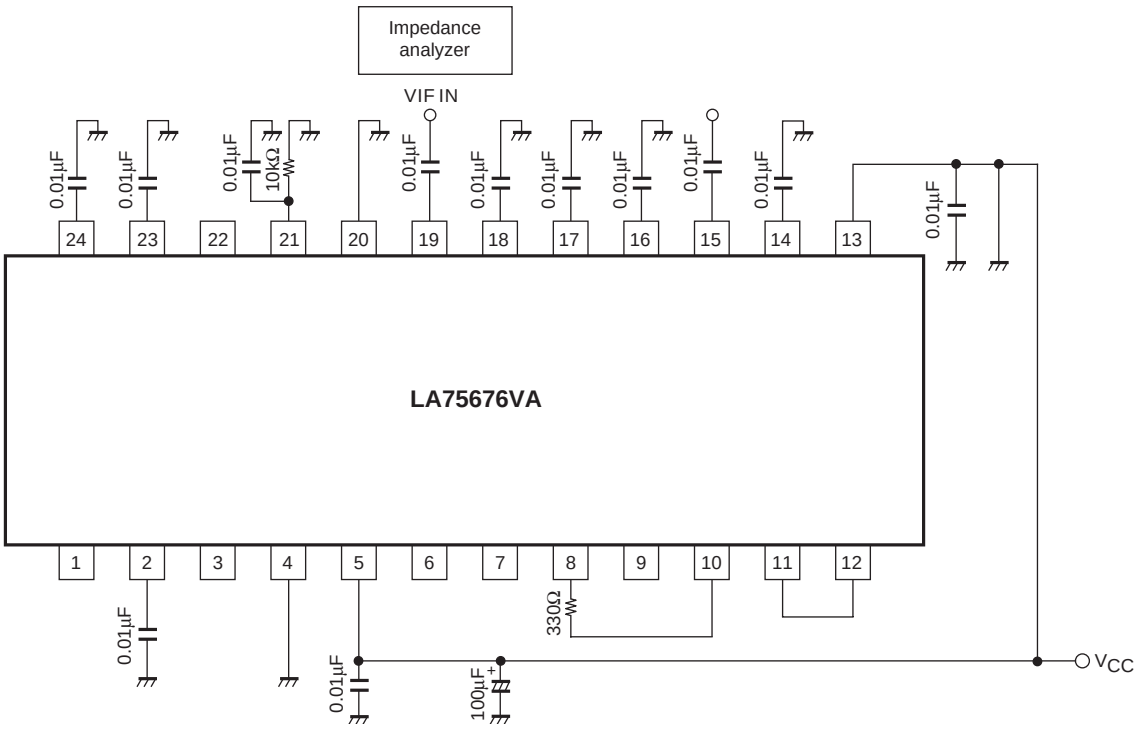
Pin Assignment



Block Diagram and AC Characteristics Test Circuit



Test Circuit (Input inpedance)



Test Conditions

V1. Circuit current • • • • [15]

1. Internal AGC
2. Input a 45.75MHz, 10mVrms, CW signal to the VIF input pin.
3. RF AGC Vr maximum
4. Connect a current meter to V_{CC} and measure the current flowing into the IC.

V2, V3. Maximum RF AGC voltage, minimum RF AGC voltage • • • • [V9H, V9L]

1. Internal AGC
2. Input a 45.75MHz, 10mVrms, CW signal to the VIF input pin.
3. Vary the RF AGC Vr and, at the maximum resistance, measure the maximum RF AGC voltage. (F)
4. Vary the RF AGC Vr and, at the minimum resistance, measure the maximum RF AGC voltage. (F)

V4. Input sensitivity • • • • [Vi]

1. Internal AGC
2. fp = 45.75MHz, 400Hz 40% AM (VIF input)
3. Set S1 to the off position and pass the input through a 100kΩ resistor.
4. Measure the VIF input level such that the 400Hz detection output level at test point A becomes 0.64Vp-p.

V5. AGC range • • • • [GR]

1. External AGC. Apply the V_{CC} voltage to the IF AGC input (pin 17).
2. With the same conditions as used for V4, measure the VIF input level such that the detection output level becomes 0.64Vp-p. • • • Vi1
3. $GR = 20\log \frac{Vi1}{Vi}$ dB

V6. Maximum allowable input • • • • [Vi max]

1. Internal AGC
2. fp = 45.75MHz, 15kHz 78% AM (VIF input)
3. Measure the VIF input level such that the detection output level at test point A is ±1dB of the video output (Vo).

V7. Video output voltage (no input) • • • • [V6]

1. External AGC. Apply the V_{CC} voltage to the IF AGC input (pin 17).
2. Measure the video output (A) DC voltage.

V8. Sync signal tip voltage • • • • [V6tip]

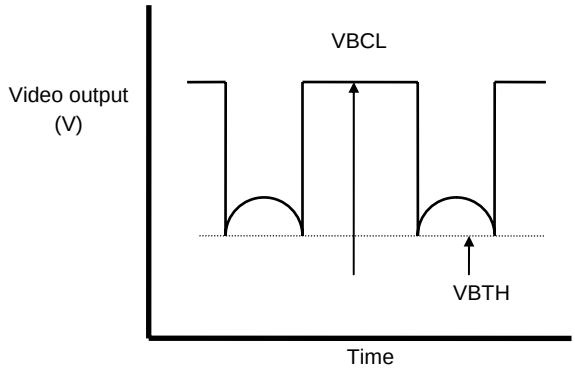
1. Internal AGC
2. Input a 45.75MHz, 10mVrms, CW signal to the VIF input pin.
3. Measure the video output (A) DC voltage.

V9. Video output level • • • • [Vo]

1. Internal AGC
2. fp = 45.75MHz, 15kHz 78% AM
   Vi = 10mVrms (VIF input)
3. Measure the wave height of the detection output level at test point A. (Vp-p)

V10, V11. Black noise threshold and clamp voltages • • • • [VBTH, VBCL]

1. Apply a DC voltage to the external AGC IF input (pin 17) and vary that voltage.
2. fp = 45.75MHz, 400Hz, 40% AM, 10mVrms (VIF input)
3. Vary the IF AGC (pin 17) voltage so that the noise canceller operates.
   Measure VBTH and VBCL at test point A.

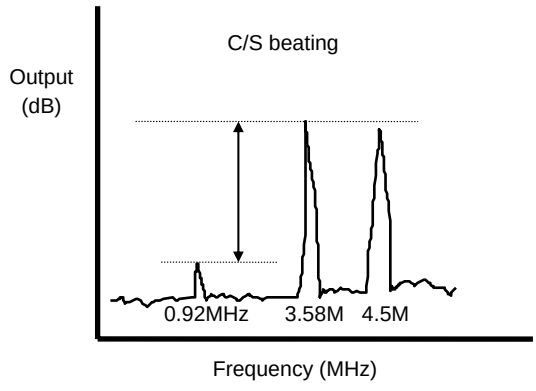


V12. Video signal-to-noise ratio • • • • [S/N]

1. Internal AGC
2. fp = 45.75MHz, CW, 10mVrms (VIF input)
3. Measure the noise voltage as an RMS level at test point A after passing through a 10kHz to 4MHz bandpass filter.
   This is the noise voltage (N).
4. $S/N = 20\log \frac{\text{Video component (Vp-p)}}{\text{Noise voltage (Vrms)}} = 20\log \frac{1.12\text{Vp-p}}{\text{Noise voltage}} = \text{(dB)}$

V13. C/S beating • • • • [ICS]

1. Apply a DC voltage to the external AGC IF input (pin 17) and vary that voltage.
2. fp = 45.75MHz, CW ; 10mVrms
   fc = 42.17MHz, CW ; 10mVrms - 10dB
   fs = 41.25MHz, CW ; 10mVrms - 10dB
3. Vary the IF AGC (pin 17) voltage to adjust the output level at test point A to be 1.3Vp-p.
4. Measure the difference in level between the 3.58MHz and the 0.92MHz components at test point A.



V14. Frequency characteristics • • • • [fc]

1. Apply a DC voltage to the external AGC IF input (pin 17) and vary that voltage.
2. SG1 : 45.75MHz, CW, 10mVrms
   SG2 : from 45.65MHz to 39.75MHz, CW, 2mVrms
   Add SG1 and SG2 using a T pad, adjust the signal generator levels to those listed above, and apply the result to VIF IN.
3. First, set the SG2 frequency to 45.65MHz.
   Next, adjust the IF AGC voltage (pin 17) so that the output level at test point A becomes 0.5Vp-p. • • V1
4. Set the SG2 frequency to 39.75MHz and measure the output level. • • V2
5. Perform the following calculation.

$$fc = 20\log\frac{V2}{V1}\,(dB)$$

V15, V16. Differential gain and differential phase • • • • [DG, DP]

1. Internal AGC
2. fp = 45.75MHz, APL 50%, 87.5% video signal, Vi = 10mVrms
3. Measure DG and DP at test point A.

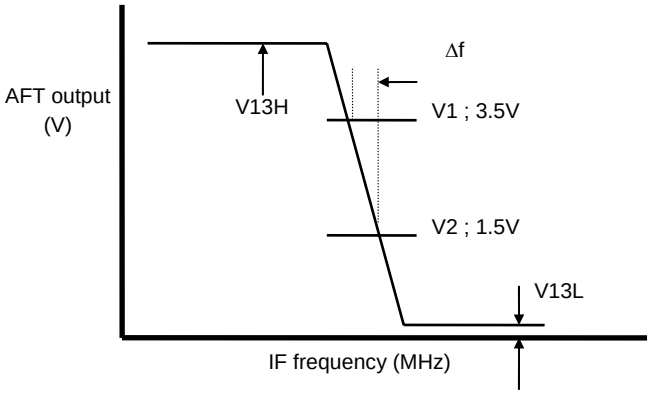
V17. AFT voltage (no signal) • • • • V13

1. Internal AGC
2. Measure the DC voltage on the AFT output (B).

V18, V19, V20. Maximum AFT voltage, minimum AFT voltage, AFT detection sensitivity • • • • [V13H, V13L, Sf]

1. Internal AGC
2. fp = 45.75MHz, ±1.5MHz sweep, 10mVrms (VIF input)
3. Record the maximum voltage as V13H and the minimum voltage as V13L.
4. Measure the frequency shift for the change in voltage at test point B from V1 to V2. • • Δf

$$Sf = \frac{2000\ (mV)}{\Delta f\ (kHz)}\ mV/kHz$$



V21, V22. VIF input resistance, input capacitance • • • • [Ri, Ci]

1. Use an impedance analyzer to measure Ri and Ci in the input impedance test circuit.

V23, V24. APC pull-in range • • • • [fpu, fpl]

1. Internal AGC
2. fp = 39MHz to 51MHz, CW : 10mVrms
3. Vary the signal generator from fp = 45.75MHz towards higher frequencies until PLL lock is lost.
   Note : PLL lock is lost at the point beating is output at test point A.
4. Lower the signal generator frequency until the PLL locks again. (f1)
5. Lower the signal generator frequency until PLL lock is lost.
6. Raise the signal generator frequency until the PLL locks again. (f2)
7. Perform the following calculations.
   fpu = f1 - 45.75MHz
   fpl = f2 - 45.75MHz

V25. AFT tolerance frequency 1 • • • • [ΔFa1]

1. Internal AGC
2. SG1 : Vary this frequency from 43.75MHz to 47.75MHz, CW, 10mVrms
3. Vary the SG1 frequency so that the AFT output (test point B) becomes 2.5V.
   Record the SG1 frequency at that point as f1.
4. External AGC (Adjust V17.)
5. Apply 5V to the IF AGC (pin 17), pick up the VCO oscillator frequency from ground or some other point, and measure that frequency. f2
6. Perform the following calculation.
   AFT tolerance frequency 1 ΔFa1 = f2 - f1 (kHz)

V26, V27. VCO maximum range (U, L) • • • • [dfu, dfl]

1. External AGC. Apply the V_{CC} voltage to the IF AGC (pin 17).
2. Pick up the VCO oscillator frequency from the video output (A), ground, or some other point and adjust the VCO coil so that frequency becomes 45.75MHz.
3. Apply 1V to the APC pin (pin 9) and let fl be the frequency at that time.
   Similarly, apply 5V and let fu be the frequency at that time.
   dfu = fu - 45.75MHz
   dfl = fl - 45.75MHz

V28. VCO control sensitivity • • • • [β]

1. External AGC. Apply the V_{CC} voltage to the IF AGC (pin 17).
2. Pick up the VCO oscillator frequency from the video output (A), ground, or some other point and adjust the VCO coil so that frequency becomes 45.75MHz.
3. Apply 3V to the APC pin (pin 9) and let f1 be the frequency at that time.
   Similarly, apply 3.4V and let f2 be the frequency at that time.

$$\beta = \frac{f2 - f1}{400} \text{ (kHz/mV)}$$

S1. SIF limiting sensitivity • • • • [Vi (lim)]

1. External AGC. Apply the V_{CC} voltage to the IF AGC (pin 17).
2. fs = 4.5MHz, fm = 400Hz, ΔF = ±25kHz (SIF input)
3. Set the SIF input level to 100mVrms and measure the value at test point D at that time. • • V1
4. Lower the SIF input level and measure the input level such that V1 is down by 3dB.

S2, S4. FM detection output voltage, total harmonic distortion • • • • [Vo(FM), THD]

1. External AGC. Apply the V_{CC} voltage to the IF AGC (pin 17).
2. fs = 4.5MHz, fm = 400Hz, ΔF = ±25kHz (SIF input, Vi = 100mVrms)
3. Measure the FM detection output voltage and total harmonic distortion at test point D.

S3. AM rejection ratio • • • • [AMR]

1. External AGC. Apply the V_{CC} voltage to the IF AGC (pin 17).
2. fs = 4.5MHz, fm = 400Hz, AM = 30% (SIF input, Vi = 90dBμV)
3. Measure the output voltage at test point D. • • • VAM
4. $AMR = 20\log \frac{VO\ (DET)}{VAM}$ dB

S5. SIF signal-to-noise ratio • • • • [S/N]

1. External AGC (V17 = V_{CC})
2. fs = 4.5MHz, no modulation, Vi = 100mVrms
3. Measure the output voltage at test point D. • • • • Vn
4. $S/N = 20\log \frac{VO\ (DET)}{Vn}$ dB

S6. 4.5MHz output level • • • • [S/N]

1. External AGC (V17 = V_{CC})
2. fs = 4.5MHz, no modulation, Vi = 10mVrms
3. Measure the output voltage at test point E. • • • • Vsout

Note 1. Unless specified otherwise, when measuring VIF, apply the V_{CC} voltage to the AGC and adjust the VCO coil so that it oscillates at 45.75MHz.

Note 2. Unless specified otherwise, switch SW1 must be in the on position.

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