

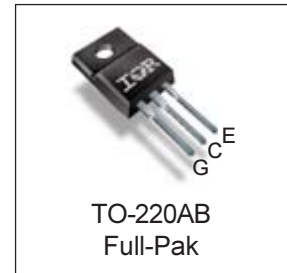
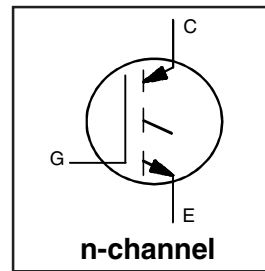
PDP TRENCH IGBT

IRGI4090PbF

Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low $V_{CE(on)}$ and Energy per Pulse (E_{PULSE}^{TM}) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters		
$V_{CE\ min}$	300	V
$V_{CE(on)}\ typ.\ @\ I_C = 11A$	1.20	V
$I_{RP}\ max\ @\ T_C = 25^\circ C$	140	A
$T_J\ max$	150	$^\circ C$



G	C	E
Gate	Collector	Emitter

Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low $V_{CE(on)}$ and low E_{PULSE}^{TM} rating per silicon area which improve panel efficiency. Additional features are $150^\circ C$ operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GE}	Gate-to-Emitter Voltage	± 30	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE} @ 15V$	21	A
$I_C @ T_C = 100^\circ C$	Continuous Collector, $V_{GE} @ 15V$	11	
$I_{RP} @ T_C = 25^\circ C$	Repetitive Peak Current ①	140	
$P_D @ T_C = 25^\circ C$	Power Dissipation	34	W
$P_D @ T_C = 100^\circ C$	Power Dissipation	14	
	Linear Derating Factor	0.27	$W/^\circ C$
T_J	Operating Junction and	-40 to + 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	N

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	3.65	$^\circ C/W$

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{CES}	Collector-to-Emitter Breakdown Voltage	300	—	—	V	$V_{GE} = 0V, I_{CE} = 500\mu A$
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ^②	30	—	—	V	$V_{GE} = 0V, I_{CE} = 1.0A$
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.30	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_{CE} = 5.0\mu A$
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	—	1.20	—	V	$V_{GE} = 15V, I_{CE} = 11A$ ^③
		—	1.67	1.94		$V_{GE} = 15V, I_{CE} = 30A$ ^③
		—	2.43	—		$V_{GE} = 15V, I_{CE} = 60A$ ^③
		—	3.35	—		$V_{GE} = 15V, I_{CE} = 90A$ ^③
		—	4.50	—		$V_{GE} = 15V, I_{CE} = 120A$ ^③
		—	4.75	—		$V_{GE} = 15V, I_{CE} = 90A, T_J = 150^\circ\text{C}$ ^③
$V_{GE(th)}$	Gate Threshold Voltage	2.6	—	5.0	V	$V_{CE} = V_{GE}, I_{CE} = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-12	—	mV/ $^\circ\text{C}$	Reference to 25°C
I_{CES}	Collector-to-Emitter Leakage Current	—	2.0	5.0	μA	$V_{CE} = 300V, V_{GE} = 0V$
		—	5.0	—		$V_{CE} = 300V, V_{GE} = 0V, T_J = 100^\circ\text{C}$
		—	100	—		$V_{CE} = 300V, V_{GE} = 0V, T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Forward Leakage	—	—	100	nA	$V_{GE} = 30V$
	Gate-to-Emitter Reverse Leakage	—	—	-100		$V_{GE} = -30V$
g_{fe}	Forward Transconductance	—	11	—	S	$V_{CE} = 25V, I_{CE} = 11A$
Q_g	Total Gate Charge	—	34	—	nC	$V_{CE} = 200V, I_C = 11A, V_{GE} = 15V$ ^③
Q_{gc}	Gate-to-Collector Charge	—	9.6	—		
$t_{d(on)}$	Turn-On delay time	—	20	—	ns	$I_C = 11A, V_{CC} = 240V$ $R_G = 10\Omega, L = 200\mu H, L_S = 150nH$ $T_J = 25^\circ\text{C}$
t_r	Rise time	—	14	—		
$t_{d(off)}$	Turn-Off delay time	—	99	—		
t_f	Fall time	—	68	—		
$t_{d(on)}$	Turn-On delay time	—	19	—	ns	$I_C = 11A, V_{CC} = 240V$ $R_G = 10\Omega, L = 200\mu H, L_S = 150nH$ $T_J = 150^\circ\text{C}$
t_r	Rise time	—	15	—		
$t_{d(off)}$	Turn-Off delay time	—	139	—		
t_f	Fall time	—	129	—		
t_{st}	Shoot Through Blocking Time	100	—	—	ns	$V_{CC} = 240V, V_{GE} = 15V, R_G = 5.1\Omega$
E_{PULSE}	Energy per Pulse	—	549	—	μJ	$L = 220nH, C = 0.10\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.10\Omega, T_J = 25^\circ\text{C}$
		—	637	—		$L = 220nH, C = 0.10\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.10\Omega, T_J = 100^\circ\text{C}$
C_{ies}	Input Capacitance	—	1153	—	pF	$V_{GE} = 0V$
C_{oes}	Output Capacitance	—	59	—		$V_{CE} = 30V$
C_{res}	Reverse Transfer Capacitance	—	27	—		$f = 1.0MHz$, See Fig.13
L_C	Internal Collector Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L_E	Internal Emitter Inductance	—	7.5	—		from package and center of die contact

Notes:

- ① Half sine wave with duty cycle = 0.05, $PW = 2\mu\text{sec}$.
 ② R_{θ} is measured at T_J of approximately 90°C .
 ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.

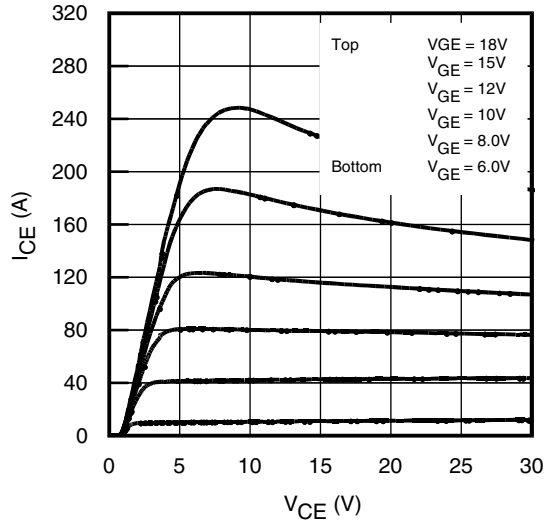


Fig 1. Typical Output Characteristics @ 25°C

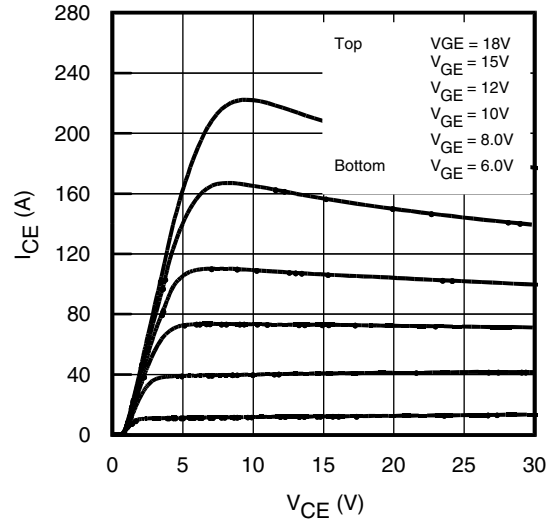


Fig 2. Typical Output Characteristics @ 75°C

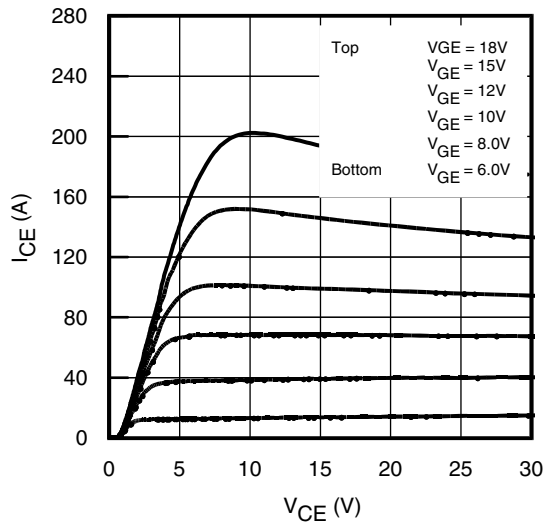


Fig 3. Typical Output Characteristics @ 125°C

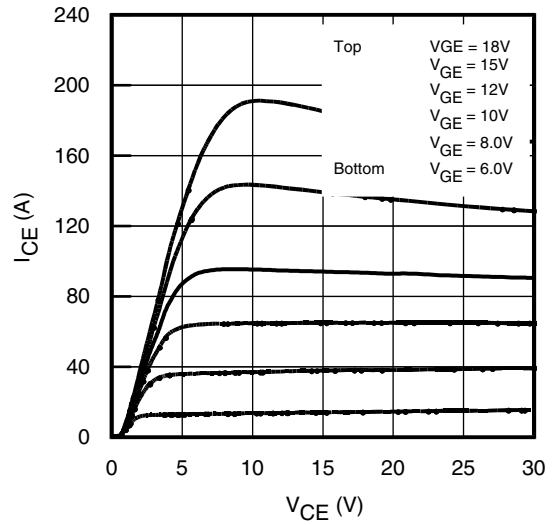


Fig 4. Typical Output Characteristics @ 150°C

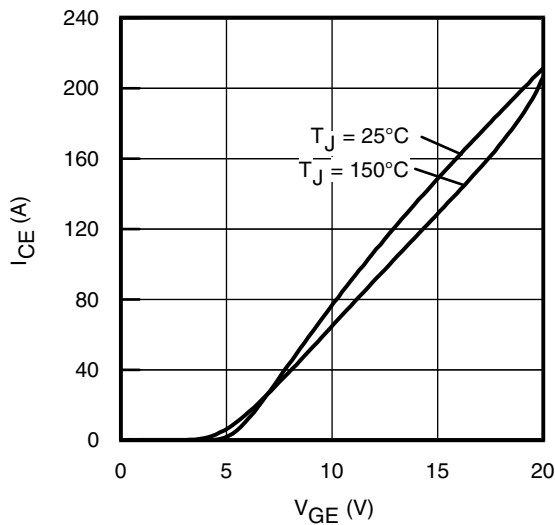


Fig 5. Typical Transfer Characteristics

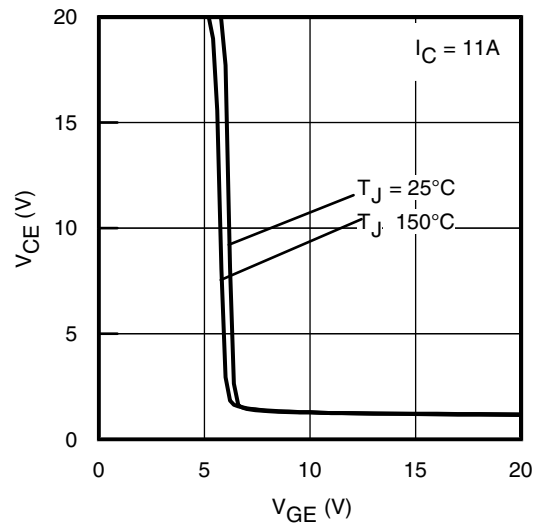


Fig 6. $V_{CE(ON)}$ vs. Gate Voltage

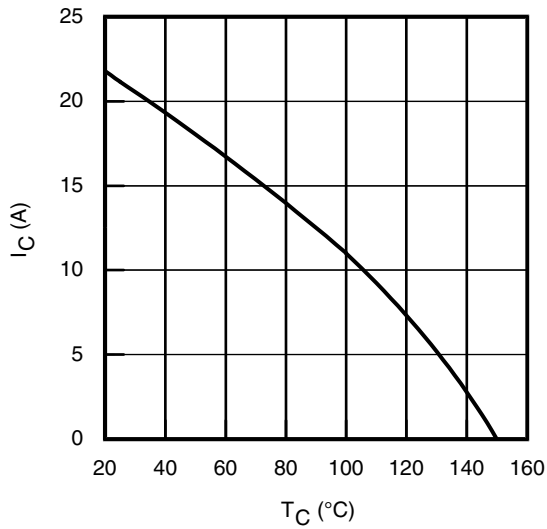


Fig 7. Maximum Collector Current vs. Case Temperature

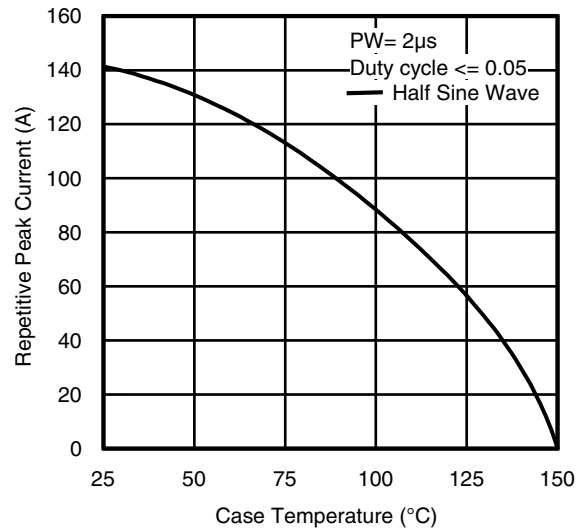


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

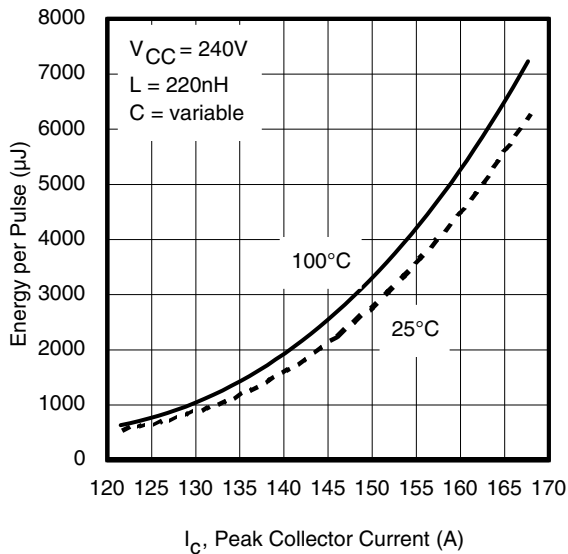


Fig 9. Typical E_{PULSE} vs. Collector Current

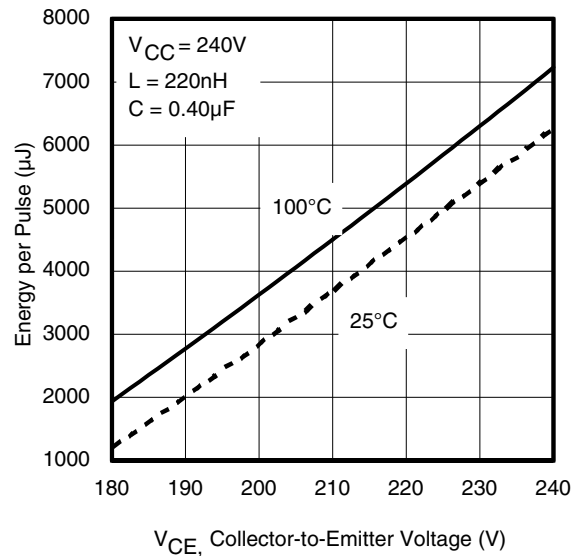


Fig 10. Typical E_{PULSE} vs. Collector-to-Emitter Voltage

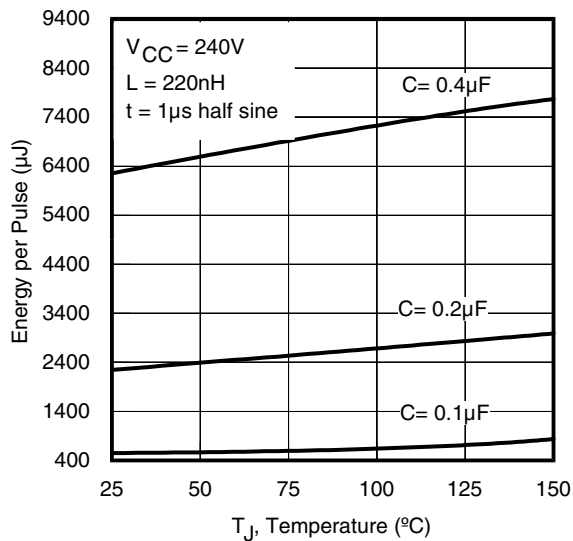


Fig 11. E_{PULSE} vs. Temperature

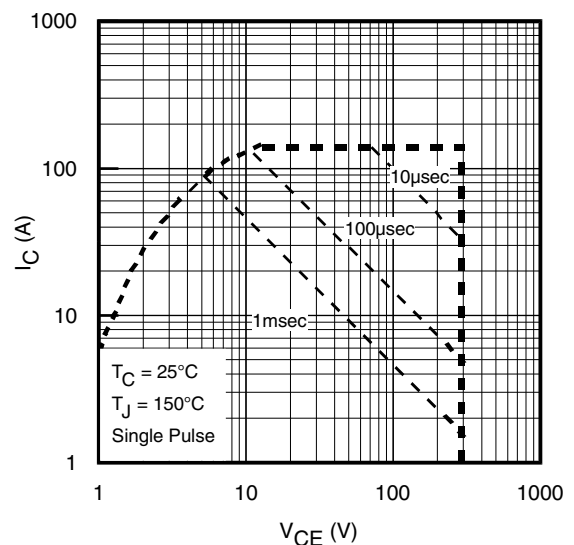


Fig 12. Forward Bias Safe Operating Area

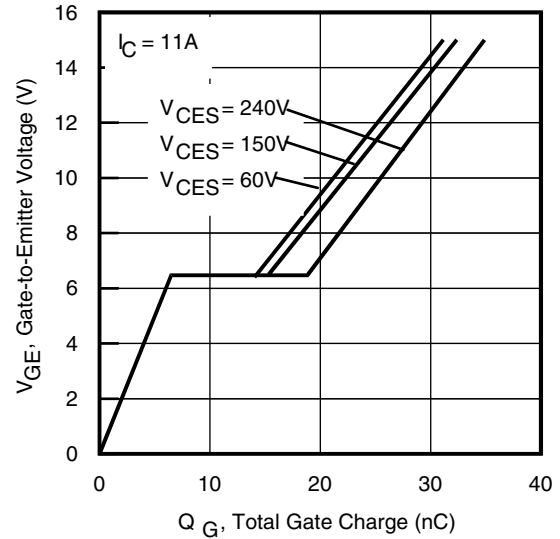
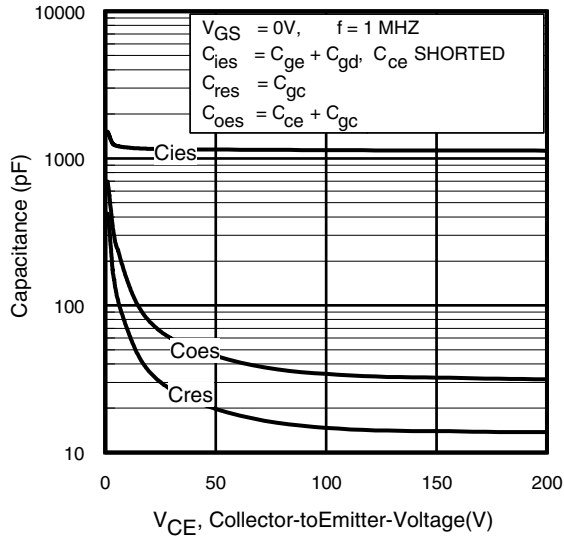


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

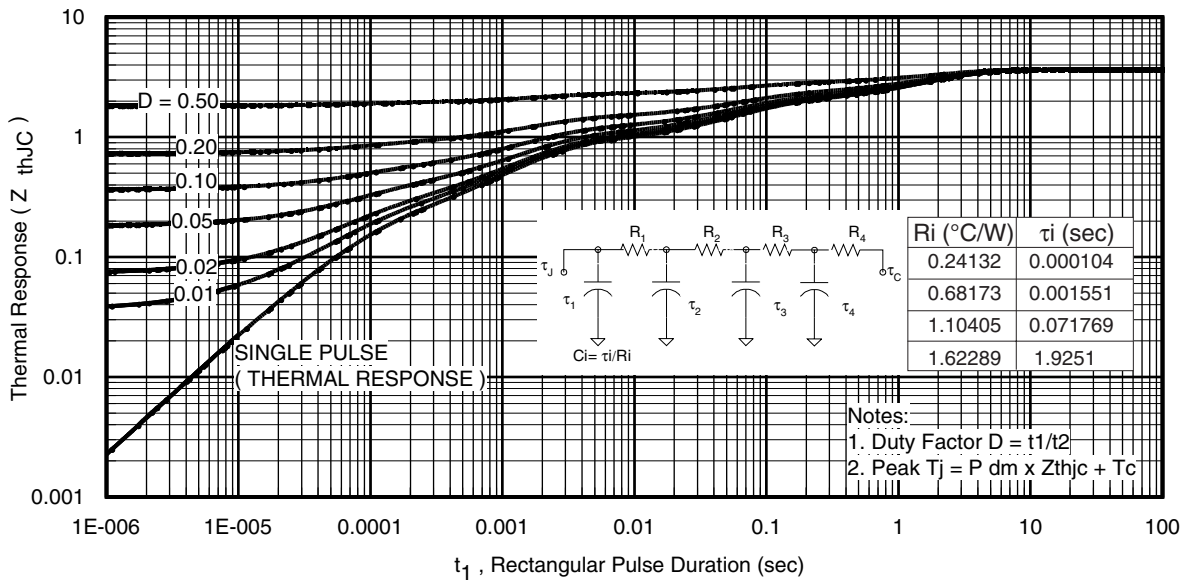


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

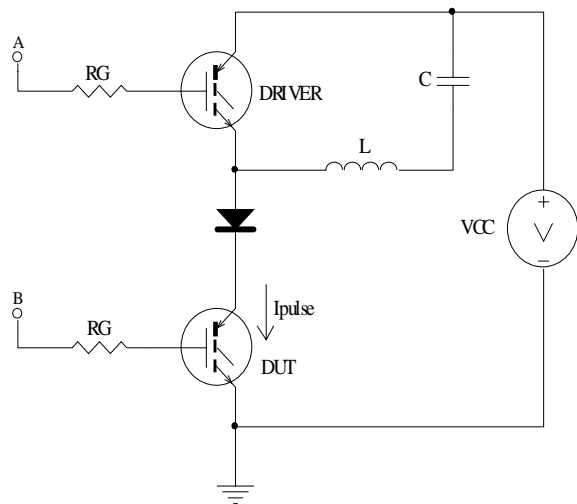


Fig 16a. t_{st} and E_{PULSE} Test Circuit

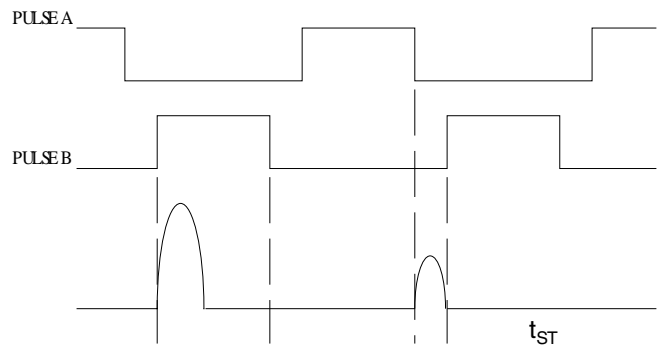


Fig 16b. t_{st} Test Waveforms

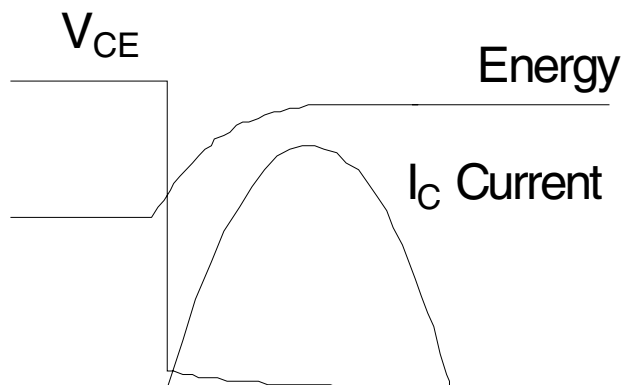


Fig 16c. E_{PULSE} Test Waveforms

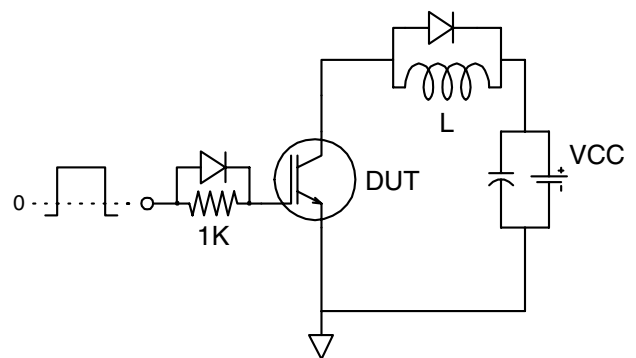
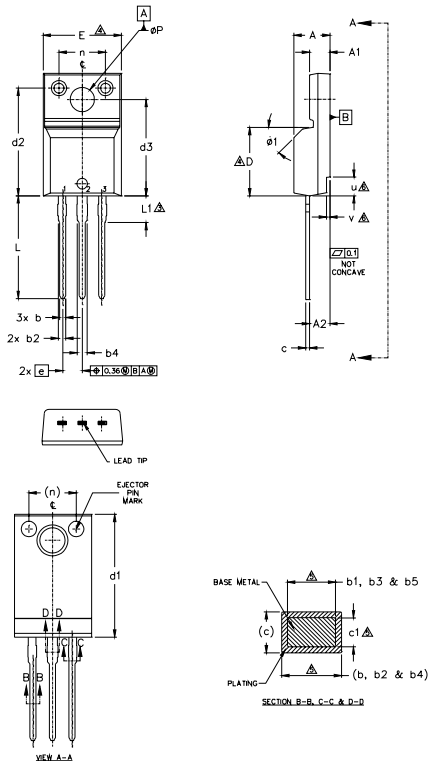


Fig 17 - Gate Charge Circuit (turn-off)

TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	NOTES: 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994. 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]. LEAD DIMENSION AND FINISH UNCONTROLLED IN L1. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY. DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY. STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v. 7.0 CONTROLLING DIMENSION : INCHES.
A1	2.57	2.83	.101	.111	
A2	2.51	2.93	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	
c	0.33	0.63	.013	.025	
c1	0.33	0.58	.013	.023	
D	8.66	9.80	.341	.386	
d1	15.80	16.13	.622	.635	
d2	13.97	14.22	.550	.560	
d3	12.30	12.93	.484	.509	
E	9.63	10.76	.379	.423	
e	2.54	BSC	.100	BSC	
L	13.20	13.72	.520	.540	
L1	3.37	3.67	.122	.145	
n	6.05	6.60	.238	.260	
phi P	3.05	3.45	.120	.136	
u	2.40	2.50	.094	.098	
v	0.40	0.50	.016	.020	
phi 1	-	45°	-	45°	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE

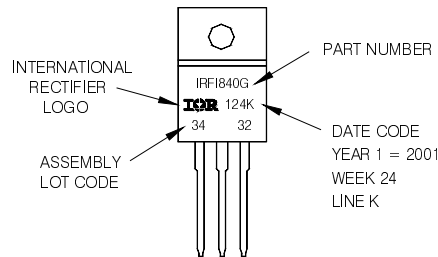
IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24, 2001
IN THE ASSEMBLY LINE 'K'

Note: 'P' in assembly line position indicates 'Lead-Free'



TO-220AB Full-Pak package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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