



3.3V CMOS OCTAL BIDIRECTIONAL TRANSCEIVER

IDT74FCT3245/A

FEATURES:

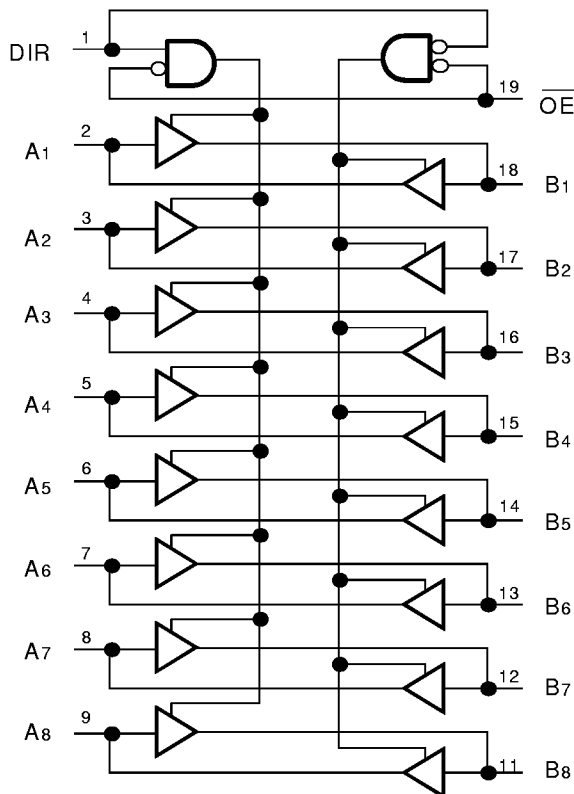
- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range or $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

DESCRIPTION:

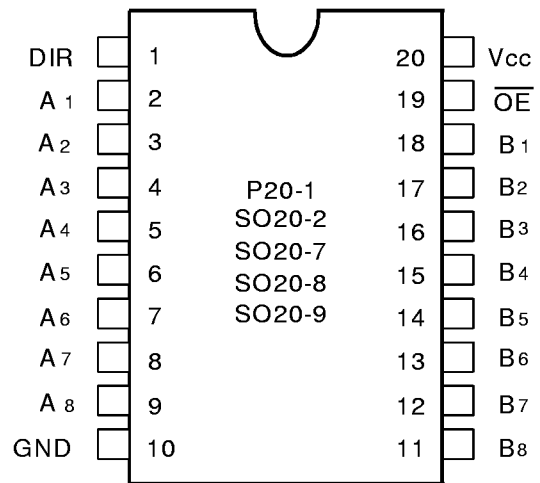
The FCT3245/A octal transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for asynchronous communication between two buses (A and B). The direction control pin (DIR) controls the direction of data flow. The output enable pin ($\overline{OE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

The FCT3245/A has series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP/ SOIC/ SSOP/ QSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to +7	V
V _{TERM} ⁽⁴⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−60 to +60	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	4	8	pF

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NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
DIR	Direction Control Input
Ax	Side A Inputs or 3-State Outputs
Bx	Side B Inputs or 3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
$\overline{OE}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	5.5	V
	Input HIGH Level (I/O pins)			2	—	$V_{CC}+0.5$	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	± 1	μA
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins)		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins)		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		-36	-60	-110	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		50	90	200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.2$	—	—	V
			$I_{OH} = -3\text{mA}$	2.4	3	—	
		$V_{CC} = 3\text{V}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	$2.4^{(5)}$	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 0.1\text{mA}$	—	—	0.2	V
			$I_{OL} = 16\text{mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{mA}$	—	0.3	0.55	
		$V_{CC} = 3\text{V}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 24\text{mA}$		0.3	0.5	
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-135	-240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	0.1	10	μA

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^\circ\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{DIR} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	85	$\mu A/\text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{DIR} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	0.9	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.6	0.9	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{DIR} = \text{GND}$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.2	1.7 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	1.2	1.8 ⁽⁵⁾	

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \text{ DH/NT} + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$
 $\text{NT} = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE ⁽³⁾

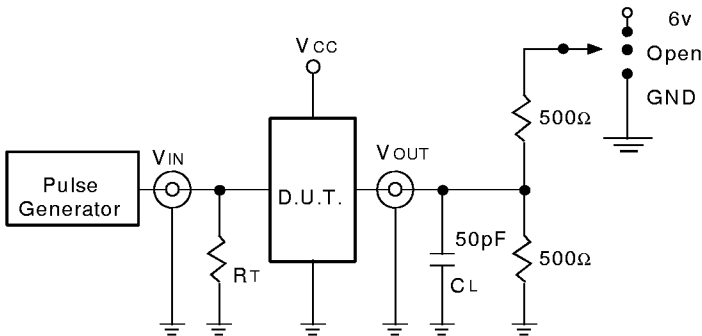
Symbol	Parameter	Condition ⁽¹⁾	FCT3245		FCT3245A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	7	1.5	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	5	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to A or B ⁽⁴⁾		1.5	9.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A or B ⁽⁴⁾		1.5	7.5	1.5	5	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, Normal Range. For $V_{CC} = 2.7V$ to $3.6V$, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
- This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

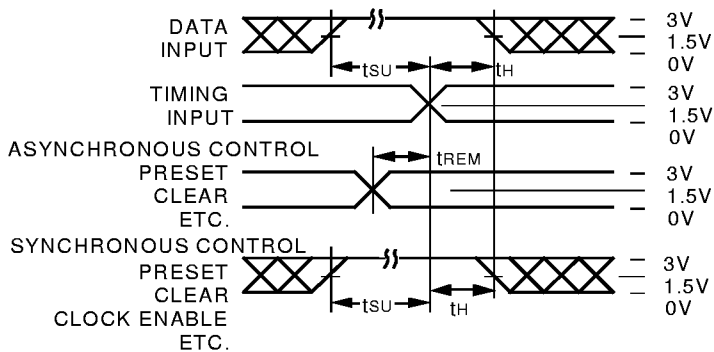
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DEFINITIONS:

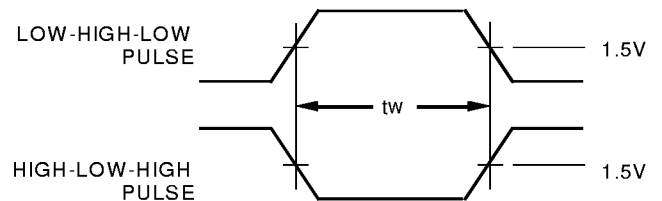
CL = Load capacitance; includes jig and probe capacitance.

RT = Termination resistance; should be equal to ZOUT of the Pulse Generator.

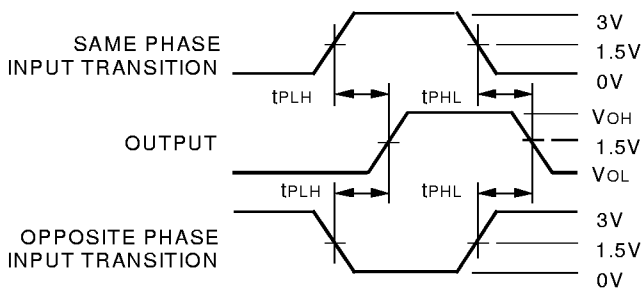
SET-UP, HOLD, AND RELEASE TIMES



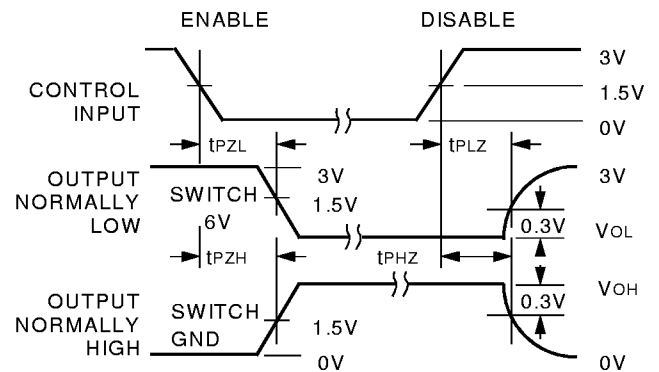
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.
- If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

ORDERING INFORMATION

IDT	XX	FCT	X	XX	X	
Temp. Range		Family		Device Type	Package	
					P	Plastic DIP (P20-1)
					SO	Small Outline IC (SO20-2)
					PY	Shrink Small Outline Package (SO20-7)
					Q	Quarter-size Small Outline Package (SO20-8)
					PG	Thin Shrink Small Outline Package (SO20-9)
				245		Octal Bidirectional Transceiver
				245A		
				3		3.3Volt
				74		- 40 °C to +85 °C



CORPORATE HEADQUARTERS

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