Dual & Quad Precision, Low Power High Speed JFET

Preliminary Technical Data

AD8682/AD8684

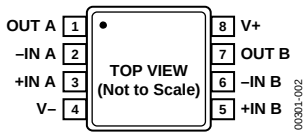
FEATURES

Low supply current: 250 μA/amp max
High slew rate: 9V/μs
Bandwidth: 4 MHz typical
Low offset voltage: 1mV max
Low input bias current: 100 pA maximum
CMRR: 90dB
Fast settling time
Unity Gain Stable

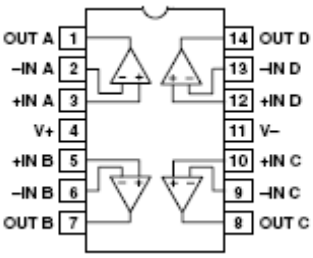
APPLICATIONS

Portable Telecom
Low Power Industrial & Instrumentation
Loop filters
Active & Precision Filters
Integrators
Strain gage amplifiers
Portable Medical instrumentation
Supply current monitoring

PIN CONFIGURATIONS



SOIC-8 lead, & MSOP-8 lead



SOIC-14 lead & TSSOP-14

GENERAL DESCRIPTION

The AD8682 and AD8684 are dual low power, precision (1mV) JFET amplifier featuring excellent speed at low supply currents. The slew rate is typically 9V/μs with a supply current under 250 μA per amplifier. These unity-gain stable amplifiers have a typical gain bandwidth of 4 MHz. The JFET input stage ensures bias current is typically a few picoamps and below 500pA over the full temperature operating range. The devices are ideal for portable, low power applications, especially with high source impedance. The device is unity gain stable and can drive higher cap loads (G=1, non-inverting) as an example of its excellent dynamic response over a wide range of conditions, delivering DC precision performance at low quiescent currents.

Rev. PrA

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_S = ±15.0 V, V_{CM} = 0 V, T_A = 25°C unless otherwise noted.)

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				1	mV
Input Bias Current	I_B	V_{CM} = 0 V			100	pA
		0°C ≤ T_A ≤ +70°C			100	pA
		−40°C ≤ T_A ≤ +85°C			500	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V			50	pA
		−40°C ≤ T_A ≤ +85°C			250	pA
Input Voltage Range			-11		+15	V
Common-Mode Rejection Ratio	CMRR	-11 < V_{CM} < +15 V, −40°C ≤ T_A ≤ +85°C	70	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20			V/mV
		R_L = 10 kΩ, −40 V ≤ T_A ≤ +85°C	15			V/mV
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C			10	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ	13.5	13.9		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ		-13.9	-13.5	V
Short-Circuit Limit	I_{SC}	Source	3	10		mA
		Sink		-12	-8	mA
Open-loop Output Impedance	I_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V, −40°C ≤ T_A ≤ +85°C		25	316	µV/V
Supply Current/Amplifier	I_{SY}	V_O = 0 V, −40°C ≤ T_A ≤ +85°C		210	250	µA
Supply Voltage Range	V_S	V_S = ± 18 V, −40°C ≤ T_A ≤ +85°C	± 4.5		± 18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	7	9		V/µs
Settling Time	t_S	To 0.01%		125		kHz
Full-Power Bandwidth	BW_P	1% distortion		1.6		µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	Øo			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		1.3		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		30		nV/√Hz
Current Noise Density	i_N			0.01		pA/√Hz

NOTES

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