

# XE88LC04

## Ultra low-power MCU with LCD driver

### General Description

- The XE88LC04 is an ultra low-power low-voltage microcontroller unit (MCU) with extremely high efficiency, allowing for 1 MIPS at 300uA and 2.4 V, and 8 x 8 bits multiplying in one clock cycle at 1.2 V.
- The XE88LC04 includes an LCD driver for up to 120 segments. The LCD lines can be used as additional IOs.
- XE88LC04 is available with on chip ROM or Multiple-Time-Programmable (MTP) program memory.

### Applications

- Portable, battery operated instruments
- RF system supervisor
- Remote control
- HVAC control
- Watches

### Key product Features

- Low-voltage low-power controller operation
  - 4 MIPS at 2.4 V to 5.5 V supply (ROM)
  - 2 MIPS at 2.4 V to 5.5 V supply (MTP)
  - 300  $\mu$ A at 1 MIPS, 2.4 V to 5.5 V supply
- 22 kByte (8 kInstruction) MTP, 1032 Byte RAM
- RC and crystal oscillators
- 5 reset, 16 interrupt, 8 event sources
- 120 segments LCD driver
- 100 years MTP Flash retention at 55°C

### Ordering Information

| Product       | Temperature range | Memory type | Package |
|---------------|-------------------|-------------|---------|
| XE88LC04MI03x | -40°C to 85 °C    | MTP         | BGA     |

# 1 Detailed Pin Description

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To be added

## 2 Absolute maximum ratings

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Stresses beyond these listed in this chapter may cause permanent damage to the device. No functional operation is implied at or beyond these conditions. Exposure to these conditions for an extended period may affect the device reliability.

| Parameter                                      | Valéue                |
|--|-----------------------|
| VBAT with respect to VSS                       | -0.3V to 6.0V         |
| Input voltage on any input pin                 | VSS-0.3V to VBAT+0.3V |
| Storage temperature                            | -55°C to 125°C        |
| Storage temperature for programmed MTP devices | -40°C to 85°C         |

**Table 2.1:** Absolute maximum ratings

These devices are ESD sensitive. Although these devices feature proprietary ESD protection structures, permanent damage may occur on devices subjected to high energy electrostatic discharges. Proper ESD precautions have to be taken to avoid performance degradation or loss of functionality.

### 3 Electrical Characteristics

All specification are -40°C to 85°C unless otherwise noted. ROM operates up to 125°C.

| Operation conditions         |   | min   | typ | max  | Unit  | Remarks |
|------------------------------|---|-------|-----|------|-------|---------|
| Power supply                 | ROM version                               | 2.4   |     | 5.5  | V     |         |
|                              | MTP version                               | 2.4   |     | 5.5  | V     |         |
| Operating speed              | 2.4 V to 5.5 V                            | 0.032 |     | 4    | MHz   |         |
| Instruction cycle            | any instruction                           |       | 250 |      | ns    | 7       |
| Current requirement          | CPU running at 1 MIPS                     |       |     | 310  | uA    | 1       |
|                              | CPU running at 32 kHz on Xtal, RC off     |       |     | 10   | uA    | 1       |
|                              | CPU halt, timer on Xtal, RC off           |       |     | 1    | uA    | 1       |
|                              | CPU halt, timer on Xtal, RC ready         |       |     | 1.7  | uA    | 1       |
|                              | CPU halt, Xtal off timer on RC at 100 kHz |       |     | 1.4  | uA    | 1       |
|                              | Voltage level detection                   |       |     | 15   | uA    |         |
| MTP Flash instruction memory | Prog. voltage                             | 10.3  |     | 10.8 | V     |         |
|                              | Erase time                                | 0.2   |     | 1    | s     | 8       |
|                              | Write/Erase cycles                        | 10    | 100 |      |       | 5       |
|                              | Data retention                            |       | 10  |      |       | years   |
|                              |   | 100   |     |      | years | 55°C, 2 |

**Table 3.1:** Specifications and current requirement of the XE88LC04

**Note:**

- 1) Power supply: 2.4 V - 5.5 V, temperature is 27°C.
- 2) < 10 erase cycles.
- 3) Output not loaded.
- 4) Current requirement can be divided by a factor of 2 or 4 by reducing the speed accordingly.
- 5) More cycles possible during development, with restraint retention
- 6) Power supply: 3.0V, at 27°C;
- 7) With 4 MHz clock, all instructions are using exactly 1 clock cycle
- 8) Longer erase time may degrade retention

## 4 CPU

The XE88LC06 CPU is a low power RISC core. It has 16 internal registers for efficient implementation of the C compiler. Its instruction set is made of 35 generic instructions, all coded on 22 bits, with 8 addressing modes. All instructions are executed in one clock cycle, including conditional jumps and 8x8 multiplication, therefore the XE88LC06 runs at 1 MIPS on a 1 MHz clock.

The CPU description with its instruction set can be found in the XE8000 databook.

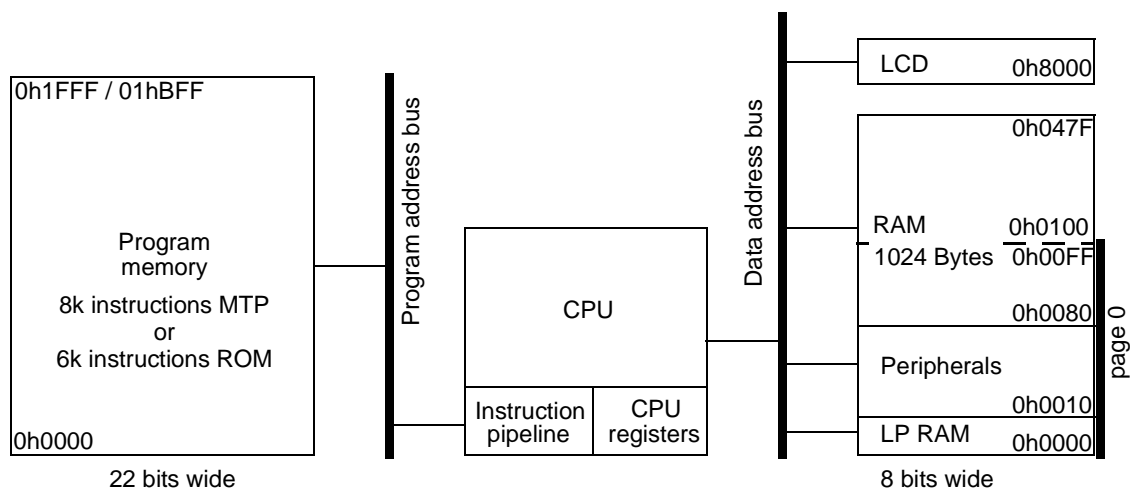
The good code efficiency of the XE8000 core makes it possible to compute a polynomial like

$Z = (A_0 + A_1 \cdot Y) \cdot X + B_0 + B_1 \cdot Y$  in less than 300 clock cycles (code generated by the XEMICS C-compiler, all numbers are Signed Integers on 16 bits).

## 5 Memory organisation

The CPU uses a Harvard architecture, so that memory is organised in two separated fields: program memory and data memory. As both memory are separated, the central processing unit can read/write data at the same time it loads an instruction. Peripherals and system control registers are mapped on data memory space.

Program memory is made in one page. Data is made of several 256 bytes pages.



**Figure 5.1:** Memory organization

## 5.1 Program memory

The program memory is implemented as Multiple Time Programmable (MTP) Flash memory. The power consumption of MTP memory is linear with the access frequency (no significant static current).

- Size of the MTP Flash memory is 8192 x 22 bits (= 22 kBytes)
- Size of the ROM memory is 6144 x 22 bits (= 17 kBytes)

| block | size      | address       |
|-------|-----------|---------------|
| MTP   | 8192 x 22 | H0000 - H1FFF |
| ROM   | 6144 x 22 | H0000 - H1BFF |

**Table 5.1:** Program addresses for MTP or ROM memory

## 5.2 Data memory

The data memory is implemented as static Random-Access Memory (RAM). The RAM size is 512 x 8 bits plus 8 low power RAM bytes that require very low current when addressed. Programs using the low-power RAM instead of RAM will use even less current.

| block  | size     | address       |
|--------|----------|---------------|
| LP RAM | 8 x 8    | H0000 - H0007 |
| RAM    | 1024 x 8 | H0080 - H047F |

**Table 5.2:** RAM addresses

## 6 Registers list

Left column include register name and address.

Right columns include bit name, access (r: read, r0: always 0 when read, w: write, c: cleared by writing any value, c1: cleared by writing 1), and reset status (0 or 1) and signal. Empty bits are reserved for future use and should not be written, neither should their read value be used for any purpose as it may change without notice.

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### 6.1 Peripherals mapping

| block              | size  | address       | Page   |
|--------------------|-------|---------------|--------|
| LP RAM             | 8x8   | H0000-H0007   | Page 0 |
| System control     | 16x8  | H0010-H001F   |        |
| Port A             | 8x8   | H0020-H0027   |        |
| Port B             | 8x8   | H0028-H002F   |        |
| Port C             | 4x8   | H0030-H0033   |        |
| Port D             | 4x8   | H0034-H0037   |        |
| MTP                | 4x8   | H0038-H003B   |        |
| Event              | 4x8   | H003C-H003F   |        |
| Interrupts control | 8x8   | H0040-H0047   |        |
| reserved           | 8x8   | H0048-H004F   |        |
| UART               | 8x8   | H0050-H0057   |        |
| Counters           | 8x8   | H0058-H005F   |        |
| Reserved           | 8x8   | H0060-H0067   |        |
| SPI                | 8x8   | H0068-H006F   |        |
| Reserved           | 12x8  | H0070-H007B   |        |
| VLD                | 4x8   | H007C-H007F   |        |
| RAM1               | 128x8 | H0080 - H00FF |        |
| RAM2               | 256x8 | H0100 - H01FF |        |
| RAM3               | 256x8 | H0200 - H02FF |        |
| RAM4               | 256x8 | H0300 - H03FF |        |
| RAM5               | 128x8 | H0400 - H047F |        |
| LCD                | 32x8  | H8000-H803F   |        |

**Table 6.1:** Peripherals addresses

### 6.2 Resets

The reset source name is simplified in the following registers description. Name mapping is in the next table.

| reset source | name in this document |
|--------------|-----------------------|
| nresetglobal | global                |
| nresetcold   | cold                  |
| nresetpconf  | pconf                 |
| nresetsleep  | sleep                 |

**Table 6.2:** Reset signal name mapping

### 6.3 Low power RAM

Low power RAM is a small additional RAM area with extremely low power requirement.

| Name<br>Address | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|-----------------|----|----|----|----|----|----|----|----|
| h0000           | rw | rw | rw | rw | rw | rw | rw | rw |
| h0001           | rw | rw | rw | rw | rw | rw | rw | rw |
| h0002           | rw | rw | rw | rw | rw | rw | rw | rw |
| h0003           | rw | rw | rw | rw | rw | rw | rw | rw |
| h0004           | rw | rw | rw | rw | rw | rw | rw | rw |
| h0005           | rw | rw | rw | rw | rw | rw | rw | rw |
| h0006           | rw | rw | rw | rw | rw | rw | rw | rw |
| h0007           | rw | rw | rw | rw | rw | rw | rw | rw |

**Table 6.3:** Low power RAM

### 6.4 System, oscillators, prescaler and watchdog

| Name<br>Address        | 7                     | 6                               | 5                                | 4                                | 3                                  | 2                                  | 1                                  | 0   |
|------------------------|-----------------------|---------------------------------|----------------------------------|----------------------------------|------------------------------------|------------------------------------|------------------------------------|---|
| RegSysCtrl<br>h0010    | SleepEn<br>rw, 0 cold | EnReset-<br>PConf<br>rw, 0 cold | EnBus-Error<br>rw, 0 cold        | EnResWD<br>rw, 0 cold            |                                    |                                    |                                    |   |
| RegSysReset<br>h0011   | Sleep<br>w, 0 global  | SleepFlag<br>rc, 0 cold         | ResBus-<br>Error<br>rc, 0 cold   | ResWD<br>rc, 0 cold              | ResPortA<br>rc, 0 cold             |                                    |                                    |   |
| RegSysClock<br>h0012   |                       | ExtClk<br>r, 0 cold             | EnExtClk<br>rw, 0 cold           | BiasRC<br>rw, 1 cold             | ColdXtal<br>r, 1 sleep             |                                    | EnableXtal<br>rw, 0 sleep          | EnableRC<br>rw, 1 sleep                         |
| RegSysMisc<br>h0013    |                       |                                 |                                  |                                  |                                    |                                    | Output16k<br>rw, 0 sleep           | Output-<br>CkCPU<br>rw, 0 sleep                 |
| RegSysWD<br>h0014      |                       |                                 |                                  |                                  | WatchDog(3)<br>special             | WatchDog(2)<br>special             | WatchDog(1)<br>special             | WatchDog(0)<br>special                          |
| RegSysPre0<br>h0015    |                       |                                 |                                  |                                  |                                    |                                    |                                    | ResPre<br>ClearLow-<br>Prescal (*)<br>w, 0 cold |
| RegSysRCTrim1<br>h001B |                       |                                 |                                  | RCFreq-<br>Range<br>rw, 0 cold   | RCFreq-<br>Coarse(3)<br>rw, 0 cold | RCFreq-<br>Coarse(2)<br>rw, 0 cold | RCFreq-<br>Coarse(1)<br>rw, 0 cold | RCFreq-<br>Coarse(0)<br>rw, 0 cold              |
| RegSysRCTrim2<br>h001C |                       |                                 | RCFreq-<br>Fine(5)<br>rw, 1 cold | RCFreq-<br>Fine(4)<br>rw, 0 cold | RCFreq-<br>Fine(3)<br>rw, 0 cold   | RCFreq-<br>Fine(2)<br>rw, 0 cold   | RCFreq-<br>Fine(1)<br>rw, 0 cold   | RCFreq-<br>Fine(0)<br>rw, 0 cold                |
| RegSysVIReg<br>h001D   |                       |                                 |                                  |                                  |                                    |                                    |                                    |   |

**Table 6.4:** System control registers



## 6.5 PortA

| Name          | 7            | 6            | 5            | 4            | 3            | 2            | 1            | 0            |
|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| RegPAIn       | PAIn(7)      | RegPAIn(6)   | PAIn(5)      | PAIn(4)      | PAIn(3)      | PAIn(2)      | PAIn(1)      | PAIn(0)      |
| h0020         | r            | r            | r            | r            | r            | r            | r            | r            |
| RegPADebounce | PADeb(7)     | PADeb(6)     | PADeb(5)     | PADeb(4)     | PADeb(3)     | PADeb(2)     | PADeb(1)     | PADeb(0)     |
| h0021         | rw, 0 pconf  | rw, 0 pconf  | rw, 0 pconf  | rw, 0 pconf  | rw, 0 pconf  | rw, 0 pconf  | rw, 0 pconf  | rw, 0 pconf  |
| RegPAEdge     | PAEdge(7)    | PAEdge(6)    | PAEdge(5)    | PAEdge(4)    | PAEdge(3)    | PAEdge(2)    | PAEdge(1)    | PAEdge(0)    |
| h0022         | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global |
| RegPAPullup   | PAPullUp(7)  | PAPullUp(6)  | PAPullUp(5)  | PAPullUp(4)  | PAPullUp(3)  | PAPullUp(2)  | PAPullUp(1)  | PAPullUp(0)  |
| h0023         | rw, 1 pconf  | rw, 1 pconf  | rw, 1 pconf  | rw, 1 pconf  | rw, 1 pconf  | rw, 1 pconf  | rw, 1 pconf  | rw, 1 pconf  |
| RegPARes0     | PARes0(7)    | PARes0(6)    | PARes0(5)    | PARes0(4)    | PARes0(3)    | PARes0(2)    | PARes0(1)    | PARes0(0)    |
| h0024         | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global |
| RegPARes1     | PARes1(7)    | PARes1(6)    | PARes1(5)    | PARes1(4)    | PARes1(3)    | PARes1(2)    | PARes1(1)    | PARes1(0)    |
| h0025         | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global | rw, 0 global |
| RegSysPACtrl  |              |              |              |              |              |              |              | DebFast      |
| h0026         |              |              |              |              |              |              |              | rw, 0 pconf  |
| RegSysPASnap  | tbd          | tbd          | tbd          | tbd          | tbd          | tbd          | tbd          | tbd          |
| h0027         |              |              |              |              |              |              |              |              |

**Table 6.5:** Port A registers

## 6.6 PortB

| Name        | 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| RegPBOut    | PBOut(7)    | PBOut(6)    | PBOut(5)    | PBOut(4)    | PBOut(3)    | PBOut(2)    | PBOut(1)    | PBOut(0)    |
| h0028       | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf |
| RegPBIn     | PBIn(7)     | PBIn(6)     | PBIn(5)     | PBIn(4)     | PBIn(3)     | PBIn(2)     | PBIn(1)     | PBIn(0)     |
| h0029       | r           | r           | r           | r           | r           | r           | r           | r           |
| RegPBDir    | PBDir(7)    | PBDir(6)    | PBDir(5)    | PBDir(4)    | PBDir(3)    | PBDir(2)    | PBDir(1)    | PBDir(0)    |
| h002A       | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf |
| RegPBOpen   | PBOpen(7)   | PBOpen(6)   | PBOpen(5)   | PBOpen(4)   | PBOpen(3)   | PBOpen(2)   | PBOpen(1)   | PBOpen(0)   |
| h002B       | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf |
| RegPBPullup | PBPullUp(7) | PBPullUp(6) | PBPullUp(5) | PBPullUp(4) | PBPullUp(3) | PBPullUp(2) | PBPullUp(1) | PBPullUp(0) |
| h002C       | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf |
| RegPBAna    |             |             |             |             | PBAna(3)    | PBAna(2)    | PBAna(1)    | PBAna(0)    |
| h002D       |             |             |             |             | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf |

**Table 6.6:** Port B registers

## 6.7 PortC

| Name        | 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| RegPCOut    | PCOut(7)    | PCOut(6)    | PCOut(5)    | PCOut(4)    | PCOut(3)    | PCOut(2)    | PCOut(1)    | PCOut(0)    |
| h0030       | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf |
| RegPCIn     | PCIn(7)     | PCIn(6)     | PCIn(5)     | PCIn(4)     | PCIn(3)     | PCIn(2)     | PCIn(1)     | PCIn(0)     |
| h0031       | r           | r           | r           | r           | r           | r           | r           | r           |
| RegPCDir    | PCDir(7)    | PCDir(6)    | PCDir       | PCDir(4)    | PCDir(3)    | PCDir(2)    | PCDir(1)    | PCDir(0)    |
| h0032       | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf | rw, 0 pconf |
| RegPCPullup | PCPullup(7) | PCPullup(6) | PCPullup(5) | PCPullup(4) | PCPullup(3) | PCPullup(2) | PCPullup(1) | PCPullup(0) |
| h0033       | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf | rw, 1 pconf |

**Table 6.7:** Port C registers

## 6.8 MTP

| Name             | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Address          |         |         |         |         |         |         |         |         |
| RegEEP<br>h0038  | rw      | rw      | rw      | rw      | rw      | rw      | rw      | rw      |
| RegEEP1<br>h0039 | rw      | rw      | rw      | rw      | rw      | rw      | rw      | rw      |
| RegEEP2<br>h003A | special | special | special | special | special | special | special | special |
| RegEEP3<br>h003B | special | special | special | special | special | special | special | special |

**Table 6.8:** MTP control registers

## 6.9 Events

| Name                    | 7                            | 6                            | 5                            | 4                            | 3                            | 2                            | 1                            | 0                            |
|-------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|
| Address                 |                              |                              |                              |                              |                              |                              |                              |                              |
| RegEvn<br>h003C         | EvnCntA<br>rc1, 0 global     | EvnCntC<br>rc1, 0 global     | EvnPre1<br>rc1, 0 global     | EvnPA(1)<br>rc1, 0 global    | EvnCntB<br>rc1, 0 global     | EvnCntD<br>rc1, 0 global     | EvnPre2<br>rc1, 0 global     | EvnPA(0)<br>rc1, 0 global    |
| RegEvnEn<br>h003D       | EvnEnCntA<br>rw, 0 global    | EvnEnCntC<br>rw, 0 global    | EvnEnPre1<br>rw, 0 global    | EvnEnPA(1)<br>rw, 0 global   | EvnEnCntB<br>rw, 0 global    | EvnEnCntD<br>rw, 0 global    | EvnEnPre2<br>rw, 0 global    | EvnEnPA(0)<br>rw, 0 global   |
| RegEvnPriority<br>h003E | EvnPriority(7)<br>r,1 global | EvnPriority(6)<br>r,1 global | EvnPriority(5)<br>r,1 global | EvnPriority(4)<br>r,1 global | EvnPriority(3)<br>r,1 global | EvnPriority(2)<br>r,1 global | EvnPriority(1)<br>r,1 global | EvnPriority(0)<br>r,1 global |
| RegEvnEvn<br>h003F      |                              |                              |                              |                              |                              |                              | EvnHigh<br>r, 0 global       | EvnLow<br>r, 0 global        |

**Table 6.9:** Events control registers

## 6.10 Interrupts

| Name                    | 7                                    | 6                                   | 5                             | 4                             | 3                             | 2                             | 1                             | 0                             |
|-------------------------|--------------------------------------|-------------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|
| Address                 |                                      |                                     |                               |                               |                               |                               |                               |                               |
| RegIrqHig<br>h0040      |                                      | IrqPre1<br>rc1, 0 global            |                               | IrqCntA<br>rc1, 0 global      | IrqCntC<br>rc1, 0 global      | IrqCmpd<br>rc1, 0 global      | IrqUartTx<br>rc1, 0 global    | IrqUartRx<br>rc1, 0 global    |
| RegIrqMid<br>h0041      | IrqUsrtCond2<br>rc1, 0 global        | IrqUsrtCond1<br>rc1, 0 global       | IrqPA(5)<br>rc1, 0 global     | IrqPA(4)<br>rc1, 0 global     | IrqPre2<br>rc1, 0 global      | IrqVld<br>rc1, 0 global       | IrqPA(1)<br>rc1, 0 global     | IrqPA(0)<br>rc1, 0 global     |
| RegIrqLow<br>h0042      | IrqPA(7)<br>rc1, 0 global            | IrqPA(6)<br>rc1, 0 global           | IrqCntB<br>rc1, 0 global      | IrqCntD<br>rc1, 0 global      | IrqPA(3)<br>rc1, 0 global     | IrqPA(2)<br>rc1, 0 global     |                               |                               |
| RegIrqEnHig<br>h0043    |                                      | IrqEnPre1<br>rw, 0 global           |                               | IrqEnCntA<br>rw, 0 global     | IrqEnCntC<br>rw, 0 global     | IrqEnCmpd<br>rw, 0 global     | IrqEnUartTx<br>rw, 0 global   | IrqEnUartRx<br>rw, 0 global   |
| RegIrqEnMid<br>h0044    | IrqEnUsrt-<br>tCond2<br>rw, 0 global | IrqEnUsrt-<br>Cond1<br>rw, 0 global | IrqEnPA(5)<br>rw, 0 global    | IrqEnPA(4)<br>rw, 0 global    | IrqEnPre2<br>rw, 0 global     | IrqEnVld<br>rw, 0 global      | IrqEnPA(1)<br>rw, 0 global    | IrqEnPA(0)<br>rw, 0 global    |
| RegIrqEnLow<br>h0045    | IrqEnPA(7)<br>rw, 0 global           | IrqEnPA(6)<br>rw, 0 global          | IrqEnCntB<br>rw, 0 global     | IrqEnCntD<br>rw, 0 global     | IrqEnPA(3)<br>rw, 0 global    | IrqEnPA(2)<br>rw, 0 global    |                               |                               |
| RegIrqPriority<br>h0046 | IrqPriority(7)<br>r, 1 global        | IrqPriority(6)<br>r, 1 global       | IrqPriority(5)<br>r, 1 global | IrqPriority(4)<br>r, 1 global | IrqPriority(3)<br>r, 1 global | IrqPriority(2)<br>r, 1 global | IrqPriority(1)<br>r, 1 global | IrqPriority(0)<br>r, 1 global |
| RegIrqIrq<br>h0047      |                                      |                                     |                               |                               |                               | IrqHig<br>r, 0 global         | IrqMid<br>r, 0 global         | IrqLow<br>r, 0 global         |

**Table 6.10:** Interrupts control registers

## 6.11 USRT

| Name                     | 7 | 6 | 5 | 4 | 3                         | 2                                    | 1                            | 0                          |
|--------------------------|---|---|---|---|---------------------------|--------------------------------------|------------------------------|----------------------------|
| Address                  |   |   |   |   |                           |                                      |                              |                            |
| RegUsrtS1<br>h0048       |   |   |   |   |                           |                                      |                              | UsrtS1<br>rw, 1 global     |
| RegUsrtS0<br>h0049       |   |   |   |   |                           |                                      |                              | UsrtS0<br>rw, 1 global     |
| RegUsrtCtrl<br>h004A     |   |   |   |   | UsrtWaitS0<br>r, 0 global | UsrtEnWait-<br>Cond1<br>rw, 0 global | UsrtEnWaitS0<br>rw, 0 global | UsrtEnable<br>rw, 0 global |
| RegUsrtCond1<br>h004B    |   |   |   |   |                           |                                      |                              | UsrtCond1<br>rc, 0 global  |
| RegUsrtCond2<br>h004C    |   |   |   |   |                           |                                      |                              | UsrtCond2<br>rc, 0 global  |
| RegUsrtBufferS1<br>h004D |   |   |   |   |                           |                                      |                              | UsrtBufferS1<br>r          |
| RegUsrtEdgeS0<br>h004E   |   |   |   |   |                           |                                      |                              | UsrtEdgeS0<br>r, 0 global  |
| Reserved<br>h004F        |   |   |   |   |                           |                                      |                              |                            |

**Table 6.11:** USRT control registers

## 6.12 UART

| Name                  | 7                         | 6                          | 5                            | 4                            | 3                            | 2                         | 1                         | 0                         |
|-----------------------|---------------------------|----------------------------|------------------------------|------------------------------|------------------------------|---------------------------|---------------------------|---------------------------|
| Address               |                           |                            |                              |                              |                              |                           |                           |                           |
| RegUartCtrl<br>h0050  | UartEcho<br>rw, 0 global  | UartEnRx<br>rw, 0 global   | UartEnTx<br>rw, 0 global     | UartXRx<br>rw, 0 global      | UartXTx<br>rw, 0 global      | UartBR(2)<br>rw, 1 global | UartBR(1)<br>rw, 0 global | UartBR(0)<br>rw, 1 global |
| RegUartCmd<br>h0051   | SeIXtal<br>rw, 0 global   | UartWakeup<br>rw, 0 global | UartRCSel(2)<br>rw, 0 global | UartRCSel(1)<br>rw, 0 global | UartRCSel(0)<br>rw, 0 global | UartPM<br>rw, 0 global    | UartPE<br>rw, 0 global    | UartWL<br>rw, 1 global    |
| RegUartTx<br>h0052    | UartTx(7)<br>rw, 0 global | UartTx(6)<br>rw, 0 global  | UartTx(5)<br>rw, 0 global    | UartTx(4)<br>rw, 0 global    | UartTx(3)<br>rw, 0 global    | UartTx(2)<br>rw, 0 global | UartTx(1)<br>rw, 0 global | UartTx(0)<br>rw, 0 global |
| RegUartTxSta<br>h0053 |                           |                            |                              |                              |                              |                           | UartTxBusy<br>r, 0 global | UartTxFull<br>r, 0 global |
| RegUartRx<br>h0054    | UartRx(7)<br>r            | UartRx(6)<br>r             | UartRx(5)<br>r               | UartRx(4)<br>r               | UartRx(3)<br>r               | UartRx(2)<br>r            | UartRx(1)<br>r            | UartRx(0)<br>r            |
| RegUartRxSta<br>h0055 |                           |                            | UartRxSErr<br>r              | UartRxPErr<br>r              | UartRxFErr<br>r              | UartRxOErr<br>c           | UartRxBusy<br>r           | UartRxFull<br>r           |
| Reserved<br>h0056     |                           |                            |                              |                              |                              |                           |                           |                           |
| Reserved<br>h0057     |                           |                            |                              |                              |                              |                           |                           |                           |

**Table 6.12:** UART control registers

### 6.13 Counters

| Name<br>Address        | 7                         | 6                         | 5                          | 4                          | 3                          | 2                          | 1                          | 0                          |
|------------------------|---------------------------|---------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| RegCntA<br>h0058       | CounterA(7)<br>rw         | CounterA(6)<br>rw         | CounterA(5)<br>rw          | CounterA(4)<br>rw          | CounterA(3)<br>rw          | CounterA(2)<br>rw          | CounterA(1)<br>rw          | CounterA(0)<br>rw          |
| RegCntB<br>h0059       | CounterB(7)<br>rw         | CounterB(6)<br>rw         | CounterB(5)<br>rw          | CounterB(4)<br>rw          | CounterB(3)<br>rw          | CounterB(2)<br>rw          | CounterB(1)<br>rw          | CounterB(0)<br>rw          |
| RegCntC<br>h005A       | CounterC(7)<br>rw         | CounterC(6)<br>rw         | CounterC(5)<br>rw          | CounterC(4)<br>rw          | CounterC(3)<br>rw          | CounterC(2)<br>rw          | CounterC(1)<br>rw          | CounterC(0)<br>rw          |
| RegCntD<br>h005B       | CounterD(7)<br>rw         | CounterD(6)<br>rw         | CounterD(5)<br>rw          | CounterD(4)<br>rw          | CounterD(3)<br>rw          | CounterD(2)<br>rw          | CounterD(1)<br>rw          | CounterD(0)<br>rw          |
| RegCntCtrlCk<br>h005C  | CntDSEL(1)<br>rw          | CntDSEL(0)<br>rw          | CntCSEL(1)<br>rw           | CntCSEL(0)<br>rw           | CntBSEL(1)<br>rw           | CntBSEL(0)<br>rw           | CntASEL(1)<br>rw           | CntASEL(0)<br>rw           |
| RegCntConfig1<br>h005D | CntDDownUp<br>rw          | CntCDownUp<br>rw          | CntBDownUp<br>rw           | CntADownUp<br>rw           | CascadeCD<br>rw            | CascadeAB<br>rw            | CntPWM1<br>rw, 0 global    | CntPWM0<br>rw, 0 global    |
| RegCntConfig2<br>h005E | CapSel(1)<br>rw, 0 global | CapSel(0)<br>rw, 0 global | CapFunc(1)<br>rw, 0 global | CapFunc(0)<br>rw, 0 global | PWM1Size(1)<br>rw          | PWM1Size(0)<br>rw          | PWM0Size(1)<br>rw          | PWM0Size(0)<br>rw          |
| RegCntOn<br>h005F      |                           |                           |                            |                            | CntDEnable<br>rw, 0 global | CntCEnable<br>rw, 0 global | CntBEnable<br>rw, 0 global | CntAEnable<br>rw, 0 global |

**Table 6.13:** Counters control registers

### 6.14 LP comparators

| Name<br>Address      | 7                                     | 6                                     | 5                                     | 4                           | 3                          | 2                          | 1                          | 0                         |
|----------------------|---------------------------------------|---------------------------------------|---------------------------------------|-----------------------------|----------------------------|----------------------------|----------------------------|---------------------------|
| RegCmpdStat<br>h0072 | CmpdStat(3)<br>rc, 0 global           | CmpdStat(2)<br>rc, 0 global           | CmpdStat(1)<br>rc, 0 global           | CmpdStat(0)<br>rc, 0 global | CmpdOut(3)<br>r, 0 global  | CmpdOut(2)<br>r, 0 global  | CmpdOut(1)<br>r, 0 global  | CmpdOut(0)<br>r, 0 global |
| RegCmpdCtrl<br>h0073 | IrqOnRising-<br>Ch(2)<br>rw, 0 global | IrqOnRising-<br>Ch(1)<br>rw, 0 global | IrqOnRising-<br>Ch(0)<br>rw, 0 global | EnIrqCh(3)<br>rw, 0 global  | EnIrqCh(2)<br>rw, 0 global | EnIrqCh(1)<br>rw, 0 global | EnIrqCh(0)<br>rw, 0 global | Enable<br>rw, 0 global    |

**Table 6.14:** LP comparators control registers

### 6.15 Vmult and Vld registers

| Name<br>Address     | 7 | 6 | 5 | 4 | 3                     | 2                        | 1                        | 0                        |
|---------------------|---|---|---|---|-----------------------|--------------------------|--------------------------|--------------------------|
| RegVldCtrl<br>h007E |   |   |   |   | VldMult<br>rw, 0 cold | VldTune(2)<br>rw, 0 cold | VldTune(1)<br>rw, 0 cold | VldTune(0)<br>rw, 0 cold |
| RegVldStat<br>h007F |   |   |   |   |                       | VldIrq<br>r, 0 global    | VldValid<br>r, 0 global  | VldEn<br>rw, 0 global    |

**Table 6.15:** Vmult and Vld control registers

### 6.16 LCD driver registers

| Name<br>Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---|---|---|---|---|---|---|---|
| starts h8000    |   |   |   |   |   |   |   |   |

**Table 6.16:** LCD driver registers

## 7 Peripherals

The XE88LC04 includes usual microcontroller peripherals and some other blocks more specific to low-voltage or mixed-signal operation. They are 3 parallel ports, one input port (A), one IO and analog port (B) with analog switching capabilities and one general purpose IO port (C). A watchdog is available, connected to a prescaler. Four 8-bit counters, with capture, PWM and chaining capabilities are available. The UART can handle transmission speeds as high as 115kbaud.

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Low-power low-voltage blocks include a voltage level detector, two oscillators (one internal 0.1-4 MHz RC oscillator and a 32 kHz crystal oscillator) and a specific regulation scheme that largely uncouples current requirement from external power supply (usual CMOS ASICs require much more current at 5.5 V than they need at 2.4 V. This is not the case for the XE88LC04).

### 7.1 Counters

- 4 8-bit counters
- Daisy chain on 16 bits
- PWM on 8-16 bits
- Capture - compare on 16 bits
- Events and interrupts generation

### 7.2 Prescaler

- Interrupt generated with 1 second period for ultra low power hibernation mode

### 7.3 Watchdog

- 2 seconds watchdog

### 7.4 UART

- full duplex operation with buffered receiver and transmitter.
- Internal baudrate generator with programmable baudrate (300 - 115000 bauds).
- 7 or 8 bits word length.
- even, odd, or no-parity bit generation and detection
- 1 stop bit
- error receive detection : Start, Parity, Frame and Overrun
- receiver echo mode
- 2 interrupts (receive full and transmit empty)
- enable receive and/or transmit
- invert pad Rx and/or Tx

### 7.5 Xtal clock

The Xtal Oscillator operates with an external crystal of 32'768 Hz.

| symbol      | description  | min  | typ   | max  | unit | comments  |
|-------------|--|------|-------|------|------|---|
| f_clk32k    | nominal frequency  |      | 32768 |      | Hz   |   |
| st_x32k     | oscillator start-up time   |      | 1     | 2    | s    | for full precision  |
| duty_clk32k | duty cycle on the digital output   | 30   | 50    | 70   | %    |   |
| fstab_1     | relative frequency deviation from nominal, for a crystal with CL=8.2 pF and temperature between -40° and +85°C | -100 |       | +300 | ppm  | not included:<br>crystal frequency tolerance and aging<br>crystal frequency - temperature depen |

**Table 7.1:** Xtal oscillator specifications.

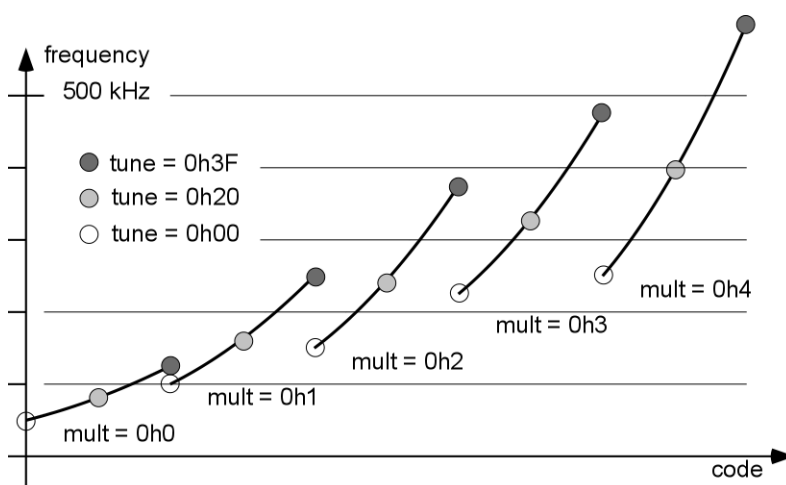
**Note:** Board layout recommendations for safer crystal oscillation and lower current consumption:  
 Keep lines xtal\_in and xtal\_out short and insert a VSS line between them.  
 Connect package of the crystal to VSS.  
 No noisy or digital lines near xtal\_in and xtal\_out.  
 Insert guards at VSS where needed.

## 7.6 RC oscillator

The RC Oscillator is always turned on at power-on reset and can be turned off after the optional Xtal oscillator has been started. The RC oscillator has two frequency ranges: sub-MHz (100kHz to 1MHz) and above-MHz (1MHz to max MCU frequency). Inside a range, the frequency can be tuned by software for coarse and fine adjustment.

**Note:** No external component is required for the RC oscillator.

The RC oscillator can be in 3 modes. In mode 1 (RC on), the RC oscillator and its bias are on. In mode 2 (RC ready), the RC oscillator is off and the bias is on. In mode 3 (RC off), the RC oscillator and the bias are off. RC ready mode is a compromise between power consumption and start-up time.



**Figure 7.1:** RC frequencies programming example for low range (typical values)

| symbol    | description           | min  | typ | max | unit       | comments                                   |
|-----------|-----------------------|------|-----|-----|------------|--|
| $F_{st}$  | frequency at start-up | 50   | 80  | 110 | kHz        |  |
| range     | range selection       | 1    |     | 10  |            | multiplies $F_{st}$                        |
| mult[3:0] | coarse tuning range   | 1    |     | 16  |            | 4 bits, multiplies $F_{st}$ * range        |
| tune[5:0] | fine tuning range     | 0.65 |     | 1.5 |            | 6 bits, multiplies $F_{st}$ * range * mult |
|           | fine tuning step      |      | 1.4 | 2   | %          |  |
| $T_{st}$  | start-up time         |      | 30  | 50  | $\mu s$    | bias current is off (RC off)               |
| $O_{st}$  | overshoot at start-up |      |     | 50  | %          | bias current is off (RC off)               |
| $T_{wu}$  | wakeup time           |      | 3   | 5   | $\mu s$    | bias current is on (RC ready)              |
| $O_{wu}$  | overshoot at wakeup   |      |     | 50  | %          | bias current is on (RC ready)              |
| jitter    | jitter rms            |      | 2   |     | $\text{‰}$ |  |

**Table 7.2:** RC specifications

## 7.7 Parallel IO ports

- 8 bit input port A with interrupt, reset and event generation.
- 8 bit input-output-analog port B with analog switching capabilities.

- 8 bit input-output port C.

| sym | description                    | condition    | min | typ | max | unit | Comments |
|-----|--------------------------------|--------------|-----|-----|-----|------|----------|
|     | Port A: low threshold limit    | Vbat = 1.2 V |     |     |     | V    |          |
|     | Port A: high threshold limit   |              |     |     |     | V    |          |
|     | output drop when sinking 1 mA  |              |     |     | 0.4 | V    |          |
|     | output drop when sourcing 1 mA |              |     |     | 0.4 | V    |          |
|     | Port A: low threshold limit    | Vbat = 2.4 V |     | 1   |     | V    |          |
|     | Port A: high threshold limit   |              |     | 1.5 |     | V    |          |
|     | output drop when sinking 1 mA  |              |     |     |     | V    |          |
|     | output drop when sinking 8 mA  |              |     |     | 0.4 | V    |          |
|     | output drop when sourcing 1 mA | Vbat = 5.0 V |     |     |     | V    |          |
|     | output drop when sourcing 8 mA |              |     |     | 0.4 | V    |          |
|     | Port A: low threshold limit    |              |     | 2   |     | V    |          |
|     | Port A: high threshold limit   |              |     | 3   |     | V    |          |
|     | output drop when sinking 1 mA  | Vbat = 5.0 V |     |     |     | V    |          |
|     | output drop when sinking 8 mA  |              |     |     | 0.4 | V    |          |
|     | output drop when sourcing 1 mA |              |     |     |     | V    |          |
|     | output drop when sourcing 8 mA |              |     |     | 0.4 | V    |          |
|     | pull-up, pull-down resistor    |              | 50  |     | 150 | kohm |          |

**Table 7.3:** IO pins performances

## 7.8 Voltage level detector

- Can be switched off, on or simultaneously with CPU activities
- Generates an interrupt if power supply is below a pre-determined level

The Voltage Level Detector monitors the state of the system battery. It returns a logical high value (an interrupt) in the status register if the supplied voltage drops below the user defined level.

| symbol           | description                  | min    | typ  | max  | unit | comments         |      |
|------------------|------------------------------|--------|------|------|------|------------------|------|
| Vth              | Threshold voltage            | Note 1 |      |      | V    | trimming values: |      |
|                  |                              |        |      |      |      | VldRange         | Vld' |
|                  |                              |        | 1.53 |      |      | 0                | 0    |
|                  |                              |        | 1.44 |      |      | 0                | 0    |
|                  |                              |        | 1.36 |      |      | 0                | 0    |
|                  |                              |        | 1.29 |      |      | 0                | 0    |
|                  |                              |        | 1.22 |      |      | 0                | 1    |
|                  |                              |        | 1.16 |      |      | 0                | 1    |
|                  |                              |        | 1.11 |      |      | 0                | 1    |
|                  |                              |        | 1.06 |      |      | 0                | 1    |
|                  |                              |        | 3.06 |      |      | 1                | 0    |
|                  |                              |        | 2.88 |      |      | 1                | 0    |
|                  |                              |        | 2.72 |      |      | 1                | 0    |
|                  |                              |        | 2.57 |      |      | 1                | 0    |
|                  |                              |        | 2.44 |      |      | 1                | 1    |
|                  |                              |        | 2.33 |      |      | 1                | 1    |
|                  |                              |        | 2.22 |      |      | 1                | 1    |
|                  | 2.13                         |        | 1    | 1    |      |                  |      |
| T <sub>EOM</sub> | duration of measurement      |        | 2.0  | 2.5  | ms   | Note 2           |      |
| T <sub>PW</sub>  | Minimum pulse width detected |        | 875  | 1350 | us   | Note 2           |      |

**Table 7.4:** Voltage level detector operation

**Note:**

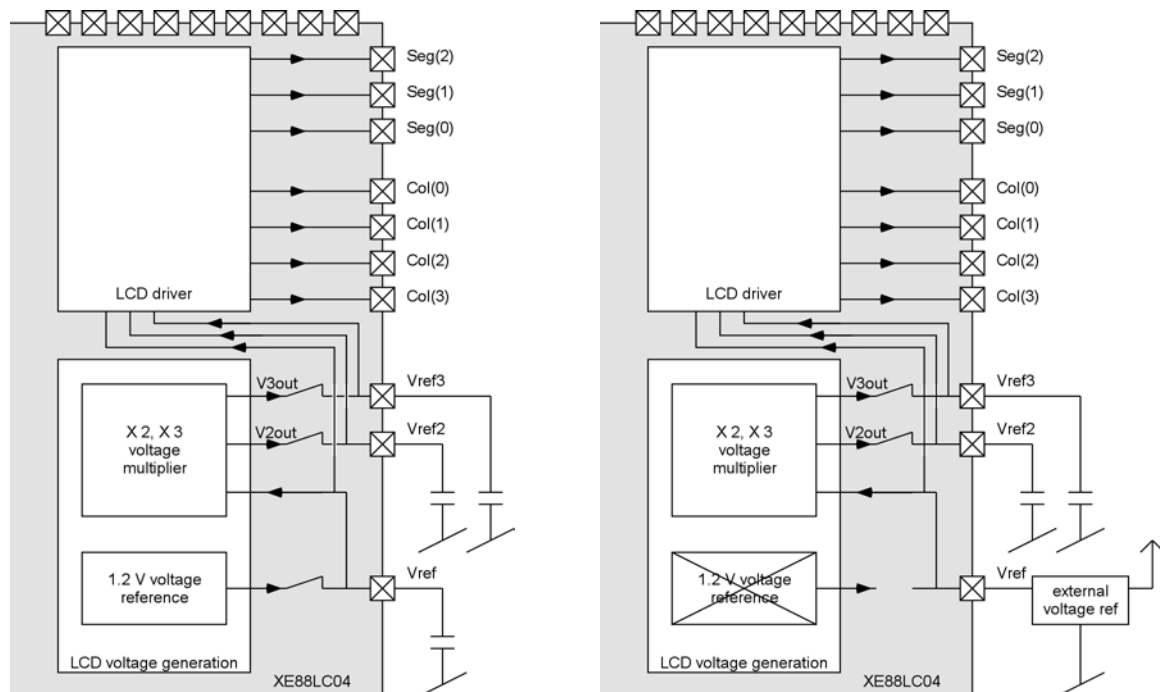
- 1) Absolute precision of the threshold voltage is  $\pm 10\%$ .
- 2) This timing is respected in case the internal RC or crystal oscillators are selected. Refer to the clock block documentation in case the external clock is used.

## 8 LCD drivers

The XE88LC04 includes LCD drivers for up to 120 segments. Multiplex can be chosen between 1 and 4. Intermediate voltages for multiplex signals can be generated on chip, even at very low power supply, thanks to a 1.2 V voltage reference and to 2 voltage multipliers.

The voltage generator of the XE88LC04 can be used in a multitude of ways: for generating absolute voltages (above or below Vbat), for generating voltages relative to Vbat, or for generating voltages relative to an external reference. This great variety of possibilities make possible to have devices compensated for temperature, or to operate LCD with good contrast even with limited voltage supply.

Registers h0068 to h0076 carry the segment value, register h0077 carries the Vref setup (on-off), Vref multiplier setup (on-off), LCD update frequency (off, 16 Hz, 32 Hz, 64 Hz), LCD size (25 lines or 30 lines) and multiplex selection (1, 2, 3 or 4).



**Figure 8.1:** Generating absolute voltages for the LCD driver, either with internal reference (left) or



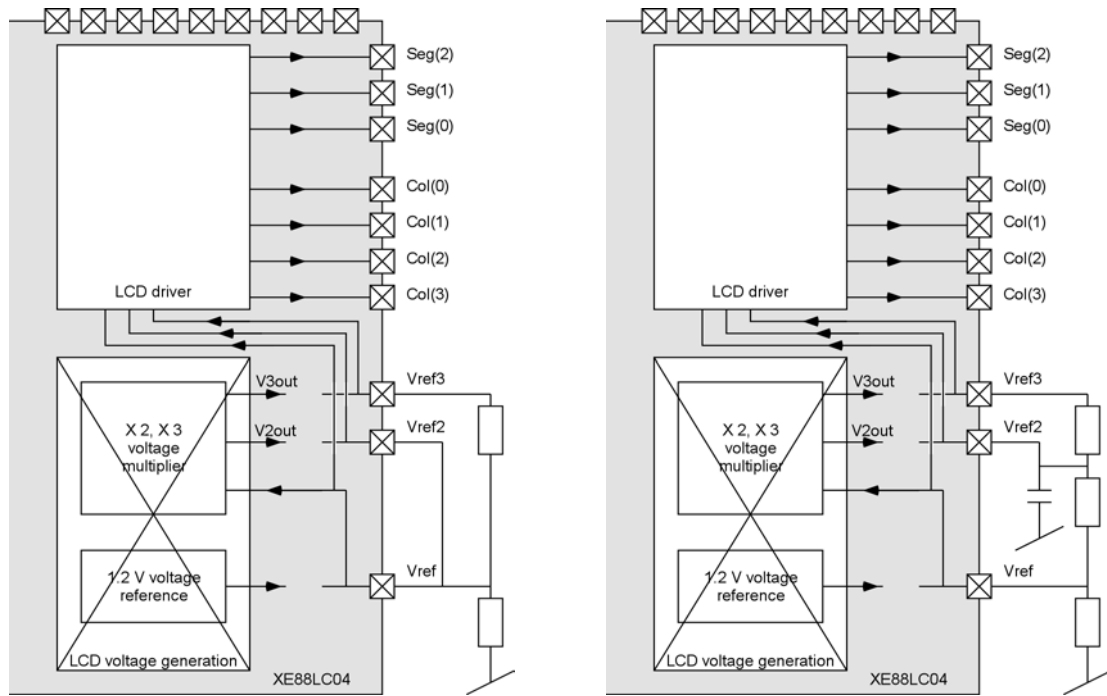


Figure 8.2: Using voltages proportional to Vbat (power supply) for multiplex by two (left) or three or four

## 9 Physical description

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### 9.1 BGA package

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Figure 9.1:

## 10 Contacting XEMICS

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You will find more information about the XE88LC04 and other XEMICS products, as well as the addresses of our representatives and distributors for your region on <http://www.xemics.com>.

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